Low Power HDMI™ 1.2 Transmitter

A CoolHD™ family product

- HDMI 1.2 compliant transmitter with patented ultra low power technology
- Optional HDCP function with internal keys
- Supports link date rates up to 165Mpixel/sec
- **Low power consumption (standby mode and normal mode)**

  - Less than 1.5 mW in 480i mode

  - Less than 1.5 mW in 480p/720p/1080i mode
- Flexible video pixel input interface, supports DVD and HD MPEG decoders

  - 24-bit RGB/YCbCr 4:4:4

  - 16/20/24-bit YCbCr 4:2:2

  - 8/10/12-bit YC Mux(ITU 601 and 656)

  - YCbCr-to-RGB colour space conversion

  - YCbCr 4:2:2 to 4:4:4 up-sample

  - 12-bit, dual-edge clocking input mode

  - 8-bit DDR YCMux (ITU 601 and 656)
- Advanced digital audio interface

  - 8-channel I^2S support Dolby Digital and DVD-Audio

  - Up to 6 channels 1-bit super audio support

  - S/PDIF supports PCM, Dolby Digital and DTS digital audio transmission

  - IEC 60958 or 61937 compatible

  - 2:1 and 4:1 down-sample to handle 96 KHz and 192 KHz audio stream
- Software-controlled power management
- Backward compatible with DVI1.1
- Programmable output swing
- 2KV ESD performance
- RoHS compliant and Halogen free package
- Package offered

  - 48-pin and 64-pin QFN

  - 80-pin LQFP

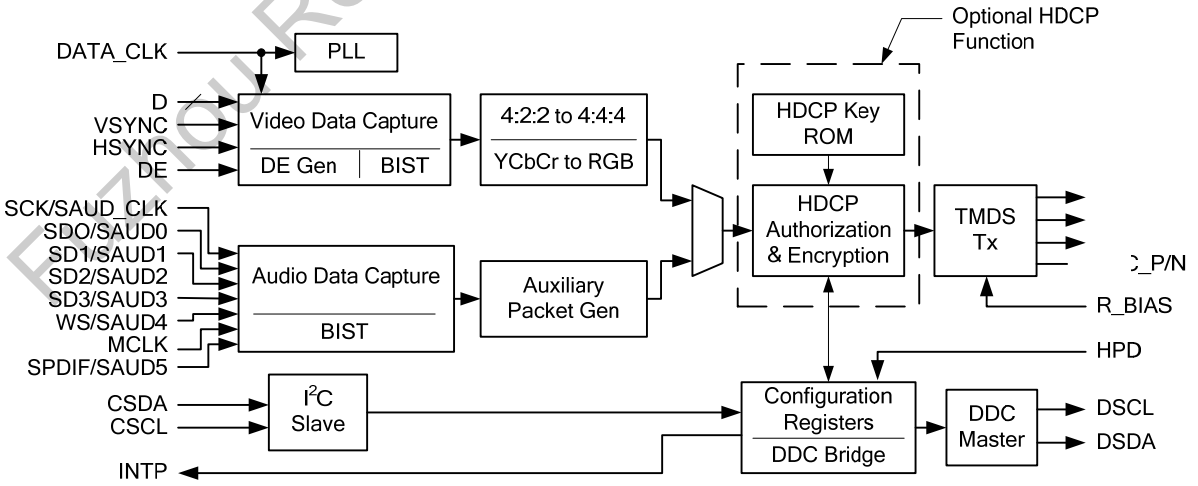
  - 81-pin BGA

ANX7150, a CoolHD™ family product, is an ultra-low power HDMI Transmitter designed for portable applications including media players, camcorders, digital still cameras. Using proprietary circuit techniques, ANX7150 uses less than 95% of the power used by similar devices.

ANX7150 can be ordered with an optional HDCP 1.1 function (including internal keys) to support content protection.

Built-in video pattern generator and audio tone generator are included for system self-test. Power requirement is 1.8V and 3.3V.

For package and HDCP options, refer to the parts ordering information.



ANX7150 Block Diagram

1 Typical Application Block Diagram

The block diagram of ANX7150 is shown in Figure 1-1. The ANX7150 chip has flexible video and audio input interfaces to receive the video and audio data from Video/Audio Processor. The ANX7150 can be controlled and configured by the system host micro controller through the dedicated host I^2C control interface. The I^2C control interface is also used to read HDMI sink E-EDID data received by DDC master through the DDC link, which means the host controller does not need extra DDC master for reading E-EDID data. The ANX7150 packages the video data, audio data and other control information into the TMDS link and generated HDMI signals that fully support HDMI 1.2 standard.

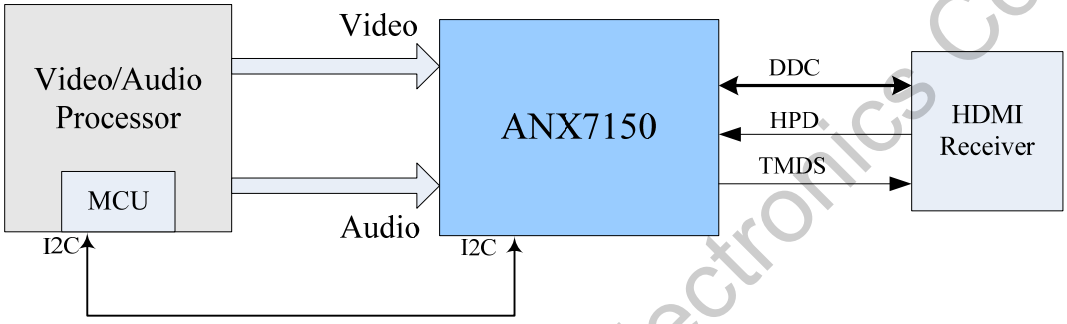


Figure 1- 1 System application of ANX7150

2 Pin Descriptions

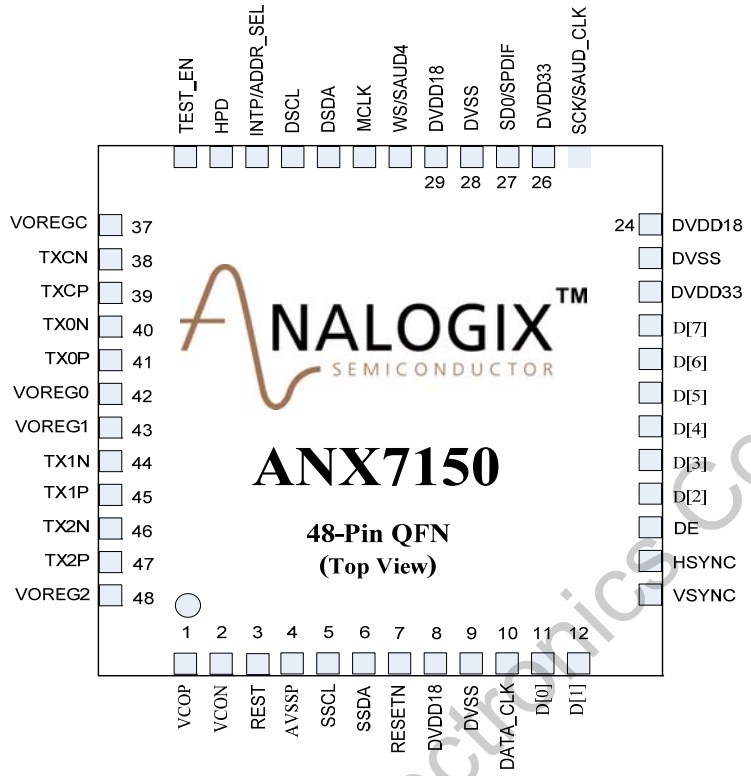


Figure 2-1 ANX7150 48-pin QFN

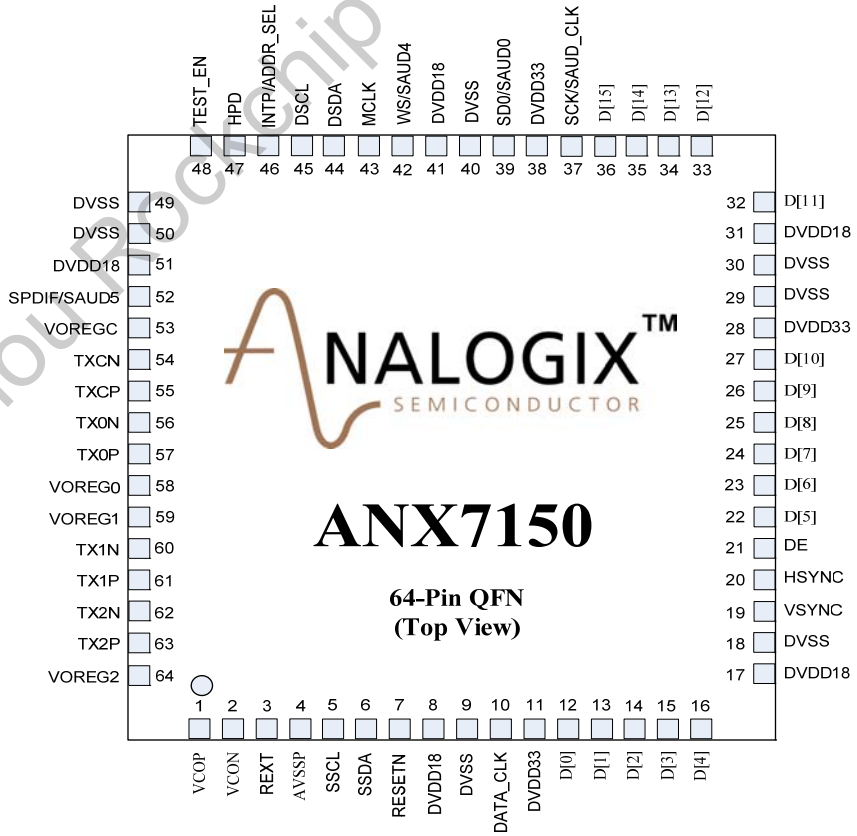


Figure 2-2 ANX7150 64-pin QFN

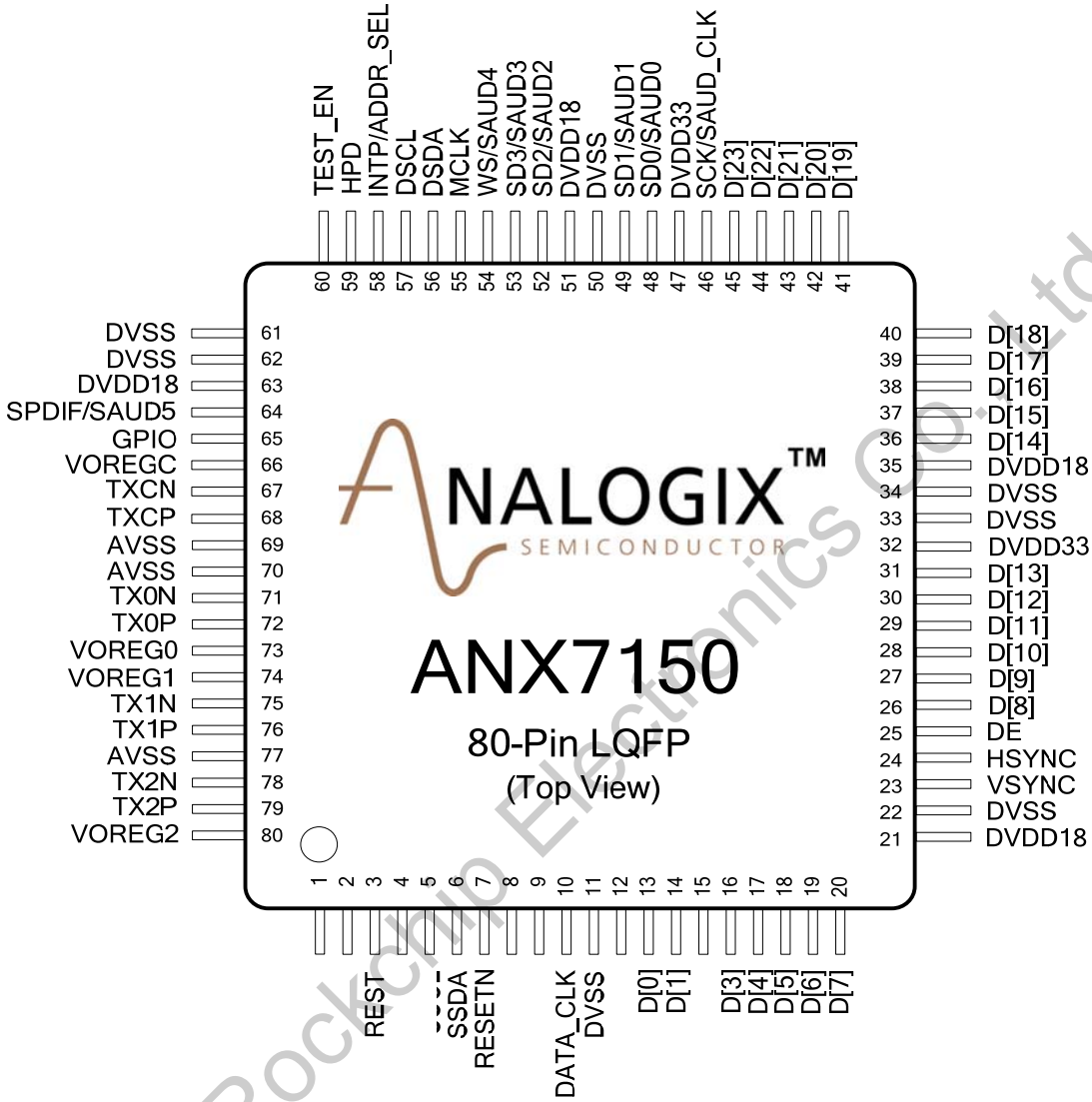


Figure 2-3 ANX7150 80-pin LQFP

	1	2	3	4	5	6	7	8	9	
A	VOREG 2	TX1P	TX1N	VOREG 1	TX0P	TX0N	AVSS	TXCP	TXCN	A
B	TX2N	AVSSP	AVSS	VOREG 0	GPIO	TEST_E N	AVSS	INTP/ ADDR_ SEL	VOREG C	B
C	TX2P	SSCL	REXT	NC	SPDIF/ SAUD5	HPD	DVSS	DSDA	DSCL	C
D	VCOP	SSDA	RESET_ N	DVSS	DVDD18	DVDD18	DVSS	MCLK	WS/SAU D4	D
E	VCON	DATA_C LK	DVDD18	DVSS	DVSS	DVSS	DVDD33	SD2/SAI D2	SD3/SA UD3	E
F	D0	D1	DVDD33	DVDD33	DVSS	DVSS	SCK/ SAUD_ CLK	SD0/SAI D0	SD1/SA UD1	F
G	D2	D3	D4	DVDD18	D12	DVDD18	D23	D22	D21	G
H	D5	D6	HSYNC	D9	D11	D14	D16	D18	D20	H
J	D7	VSYNC	DE	D8	D10	D13	D15	D17	D19	J
	1	2	3	4	5	6	7	8	9	

Figure 2-4 ANX7150 81-pin BGA

2.1 Pin Definition

2.1.1 Video Interface Pins

Table 2-1 Video Interface Pins

81-pin	80-pin	64-pin	48-pin	Name	Type	Description
E2	10	10	10	DATA_CLK	LVTTL	Pixel clock input. 25 MHz ~ 165 MHz.
J3	25	21	15	DE	LVTTL	Data enable.
J2	23	19	13	VSYNC	LVTTL	Vertical sync. input control signal.
H3	24	20	14	HSYNC	LVTTL	Horizontal sync. input control signal.
F1,F2,G1,G2, G3,H1,H2,J1, J4,H4,J5,H5, G5,J6,H6,J7, H7,J8,H8,J9, H9,G9,G8,G7	13-20, 26-31, 36-45	12-16, 22-27, 32-36	11,12, 16-21	D	LVTTL	Pixel data input.

2.1.2 Audio Interface Pins

Table 2-2 Audio Interface Pins

81-pin	80-pin	64-pin	48-pin	Name	Type	Description
C5	64	52	NC	SPDIF/SAUD5	LVTTL	S/PDIF audio input or super audio input channel 5.
D8	55	43	31	MCLK	LVTTL	Audio master clock input.
F7	46	37	25	SCK/SAUD_CLK	LVTTL	I^2S audio clock or super audio clock input.
D9	54	42	30	WS/SAUD4	LVTTL	I^2S audio word select or super audio input channel 4.
E9	53	NC	NC	SD3/SAUD3	LVTTL	8-channel I^2S audio data input or super audio input channel 0–3. For 48-pin QFN device, it is S/PDIF audio input.
E8	52	NC	NC	SD2/SAUD2	LVTTL	
F9	49	NC	NC	SD1/SAUD1	LVTTL	
F8	48	39	27	SD0/SAUD0 SD0/SPDIF	LVTTL	

2.1.3 I2C Interface Pins

Table 2-3 I2C Interface Pins

81-pin	80-pin	64-pin	48-pin	Name	Type	Description
C2	5	5	5	SSCL	LVTTL	Slave I^2C clock input.
D2	6	6	6	SSDA	LVTTL	Slave I^2C data. Open drain output.
C9	57	45	33	DSCL	LVTTL	DDC (Master I^2C) clock output.
C8	56	44	32	DSDA	LVTTL	DDC (Master I^2C) data. (open drain output).
B6	60	48	36	TEST_EN	LVTTL	Scan test enable

2.1.4 Serial Interface Pins

Table 2-4 Serial Interface Pins

81-pin	80-pin	64-pin	48-pin	Name	Type	Description
A5,A6	71,72	56,57	40,41	TX0N/P	TMDS	Channel 0 TMDS differential output.
A2,A3	75,76	60,61	44,45	TX1N/P	TMDS	Channel 1 TMDS differential output.

B1,C1	78,79	62,63	46,47	TX2N/P	TMDS	Channel 2 TMDS differential output.
A8,A9	67,68	54,55	38,39	TXCN/P	TMDS	Differential TMDS clock output.

2.1.5 Miscellaneous Signal

Table 2-5 Miscellaneous Pins

81-pin	80-pin	64-pin	48-pin	Name	Type	Description
D3	7	7	7	RESETN	Schmitt	Reset signal, active low.
C6	59	47	35	HPD	LVTTL	Hot-plug detect signal.
B8	58	46	34	INTP	LVTTL	Interrupt output signal[1]. During chip reset, used as I^2C slave device address select
C3	3	3	3	REXT	Analog	Bias circuit resistor input, 3.5K Ohms to Ground
D1	1	1	1	VCOP	Analog	Analog filtering, positive
E1	2	2	2	VCON	Analog	Analog filtering, negative
B5	65	NC	NC	GPIO	Analog	Generic purpose IO

1. The INTP pin needs a weak pull-up of approximately 10KOhm

2.1.6 Power and Ground Pins

Table 2-6 Power and Ground Pins

81-pin	80-pin	64-pin	48-pin	Name	Type	Description
D5,D6,E3,G4,G6	8, 21, 35, 51, 63	8, 17, 31, 41, 51	8, 24, 29	DVDD18	Power	1.8V core power pins
F3,F4,E7	12, 32, 47	11, 28, 38	22,26	DVDD33	Power	3.3V power pins
C7,D4,D7,E4,E5, E6,F5,F6,	9, 11, 22, 33, 34, 50, 61, 62	9, 18, 29, 30, 40, 49, 50	9, 23, 28	DVSS	Ground	Digital ground pins
A7,B7,B3,	69, 70, 77	NC	NC	AVSS	Ground	Analog ground pins
B2	4	4	4	AVSSP	Ground	Analog ground pin

2.1.7 Internal Pins

Table 2-7 Internal Pins

81-pin	80-pin	64-pin	48-pin	Name	Type	Description
B4,A4,A1,B9	66,73 74,80	53,58 59,64	37,42,43,48	VOREG 0 VOREG 1 VOREG 2 VOREG C		Internal analog power pins, which are not provided for customer, Every pin provides internal using voltage individually.

3 Electrical Specifications

3.1 Absolute Maximum Conditions

Permanent damage may occur if absolute maximum conditions are violated. Refer to Section 3.2 for functional operating limits.

Table 3-1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
DVDD33	Digital I/O supply voltage	-0.3		3.8	V
DVDD18	Digital core logic supply voltage	-0.3		1.96	V
V_{IN}	Input voltage	-1.0		DVDD33+0.3	V
T_J	Junction Temperature	--		125	°C
ESD_H	ESD protection (Human body model)			6	KV

1. Power supply sequencing must guarantee these conditions.

3.2 Normal Operating Conditions

Table 3-2 Normal operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
DVDD33	Digital I/O supply voltage[1]	3.0	3.3	3.6	V
DVDD18	Digital core logic supply voltage	1.62	1.8	1.96	V
V_{RIP}	Power supply noise[2]	--	--	--	mVp-p
T_A	Ambient temperature	-10	25	75	°C
Q_{JA}	Package thermal resistance, no air flow[3]		27		°C/W

1. DVDD33 and AVDDXX should be controlled from the same power supply source.
2. Measured at the input pin after power supply filtering.
3. ePad soldered to board.

3.3 DC Specifications

These specifications apply under normal operating conditions with output pin load CL= 10pF unless otherwise stated. Minimum output drives are specified at 70 °C ambient temperature, 3.0V supply voltage. Maximum output drives are specified at 0 °C, 3.6V supply voltage.

3.3.1 Input and Output Parameters

Table 3-3 Input and output parameters

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	High level input voltage	2.0			V
V_{IL}	Low level input voltage			0.8	V
V_{T+}	Low to high threshold voltage	1.9			V
V_{T-}	High to low threshold voltage			0.7	V
V_{OH}	High level output voltage	2.4			V
V_{OL}	Low level output voltage			0.4	V

Symbol	Parameter	Min	Typ	Max	Units
I_{IL}	Input leakage current	-10		10	uA
I_{DDPD}	Output leakage current	-10		10	uA
R_{PD}	Internal pull-down resistor		83		KΩ
I_{OPD}	Output pull-down current		60	75	uA
I_{IPD}	Input pull-down current		60	75	uA

3.3.2 Power Consumption

Current consumption is a function of the link frequency of the selected HDMI input.

Table 3-4 Power Consumptions

Item	Typical Values		Total Power	Units
	DVDD33	DVDD18		
Stand-by(No AV input)	0.38	0.12	1.08	mW
720*480p@60Hz, 27MHz	0.25	0	0.9	mW
1280*720p@60Hz, 74.25MHz	0.33	0	1.1	mW

3.3.3 Slave I²C Interface Specifications

The I2C Interface operates at a reduced signaling level to better match the operating voltages of the Intel® product. The specifications for the reduced operating voltage are provided in Table 3-5. In addition, the Slave I2C Interface must be compliant with the AC specifications provided in the I2C-Bus Specification.

Table 3-5 Slave I2C DC Specifications

Symbol	Parameter	Min	Typ	Max	Units
V_{IN}	Input voltage range [1]	-0.25	--	1.35	V
V_{IL}	Low level input voltage	--	--	0.3	V
V_{IH}	High level input voltage	0.8	--	--	V
V_{OL}	Low level output voltage	--	--	0.2	V
I_{IL}	Input leakage current (Hi-Z)	--	--	50	uA
Z_{OUT}	Output impedance	--	--	50	ohms
C_{IN}	Input capacitance	--	--	3.0	pF
C_L	I2C signal load capacitance	--	--	20	pF

1. Includes high level output voltage (VOH) on the Slave I2C interface, where VOH is established by a pull-up to the 1.1V power supply.

3.4 AC Specifications

3.4.1 HDMI Output Timing

These specifications apply under normal operating conditions with output pin load C_L = 10 pF unless otherwise stated.

Table 3-6 HDMI Output Timings

Symbol	Parameter	Min	Typ	Max	Units
S_{LH}	TMDS differential output rise time (20%-80%) [1]	100			ps
				0.25	T_{BIT} [2]

S_{HL}	TMDS differential output fall time (80%-20%)	80			ps
				0.2	T_{BIT}
T_{SDF}	Delay from DE falling edge to VSYNC or HSYNC rising edge	1			T_{CP}
T_{SDR}	Delay from VSYNC or HSYNC falling edge to DE rising edge	1			T_{CP}

1. Limits are defined by the HDMI Specification.
2. T_{BIT} is the time required to carry a single bit across an HDMI channel, and is governed by the active input clock. (10 x T_{BIT}) = T_{CP}

3.4.2 Digital Video Data Input Timing

These specifications apply under normal operating conditions with output pin load C_L = 10 pF unless otherwise stated.

Table 3-7 Digital Video Input Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{CDC}	DATA_CLK input duty cycle	15		85	%
T_{CJ}	DATA_CLK input peak-to-peak jitter tolerance [1]			2	ns
Single-edge clock mode (one pixel per clock)					
T_{CP}	Clock period of DATA_CLK	5.56		40	ns
f_{CP}	Clock frequency of DATA_CLK	25		180	MHz
T_{DSF}	Data set-up time to DATA_CLK falling edge	0.6			ns
T_{DHF}	Data hold time from DATA_CLK falling edge	1			ns
T_{DSR}	Data set-up time to DATA_CLK rising edge	0.6			ns
T_{DHR}	Data hold time from DATA_CLK rising edge	1			ns
Dual-edge clock mode (DDR Mode)					
T_{CPD}	Clock period of DATA_CLK, DDR input mode	11.12		80	ns
f_{CPD}	Clock frequency of DATA_CLK, DDR input mode	12.5		90	MHz
T_{DSD}	Data set-up time to DATA_CLK rising or falling edge	0.6			ns
T_{DHD}	Data hold time from DATA_CLK rising or falling edge	1			ns

1. Actual jitter tolerance may be higher depending on jitter phase modulation frequency.

3.4.3 Audio Data Input Timing

3.4.3.1 I²S Input Port Timing

These specifications apply under normal operating conditions with output pin load C_L = 10 pF unless otherwise stated.

Table 3-8 Audio Data Input Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{SI2S}	Audio Sample Rate (2 channels)	32		192	kHz
	Audio Sample Rate (>2 channels)	32		192	kHz
T_{CYCI2S}	Cycle Time			1	UI
T_{DCI2S}	Clock duty cycle	90%		110%	UI
T_{SUI2S}	Set-up time	5			ns
T_{HI2S}	Hold time	1.5			ns

3.4.3.2 S/PDIF Input Port Timing

These specifications apply under normal operating conditions with output pin load C_L = 10 pF unless otherwise stated.

Table 3-9 S/PDIF Input Port Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{SSPDIF}	Audio Sample Rate (2 channels)	32		192	kHz
T_{SPCYC}	S/PDIF cycle time [1]			1	UI
$T_{DC, SPDIF}$	S/PDIF duty cycle	90		110	%UI
T_{MCLK}	MCLK cycle time	20.8			ns
f_{MCLK}	MCLKOUT frequency			48	MHz
T_{DCMCLK}	MCLKOUT duty cycle	30		70	%
T_{DLYAUD}	Audio pipeline delay		30	70	µs

1. S/PDIF cycle time is proportional to audio sample rate.

4 Functional Descriptions

4.1 Video Capture Input Modes

Video data can be input to the ANX7150 in various 12-bit or 24-bit interface formats. Single or dual-edge clock latching is supported. Pixel rates up to 165 MHz enables video formats such as 1080p and WUXGA (1200 x 1920 at 60 Hz) with reduced blanking. HSYNC and VSYNC inputs are provided, or embedded sync can be detected when using ITU.656 format. A DE input is also provided, or a DE blanking period can be generated internally based on HSYNC timing and register settings. To comply with the 4:4:4 RGB output base level requirement of HDMI, a 4:2:2 to 4:4:4 sample rate interpolation filter is included, as well as a YCbCr to RGB color-space converter; either ITU.601 or ITU.709 color-matrix coefficients can be selected.

4.2 DE Generator and Video BIST Function

The ANX7150 chip includes logic to construct a DE signal from the incoming HSYNC, VSYNC and clock. Registers are programmed to enable this DE signal to define the size of the active display region. This feature is useful when interfacing to MPEG decoders which do not provide a specific DE output signal.

The video BIST function within this block internally generates several of the most popular video formats according to the specified format selection. These BIST video formats simplify the chip debug.

4.3 Audio Capture and Audio BIST

The audio capture block takes the S/PDIF, I^2S or Super-audio input. The S/PDIF stream can carry two-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets in accordance with the HDMI 1.2 specification. The audio capture block supports audio sampling rates from 32 kHz to 192 kHz.

The appropriate registers must be configured to accept the input audio format. This information is passed over the HDMI link in the CEA-861B Audio Info packets.

The audio BIST function in this block generates sine wave with controllable amplitude and frequency. It is used conveniently to test the audio output of the HDMI receiver. The sine wave amplitude and frequency are set by the registers.

4.4 HDMI Processor Datapath

The HDMI processor block takes the video data from the video capture block and passes it through a video data repeater block. The video data is repeated if it is 2X or 4X mode. The color space converter and up converter that follow convert the video data if necessary. The audio data from the audio FIFO passes to the Aux. Packet generator block and merges with the video data to form the HDMI link frame. The link data is encoded with the TMDS encoder and traverses an output FIFO to perform clock domain conversion. The output of the FIFO is synchronized with the 'tx_clk' from the transmitter analog core.

4.4.1 HDCP Encryption Engine/XOR Mask

The HDCP encryption engine contains all necessary logic to encrypt the incoming audio and video data. The encryption process is entirely controlled by the system microcontroller/microprocessor through a set sequence of register reads and writes. Preprogrammed HDCP keys and Key Selector Value (KSV) stored in the internal EEPROM are used in the encryption process. A resulting calculated value is applied to an XOR mask during each clock cycle to encrypt the audio/video data.

4.4.2 TMDS Encoder

The TMDS encoder performs 8-to-10-bit TMDS encoding on the audio/video/aux data received from the HDCP XOR mask. This data is output to three TMDS differential data lines along with a TMDS differential clock.

4.4.3 HDCP Key EEPROM

The ANX7150 comes pre-programmed with a set of production HDCP keys stored in the internal EEPROM. System manufacturers do not need to purchase key sets from the Digital-Content LLC. The pre-programmed HDCP keys provide the highest level of security, as there is no way to read out the keys once the devices are programmed.

4.4.4 Interrupt Output

The INTP pin outputs a signal to interrupt the microcontroller on conditions inside the ANX7150, including:

- Monitor Detect (either from the HPD input level, or from the Receiver Sense feature)
- VSYNC (useful for synchronizing a microcontroller to the vertical timing interval)
- Error in the audio format

A connected display may be detected with the internal Receiver Sense logic. This is useful to the host controller monitoring the chip. The state of Receiver Sense may be output on the INTP pin as a level or as an interrupt of either polarity.

5 Package Specifications

5.1 ANX7150 48-Pin QFN Package Drawings

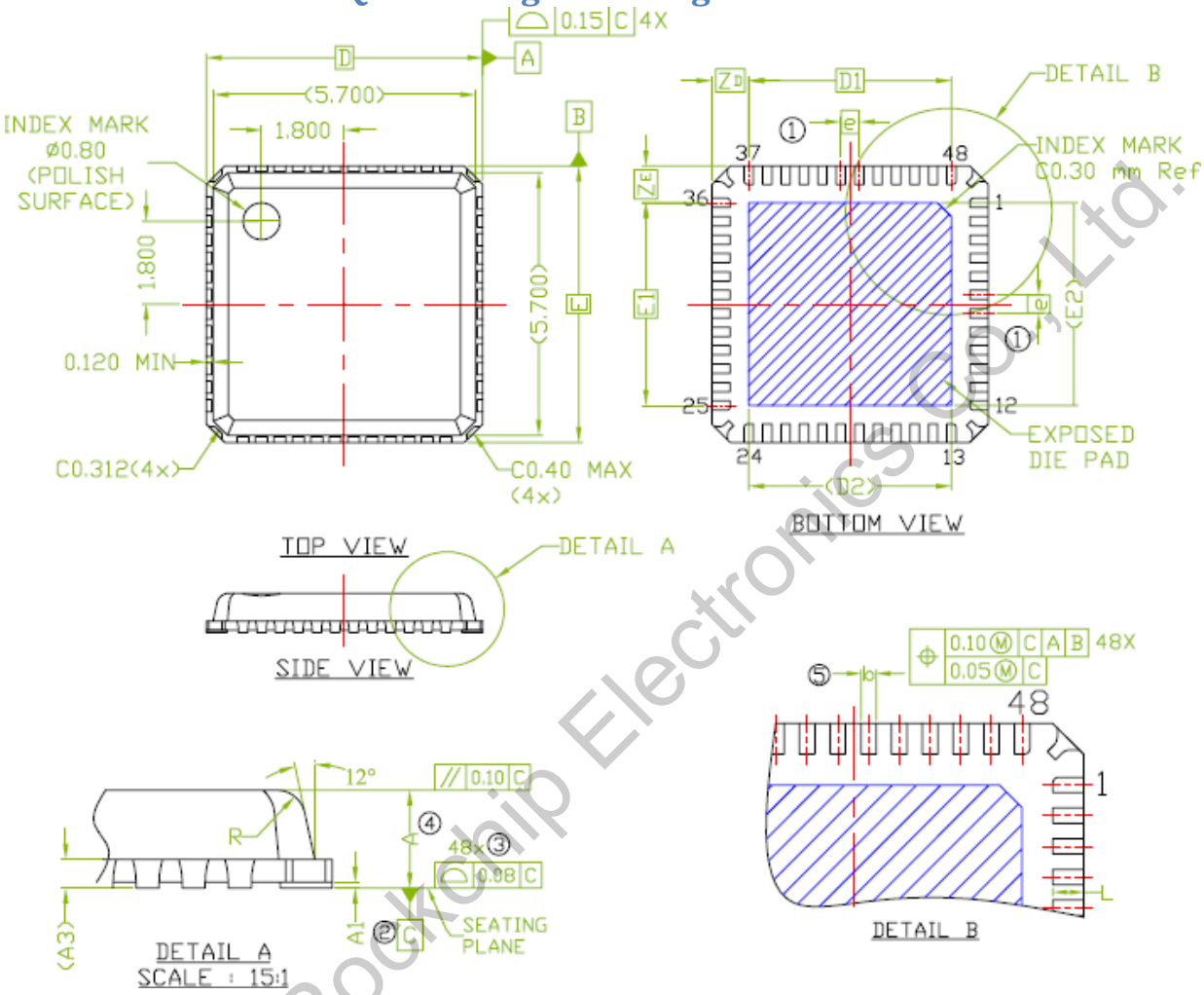


Figure 5-1 ANX7150 48-pin QFN Package

ANX7150 48-PIN QFN Package Dimensions

Ref	Min	Nom	Max
A	-	0.80	0.90
A1	0.00	0.02	0.05
A3		0.20 Ref	
D		6.00 BSC	
D1		4.40 BSC	
E		6.00 BSC	
E1		4.40 BSC	
e		0.40 BSC	
R		0.20~0.25	
ZD		0.80 BSC	
ZE		0.80 BSC	

LF Ref	Symbol	Min.	Type	Max
L-47-05057	b	0.15	0.20	0.25
	L	0.30	0.40	0.50
	D2	4.30	4.40	4.50
	E2	4.30	4.40	4.50

Notes:

1. All dimensions are in millimeters.
2. 'e' represents the basic terminal pitch.
3. Datum 'C' is the mounting surface, with which the package is in contact.
4. Specifies the vertical shift of the flat part of each terminal from the mounting surface.
5. Dimension 'A' includes package warpage.
6. Dimension 'b' applies to metalized terminal and is measured between 0.15mm and 0.3mm from terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measure in the radius area.
7. Package dimensions conform to JEDEC MO-220 Rev K, Variations VJJE-1, except D2 and E2.

5.2 ANX7150 80-Pin LQFP Package Drawings

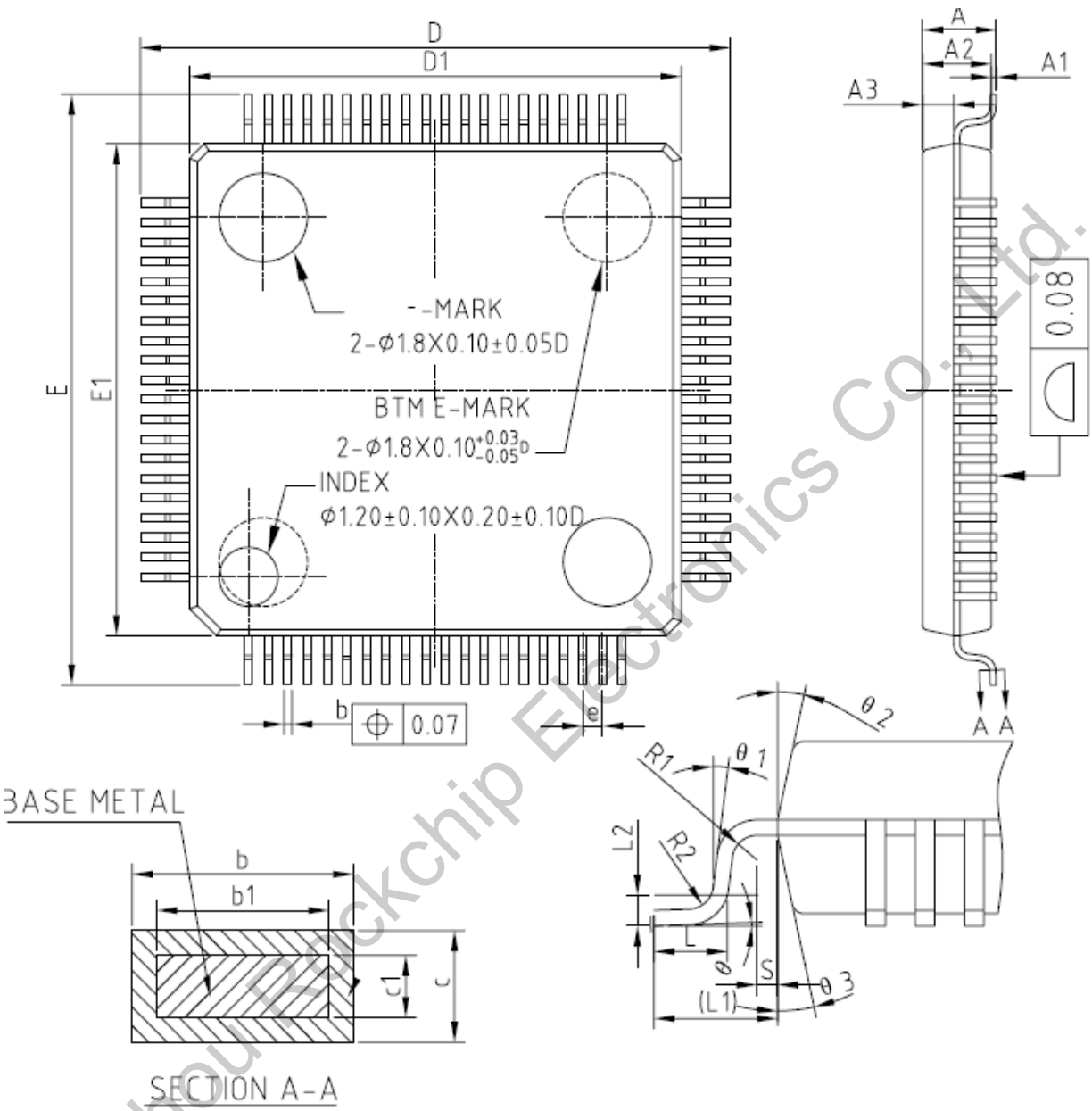


Figure 5-2 ANX7150 80-pin LQFP Package

ANX7150 80-PIN LQFP Package Dimensions

Ref	Min	Nom	Max
A	-	--	1.60
A1	0.05	--	0.20
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.13	--	0.23
B1	0.13	0.16	0.19
c	0.13	--	0.18

C1	0.12	0.13	0.14
D	11.80	12.00	12.20
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25BSC		
R1	0.08	--	--
R2	0.08	--	0.20

θ		3.5°	7°
Θ1	0°	--	--
Θ2	11°	12°	13°
Θ3	11°	12°	13°

5.3 ANX7150 81-Pin BGA Package Drawings

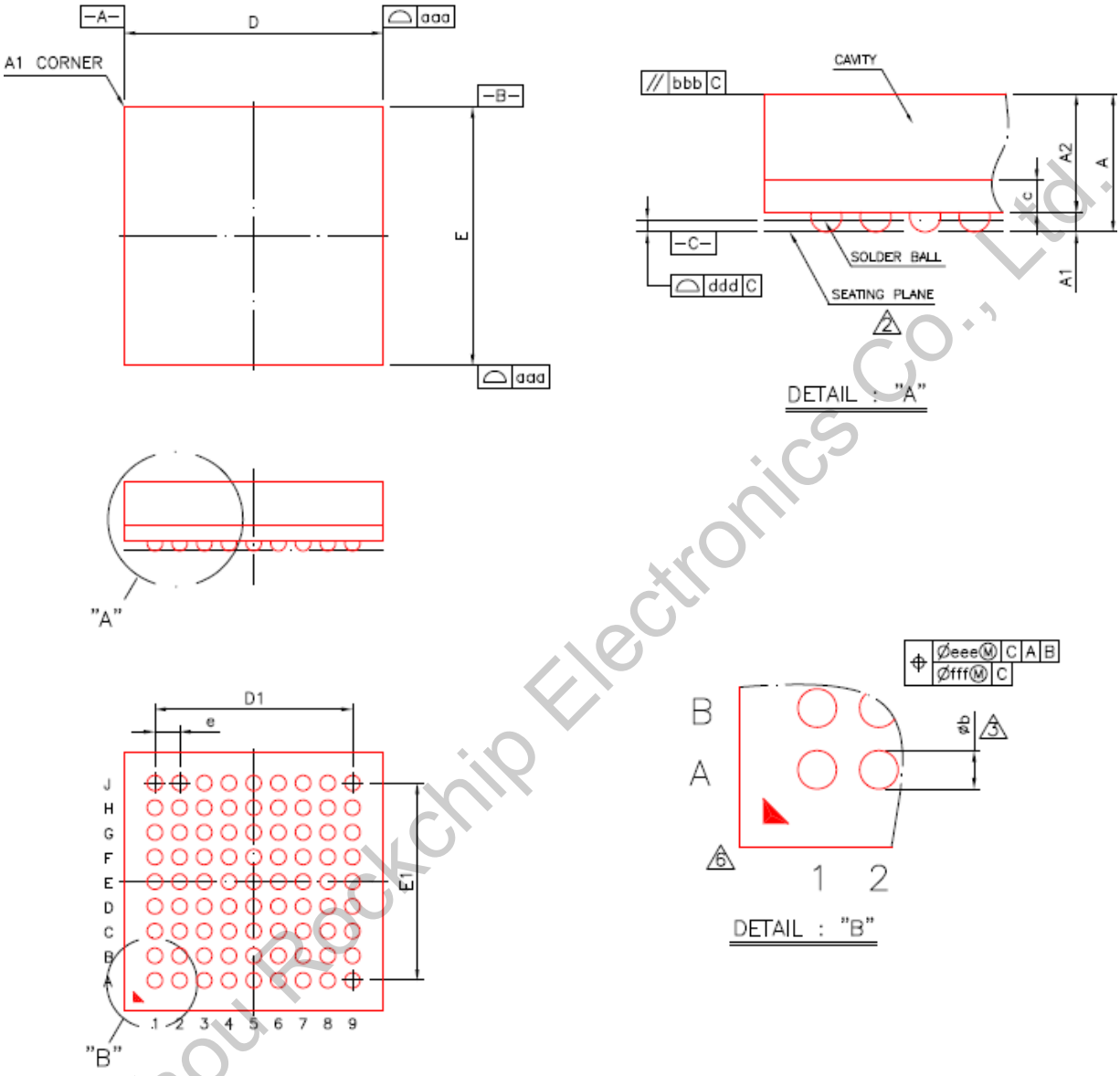


Figure 5-3 ANX7150 81-pin BGA Package

ANX7150 81-PIN BGA Package Dimensions

Ref	Min	Nom	Max
A	--	--	1.30
A1	0.11	0.16	0.21
A2	0.91	0.96	1.01
c	0.22	0.26	0.30
D	4.10	4.20	4.30
E	4.10	4.20	4.30
D1	--	3.20	--

E1	--	3.20	--
e	--	0.40	--
b	0.20	0.25	0.30
aaa	0.10		
bbb	0.10		
ddd	0.08		
eee	0.15		
fff	0.05		

Notes:

1. CONTROLLING DIENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT: JEDEC MO-195.
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd.

6 Ordering Information

The ANX7150 device is available with QFN and LQFP package options and an HDCP option. Table 6-1 and Figure 6-1 show the part ordering information and the corresponding package markings. Contact Analogix for further information.

Table 6-1 ANX7150 Ordering Information

Part No.	Description	Availability
ANX7150F	No HDCP function 48 pin, 6 x 6 mm, QFN package	July, 2009
ANX7150FH	HDCP function enabled 48 pin, 6 x 6 mm, QFN package	July, 2009
ANX7150S	No HDCP function 64 pin, 8 x 8 mm, QFN package	TBD
ANX7150SH	HDCP function enabled 64 pin, 8 x 8 mm, QFN package	TBD
ANX7150L	No HDCP function TBD 80 pin, 10 x 10 mm, LQFP package	July, 2009
ANX7150LH	HDCP function enabled TBD 80 pin, 10 x 10 mm, LQFP package	July, 2009
ANX7150B	No HDCP function 81 ball, 4.2 x 4.2 mm, BGA package	July, 2009
ANX7150BH	HDCP function enabled 81 ball, 4.2 x 4.2 mm, BGA package	July, 2009

7 Marking Information

..XXAA

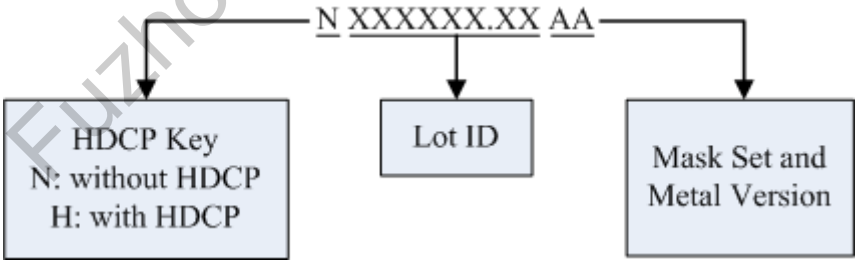
Line 1= Analogix Semiconductor logo

Line 2 = Marking name

Line 3 = Date Code+F, Location (CN)

Line 4 = N+Lot number+Rev i.e.: NXXXXXX.XXAA

Line 4:



Reference

Application Notes	Comments
Design SPEC of ANX7150	
DisplayPort™ Specification, Ver.1 Rev.1a	
VESA E-EDID STANDARD	
I2C SPECIFICATION	
IEC 60958	
IEC 61937	

Copyright ©2009 Analogix Semiconductor, Inc.
3211 Scott Blvd., Suite 102
Santa Clara, CA 95054, USA

(1) 408-988-8848

http://www.analogix.com/