

MAXIM

宽带、四路 DPDT 开关

MAX4760/MAX4761

概述

MAX4760/MAX4761(DPDT)模拟开关采用+1.8V至+5.5V单电源供电。这两款开关具有25pF的低电容特性,适合高速数据切换的应用。

MAX4760为4路双刀双掷(DPDT)开关,而MAX4761为8路单刀双掷开关(SPDT),它们均有8个导通电阻为3.5Ω的低电容开关,可用于切换音频和数据信号。MAX4760有4个逻辑输入端分别控制成对的开关,而MAX4761有1个逻辑控制输入端和1个可用来禁止开关的使能输入端(EN)。

MAX4760/MAX4761提供小型36引脚(6mm x 6mm)薄型QFN封装和36焊球(3mm x 3mm)晶片级封装(UCSP™)。

应用

- USB信号切换
- 音频信号切换
- 蜂窝电话
- PDA/手持式设备
- 笔记本电脑

特性

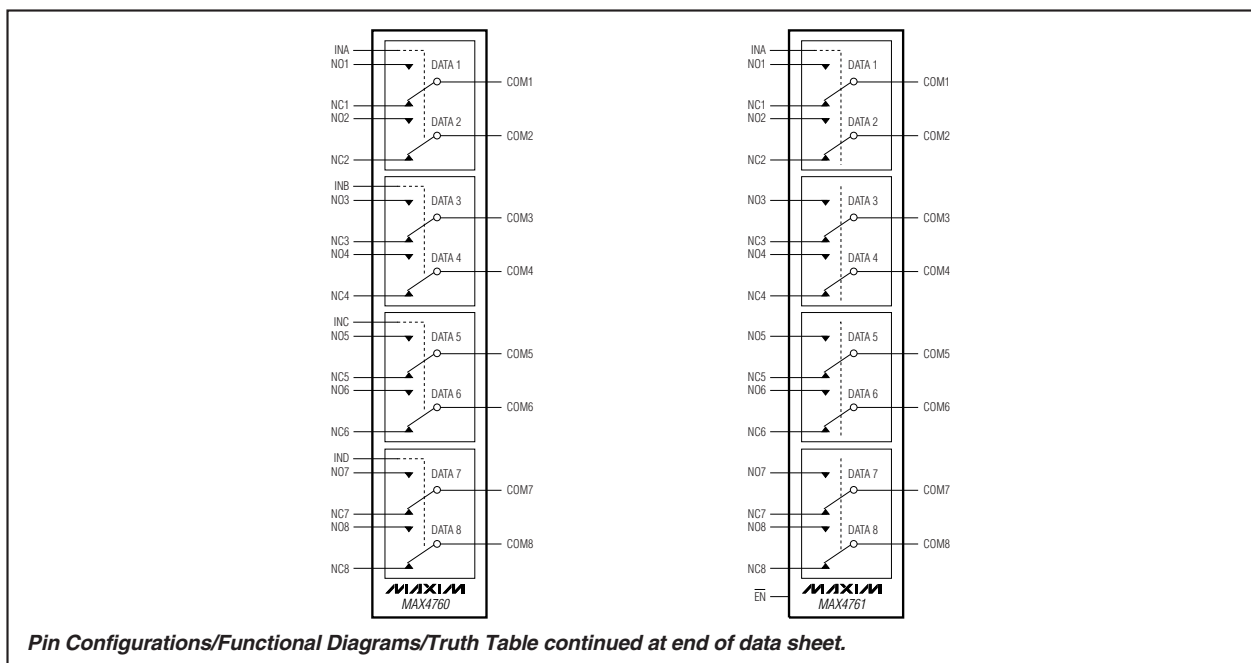
- ◆ 符合USB 1.1和USB 2.0(全速)信号开关规范
- ◆ 用于数据和音频信号切换
- ◆ 低电容(25pF)数据开关
- ◆ 偏斜小于0.2ns
- ◆ -3dB带宽:325MHz
- ◆ 0.2Ω通道间匹配度
- ◆ 0.8Ω导通电阻平坦度
- ◆ 满摆幅信号处理
- ◆ 0.03% THD
- ◆ +1.8V至+5.5V电源供电范围
- ◆ 微型36焊球UCSP(3mm x 3mm)封装
- ◆ 36引脚薄型QFN(6mm x 6mm)封装

订购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX4760EBX-T*	-40°C to +85°C	36 UCSP-36
MAX4760ETX*	-40°C to +85°C	36 Thin QFN (6mm x 6mm)
MAX4761EBX-T	-40°C to +85°C	36 UCSP-36
MAX4761ETX	-40°C to +85°C	36 Thin QFN (6mm x 6mm)

*Future product—contact factory for availability.

功能框图



UCSP是Maxim Integrated Products, Inc.的一个注册商标



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ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V+, IN_, EN_	-0.3V to +6V
COM_, NO_, NC_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current	
NO_, NC_, COM_	±100mA
Peak Current	
(pulsed at 1ms, 10% duty cycle)	±200mA
(pulsed at 1ms, 50% duty cycle)	±300mA
Continuous Power Dissipation (T _A = +70°C)	
36-Bump UCSP (derate 15.3mW/°C above +70°C)	1221mW
36-Pin Thin QFN (derate 26.3mW/°C above +70°C)	2105mW

ESD per Method 3015.7	±2kV
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Bump Temperature (soldering)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C

Note 1: Signals on NO_, NC_, COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{COM_} , V _{NO_} , V _{NC_}		T _{MIN} to T _{MAX}	0		V+	V
On-Resistance (Note 4)	R _{ON}	V+ = 2.7V, I _{COM_} = 10mA, V _{NC_} or V _{NO_} = 0V or V+	+25°C		2.0	3.5	Ω
			T _{MIN} to T _{MAX}			4	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR _{ON}	V+ = 2.7V, I _{COM_} = 10mA, V _{NO_} or V _{NC_} = 1.5V	+25°C		0.2	0.4	Ω
			T _{MIN} to T _{MAX}			0.55	
On-Resistance Flatness (Note 6)	R _{FLAT(ON)}	V+ = 2.7V, I _{COM_} = 10mA, V _{NC_} or V _{NO_} = 0V or V+	+25°C		0.8	1.5	Ω
			T _{MIN} to T _{MAX}			1.8	
NO_, NC_ Off-Leakage Current	I _{NO_(OFF)} , I _{NC_(OFF)}	V+ = 3.6V; V _{COM_} = 3.3V, 0.3V; V _{NO_} or V _{NC_} = 0.3V, 3.3V	+25°C	-5		+5	nA
			T _{MIN} to T _{MAX}	-25		+25	
COM_ Off-Leakage Current		V+ = 3.6V (MAX4761); V _{COM_} = 3.3V, 0.3V; V _{NO_} or V _{NC_} = 0.3V, 3.3V	+25°C	-5	0.01	+5	nA
			T _{MIN} to T _{MAX}	-25		+25	
COM_ On-Leakage Current	I _{COM_(ON)}	V+ = 3.6V; V _{COM_} = 3.3V, 0.3V; V _{NO_} or V _{NC_} = 3.3V, 0.3V or floating	+25°C	-5		+5	nA
			T _{MIN} to T _{MAX}	-25		+25	
DYNAMIC							
Turn-On Time	t _{ON}	V _{NO_} or V _{NC_} = 1.5V; R _L = 50Ω; C _L = 35pF, Figure 2	+25°C		45	140	ns
			T _{MIN} to T _{MAX}			150	
Turn-Off Time	t _{OFF}	V+ = 2.7V, V _{NO_} or V _{NC_} = 1.5V; R _L = 50Ω; C _L = 35pF, Figure 2	+25°C		25	50	ns
			T _{MIN} to T _{MAX}			60	

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ELECTRICAL CHARACTERISTICS (continued)(V+ = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
Break-Before-Make (Note 7)	t _{BBM}	V+ = 2.7V, V _{NO_} or V _{NC_} = 1.5V; R _L = 50Ω, C _L = 35pF, Figure 3	+25°C	15		ns	
			T _{MIN} to T _{MAX}	2			
Skew (Note 7)	t _{SKEW}	R _S = 39Ω, C _L = 50pF, Figure 4	+25°C	0.2	0.5	ns	
Charge Injection	Q	V _{GEN} = 0V, R _{GEN} = 0, C _L = 1.0nF, Figure 5	+25°C	15		pC	
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, C _L = 5pF, R _L = 50Ω	+25°C	320		MHz	
Off-Isolation (Note 8)	V _{ISO}	C _L = 5pF, R _L = 50Ω, V _{COM_} = 1V _{P-P} , f = 100kHz, Figure 6	+25°C	100		dB	
Crosstalk (Note 9)	V _{CT}	C _L = 5pF, R _L = 50Ω, V _{COM_} = 1V _{P-P} , f = 100kHz, Figure 6	+25°C	95		dB	
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, 1V _{P-P} , R _L = 600Ω	+25°C	0.03		%	
NO_, NC_ Off-Capacitance	C _{NO_(OFF)} , C _{NC_(OFF)}	V _{NO_} , V _{NC_} = GND, f = 1MHz, Figure 7	+25°C	25		pF	
COM_ On-Capacitance	C _{COM(ON)}	V _{NO_} , V _{NC_} = GND, f = 1MHz, Figure 7	+25°C	54		pF	
COM_ Off-Capacitance	C _{COM(OFF)}	V _{COM_} = GND, f = 1MHz (MAX4761), Figure 7	+25°C	25		pF	
DIGITAL I/O (IN_, EN)							
Input Logic High	V _{IH}	V+ = 2.7V to 3.6V	T _{MIN} to T _{MAX}	1.4		V	
		V+ = 3.6V to 5.5V	T _{MIN} to T _{MAX}	2.0			
Input Logic Low	V _{IL}	V+ = 2.7V to 3.6V	T _{MIN} to T _{MAX}	0.5		V	
		V+ = 3.6V to 5.5V	T _{MIN} to T _{MAX}	0.6			
Input Leakage Current	I _{IN}	V _{IN} = 0 or V+	T _{MIN} to T _{MAX}	1		μA	
POWER SUPPLY							
Power-Supply Range	V+		T _{MIN} to T _{MAX}	1.8	5.5	V	
Positive Supply Current	I+	V+ = 5.5V, V _{IN_} = 0V or V+	+25°C	0.01		μA	
			T _{MIN} to T _{MAX}	1.0			

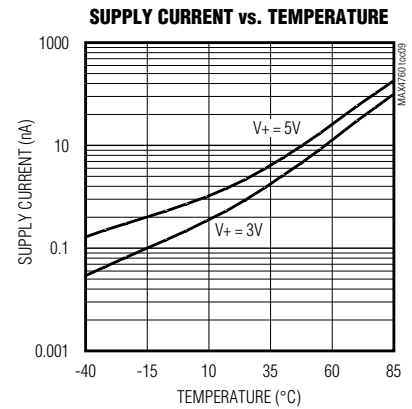
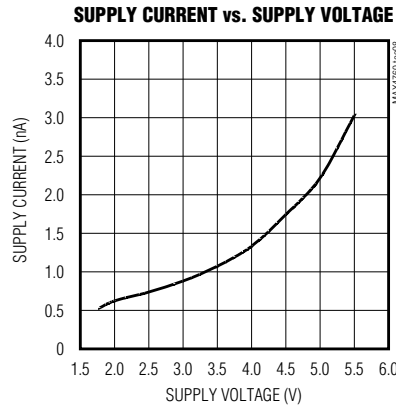
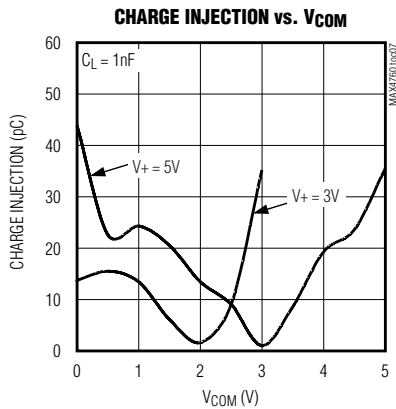
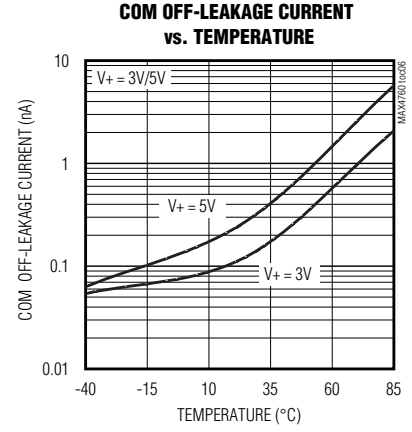
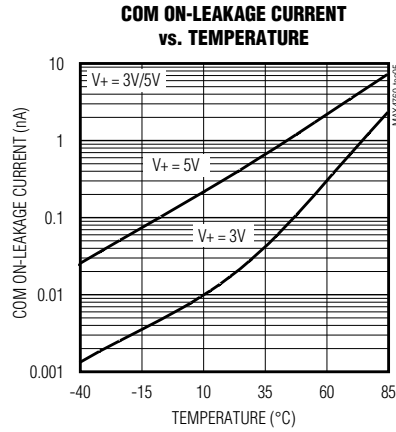
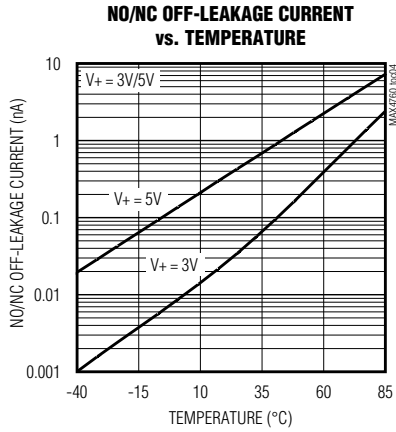
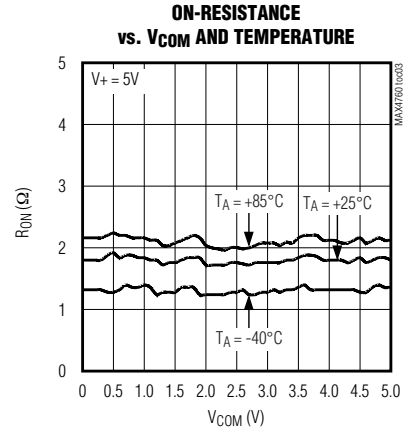
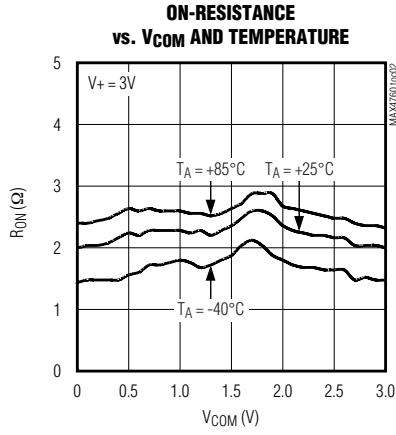
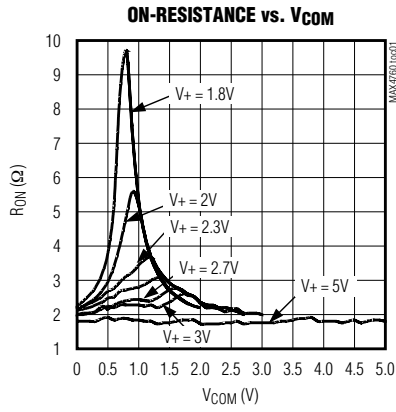
Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.**Note 3:** UCSP packages are 100% tested at +25°C and limits across the full temperature range are guaranteed by correlation and design. Thin QFN packages are 100% tested at +85°C and limits across the full temperature range are guaranteed by correlation and design.**Note 4:** R_{ON} and ΔR_{ON} matching specifications are guaranteed by design.**Note 5:** ΔR_{ON} = R_{ON(MAX)} - R_{ON(MIN)}.**Note 6:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.**Note 7:** Guaranteed by design, not production tested.**Note 8:** Off-isolation = 20log₁₀ [V_{COM_} / (V_{NO_} or V_{NC_})], V_{COM_} = output, V_{NO_} or V_{NC_} = input to off switch.**Note 9:** Between any two switches.

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典型工作特性

($V_+ = 3V$, $T_A = +25^\circ C$, unless otherwise noted.)

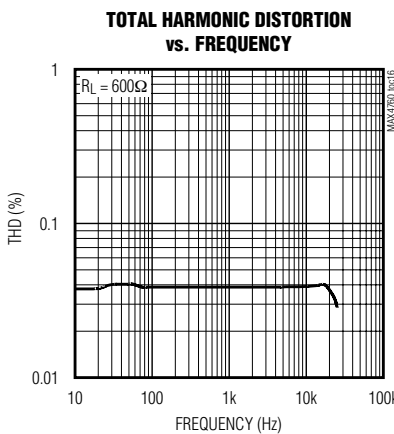
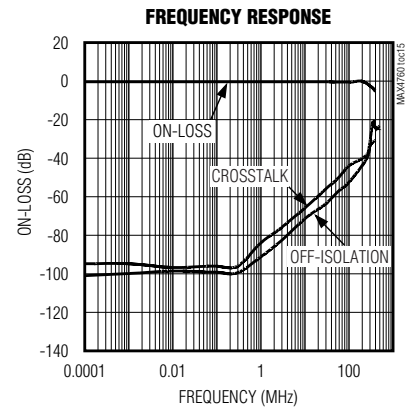
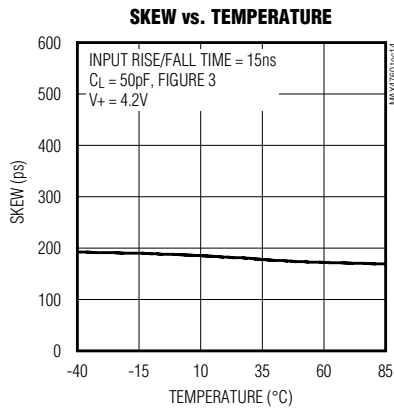
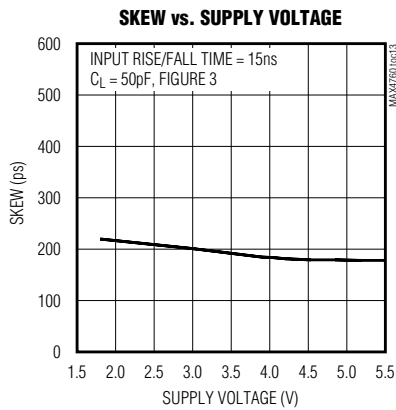
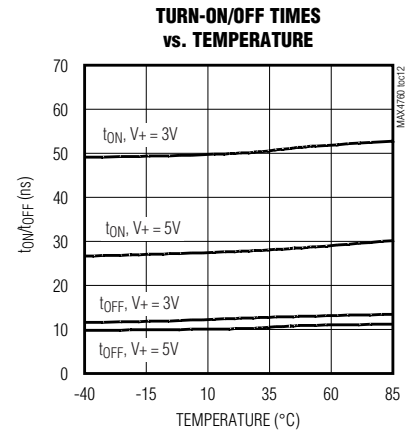
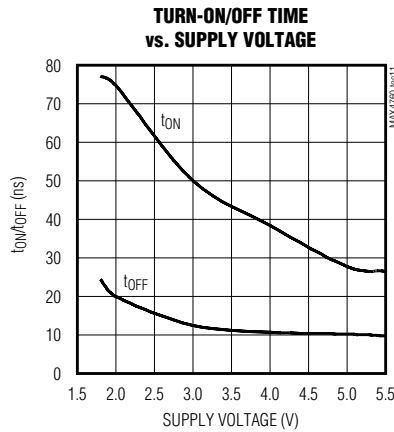
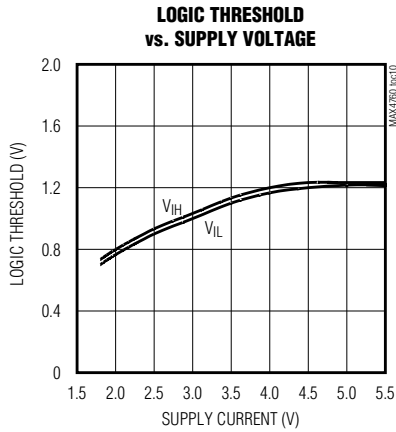
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典型工作特性(续)

($V_+ = 3V$, $T_A = +25^\circ C$, unless otherwise noted.)



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宽带、四路DPDT开关

引脚说明

MAX4760/MAX4761

引脚				名称	功能
MAX4760		MAX4761			
THIN QFN	UCSP	THIN QFN	UCSP		
1	A1	1	A1	NC1	模拟开关1, 常闭端1
2	B2	2	B2	COM2	模拟开关2, 公共端2
3	A2	3	A2	NC2	模拟开关2, 常闭端2
4	A3	4	A3	INA	MAX4760开关1和开关2的逻辑数控输入端。MAX4761所有开关的数控输入端。
5	C3, D4	5	C3, D4	V+	正电源输入
6	A4	—	—	INB	开关3和开关4的逻辑数控输入端
7	A5	7	A5	NC3	模拟开关3, 常闭端3
8	B5	8	B5	COM3	模拟开关3, 公共端3
9	A6	9	A6	NC4	模拟开关4, 常闭端4
10	B6	10	B6	COM4	模拟开关4, 公共端4
11, 14, 17, 29, 32, 35	—	6, 11, 14, 17, 24, 29, 32, 35	A4, F3	N.C.	未接, 内部无连接
12	C5	12	C5	NO3	模拟开关3, 常开端3
13	C6	13	C6	NO4	模拟开关4, 常开端4
15	D6	15	D6	NO8	模拟开关8, 常开端8
16	D5	16	D5	NO7	模拟开关7, 常开端7
18	E6	18	E6	COM8	模拟开关8, 公共端8
19	F6	19	F6	NC8	模拟开关8, 常闭端8
20	E5	20	E5	COM7	模拟开关7, 公共端7
21	F5	21	F5	NC7	模拟开关7, 常闭端7
22	F4	—	—	IND	开关7和开关8的逻辑数控输入端
23	C4, D3	23	C4, D3	GND	地
24	F3	—	—	INC	开关5和开关6的逻辑数控输入端
25	F2	25	F2	NC6	模拟开关6, 常闭端6
26	E2	26	E2	COM6	模拟开关6, 公共端6
27	F1	27	F1	NC5	模拟开关5, 常闭端5
28	E1	28	E1	COM5	模拟开关5, 公共端5
30	D2	30	D2	NO6	模拟开关6, 常开端6
31	D1	31	D1	NO5	模拟开关5, 常开端5
33	C1	33	C1	NO1	模拟开关1, 常开端1
34	C2	34	C2	NO2	模拟开关2, 常开端2
36	B1	36	B1	COM1	模拟开关1, 公共端1
—	—	22	F4	$\overline{\text{EN}}$	输出使能端, 低电平有效
EP	—	EP	—	EP	裸露焊盘, 接地

宽带、四路DPDT开关

详细说明

四路双刀双掷 (DPDT) 模拟开关 MAX4760 和八路单刀双掷 (SPDT) 模拟开关 MAX4761 采用 +1.8V 至 +5.5V 单电源供电，这些开关完全规范于 +3V 电源供电的应用。

MAX4760/MAX4761 导通电阻可保证 3.5Ω (最大)，可用于切换数据和音频信号。低至 25pF 的电容和 0.2ns 的偏斜变化非常适合数据交换应用。MAX4760 有 4 个逻辑输入端分别控制两个成对的开关，而 MAX4761 有 1 个逻辑输入端和 1 个可用来禁止开关的使能端 ($\overline{\text{EN}}$)。

应用信息

数控输入

无论采用何种电源电压，MAX4760/MAX4761 可接受高达 +5.5V 的逻辑输入，例如在 +3.3V 供电时， $\text{IN}_$ 可以低至 GND，也可以高至 +5.5V，保证了系统混合逻辑电平的兼容性。满摆幅驱动控制逻辑输入可将功耗降至最低。+3V 供电时，逻辑门限为 0.5V (低电平) 和 1.4V (高电平)。MAX4761 使能端 ($\overline{\text{EN}}$) 低电平有效， $\overline{\text{EN}}$ 端为高电平时， $\text{COM}_$ 为高阻状态。

模拟信号电平

处于供电电压范围内的模拟输入信号都可通过开关，且导通电阻变化极小 (见典型工作特性)，由于开关是双向的，所以 $\text{NO}_$ 、 $\text{NC}_$ 、 $\text{COM}_$ 可作为输入，也可作为输出。

电源旁路

电源旁路设计能够改善噪声容限，并防止开关噪声通过 $V+$ 电源传播到其他器件，对于多数应用来说，在 $V+$ 和 GND 之间并联一个 $0.1\mu\text{F}$ 的电容即可满足要求。

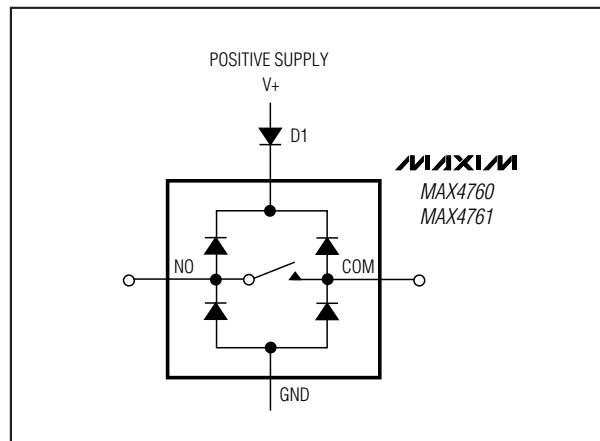


图1. 外接隔离二极管实现过压保护

供电顺序

CMOS 器件需要正确的供电顺序，总是在加载模拟信号前先加 V_{CC} ，特别是在输入信号没有限流的情况下。如果供电顺序不能保证，而且输入信号电流无法限制在 20mA 以内，则需要加一个小信号二极管 (见图 1)。增加了这个二极管，模拟信号范围要比 $V+$ 降低一个二极管压降 (0.7V)，并略微增大导通电阻。无论何时，最大供电电压都不能超过 +6V。

UCSP 应用信息

关于 UCSP 结构、尺寸、载带信息、印刷电路板技术、焊盘布局、推荐的回流温度特性，以及可靠性测试结果的最新应用数据，可从 Maxim 网站 www.maxim-ic.com/ucsp 下载 UCSP 应用笔记：“UCSP-A Wafer-Level Chip-Scale Package”。

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测试电路/时序图

MAX4760/MAX4761

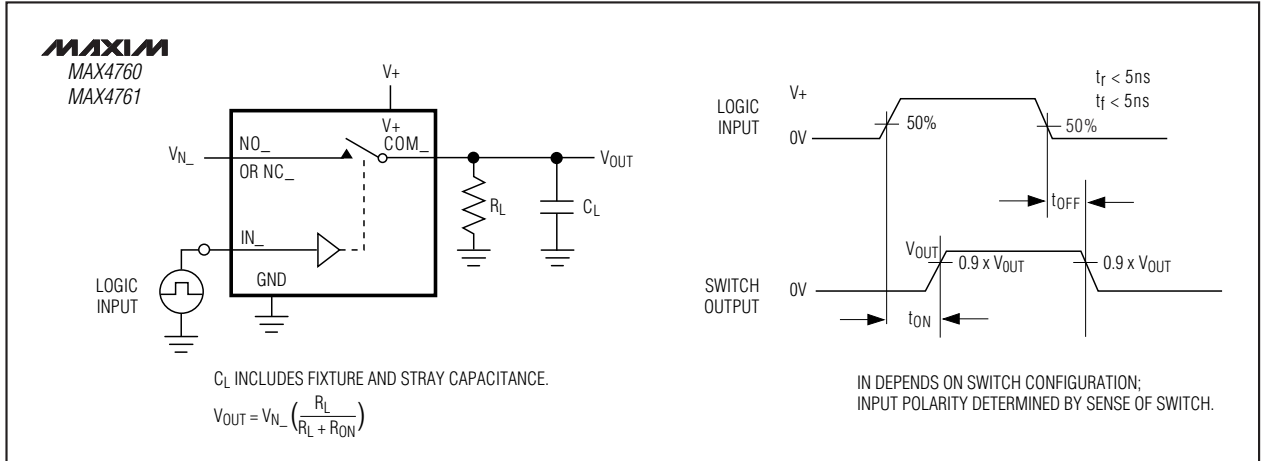


图2. 开关时间

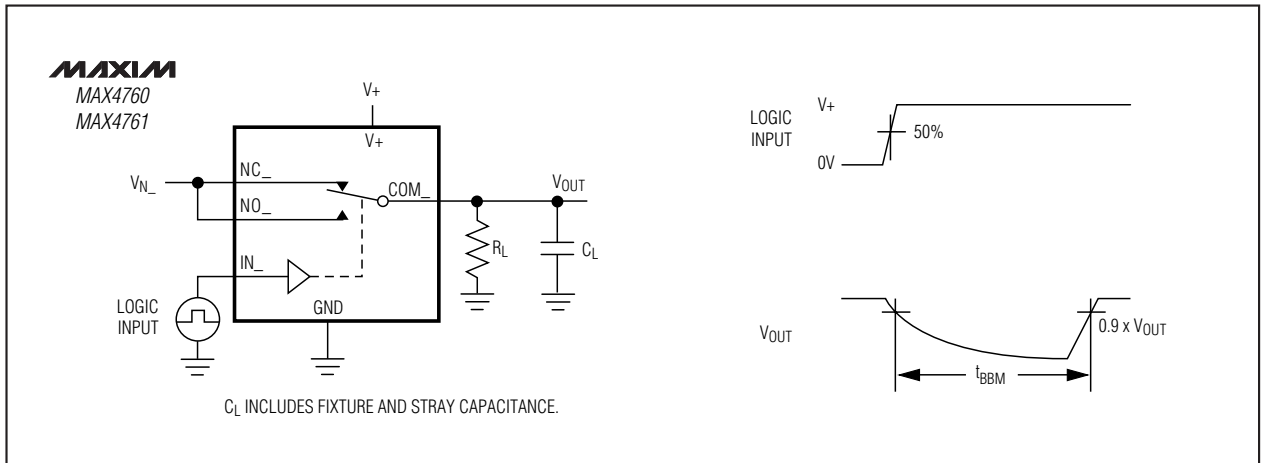


图3. 先断后合的间隔

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测试电路/时序图 (续)

MAX4760/MAX4761

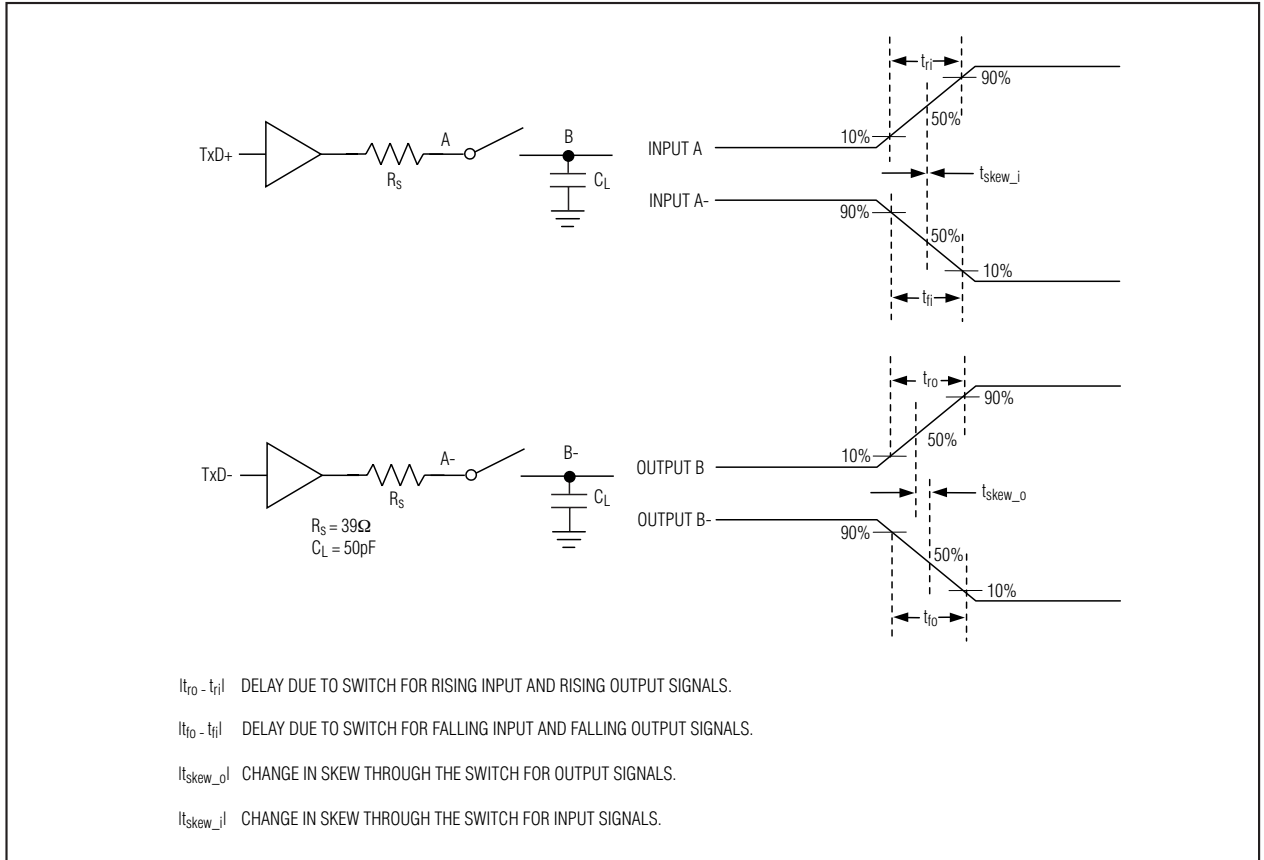


图4. 输入/输出偏差时序图

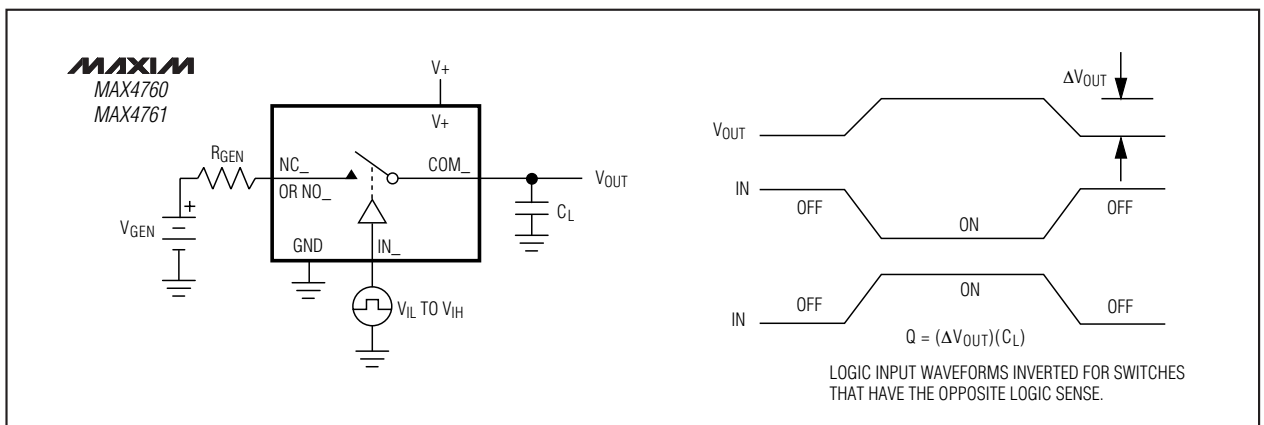


图5. 电荷注入

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测试电路/时序图 (续)

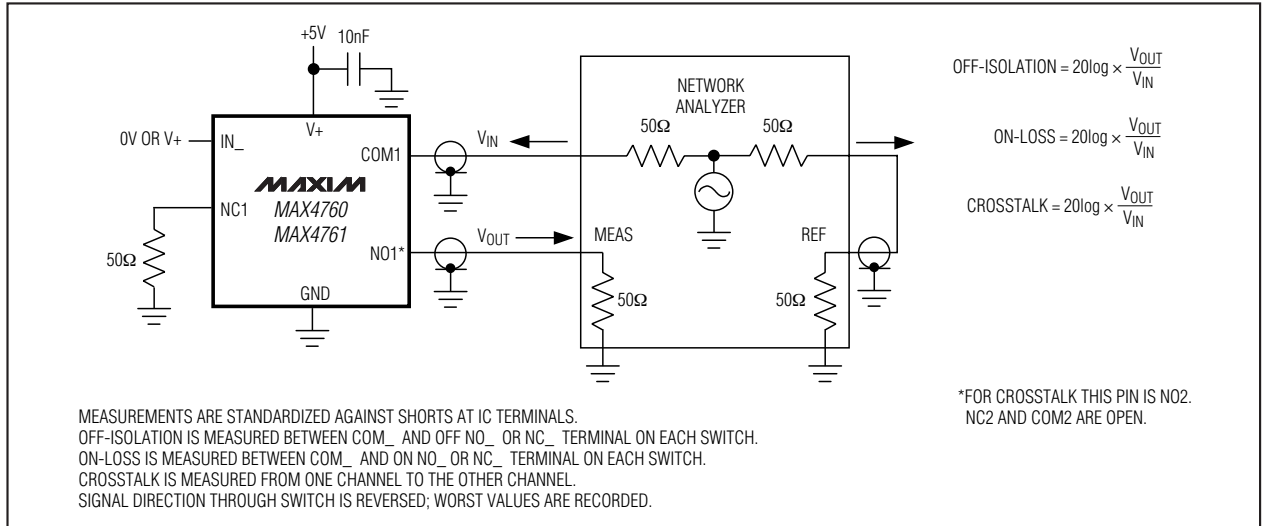


图6. 导通损耗，关断隔离和串扰

典型工作电路

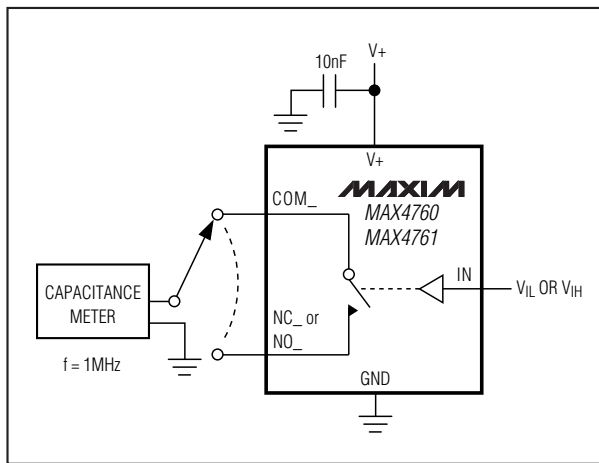
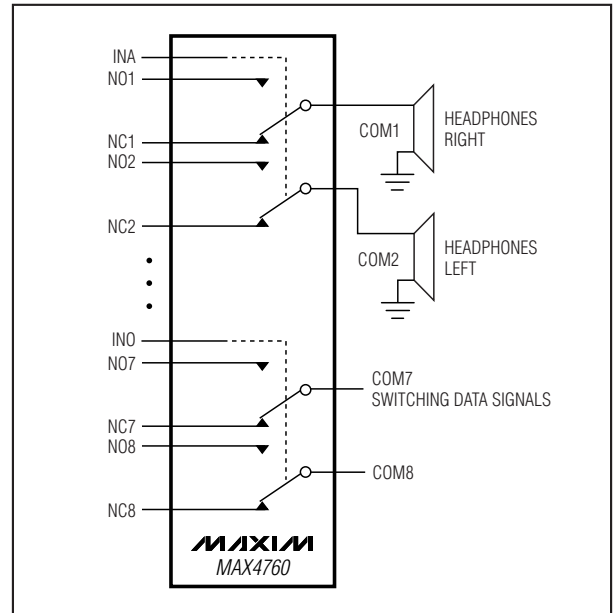


图7. 通道开/关电容



宽带、四路DPDT开关

引脚配置/真值表

MAX4760/MAX4761

TOP VIEW

MAXIM
MAX4760

(BUMP SIDE DOWN)

UCSP
MAX4760

INA	NO1/NO2	NC1/NC2
LOW	OFF	ON
HIGH	ON	OFF
INB	NO3/NO4	NC3/NC4
LOW	OFF	ON
HIGH	ON	OFF
INC	NO5/NO6	NC5/NC6
LOW	OFF	ON
HIGH	ON	OFF
IND	NO7/NO8	NC7/NC8
LOW	OFF	ON
HIGH	ON	OFF

THIN QFN

MAX4761

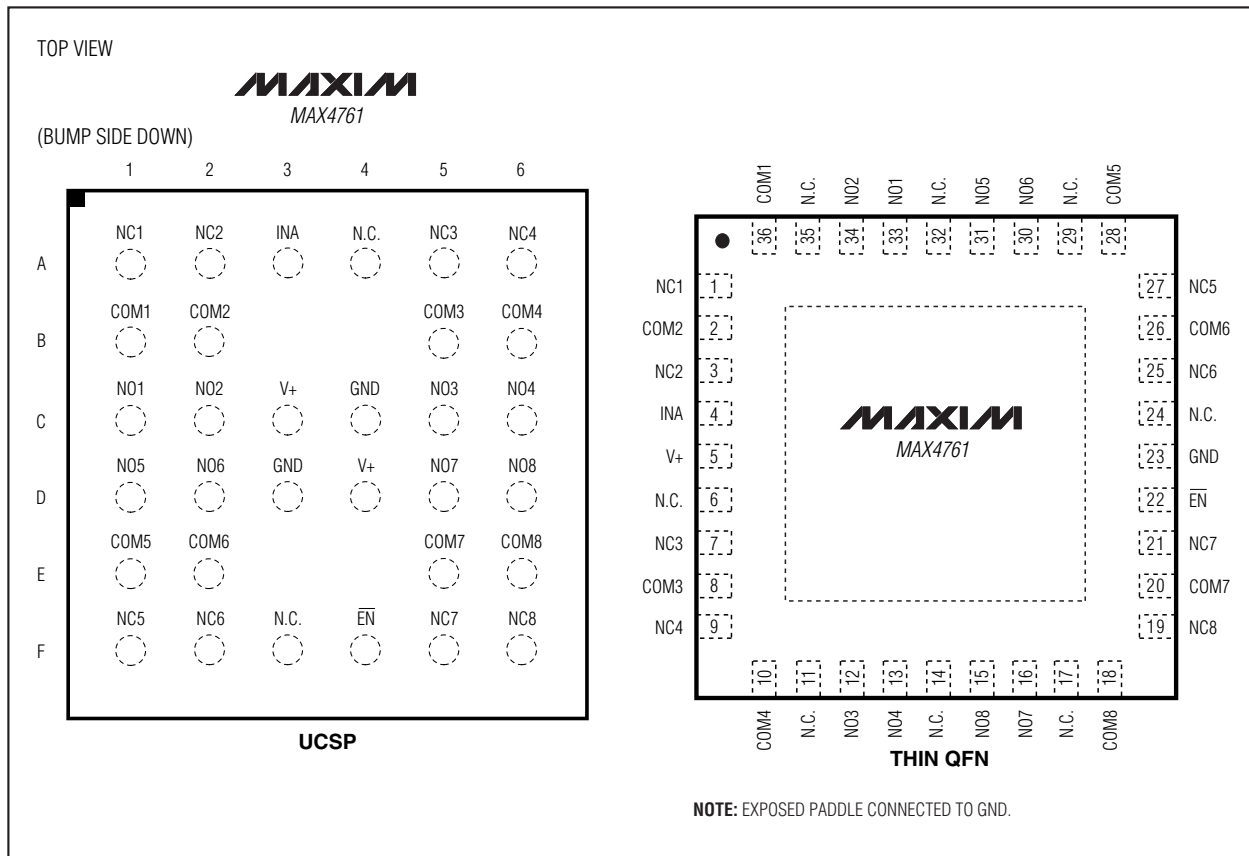
EN	INA	NO_	NC_
LOW	LOW	OFF	ON
LOW	HIGH	ON	OFF
HIGH	X	OFF	OFF
HIGH	X	OFF	OFF

NOTE: EXPOSED PADDLE CONNECTED TO GND OR FLOATING.

宽带、四路DPDT开关

引脚配置/真值表(续)

MAX4760/MAX4761



芯片信息

TRANSISTOR COUNT: 1432

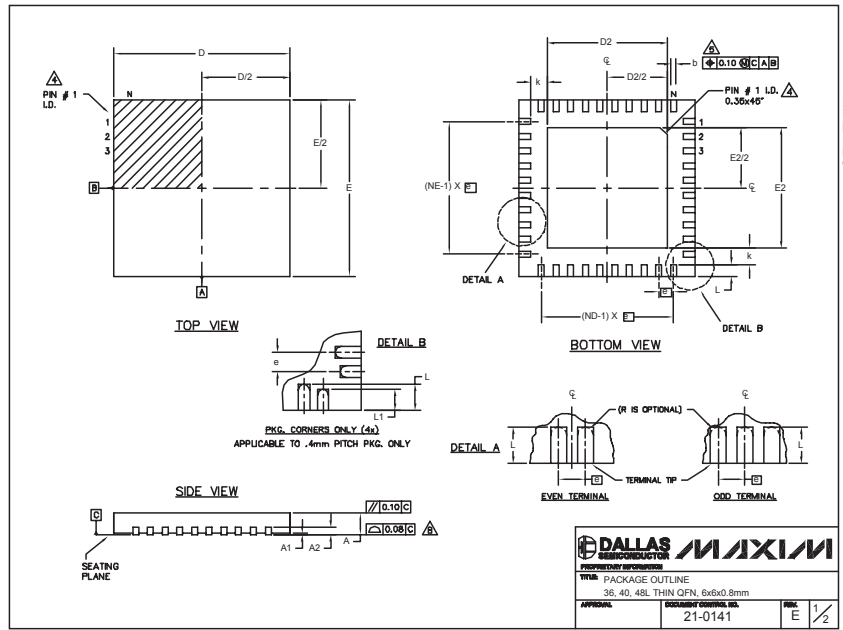
PROCESS: CMOS

宽带、四路DPDT开关

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 www.maxim-ic.com/packages。)

MAX4760/MAX4761



COMMON DIMENSIONS									
SYMBOL	36L 6x6			40L 6x6			48L 6x6		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	—	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	—	—	0.25	—	—	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	—	—	—	—	—	—	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WQAD-1			WQAD-2			—		

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
- WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR		MAXIM	
PRELIMINARY INFORMATION			
TITLE PACKAGE OUTLINE			
36, 40, 48L THIN QFN, 6x6x0.8mm			
APPROVAL	DESIGNER/DATE	REV	2/2
	21-0141	E	