低电压，单/双电源，8合1多路复用器和差分4合1多路复用器

概述

Intersil ISL43681 和 ISL43741 是精密，双向模拟开关，配有 8 通道和一个差分 4 通道多路复用器/多路信号分离器。它们工作在+2V 到+12V 的单电源，或±2V 到±6V 的电源下。它设有抑制管脚，可同时打开所有的信号通道。它还有一个锁存引脚，可锁住最后的开关地址。

接通电阻在±5V 电源下，为 39Ω；±3.3V 电源下，为 125Ω。每个开关都能够处理轨对轨模拟信号。漏放电流在+25℃下只有 0.1nA，在+85℃下为 2.5nA。

使用 3.3V 或+5V 单电源，或±5V 的双电源时，所有的数字输入有 0.8V 到 2.4V 的逻辑门限，以保证 TTL/CMOS 的逻辑兼容性。

ISL43681 是单一的 8 合 1 多路复用器，ISL43741 是差分 4 合 1 多路复用器。表 1 概括了它们的性能。

TABLE 1. FEATURES AT A GLANCE

CONFIGURATION	SINGLE 8:1 MUX, DIFF 4:1 MUX
±5V R_{ON}	39Ω
±5V t_{ON}/t_{OFF}	32ns/18ns
12V R_{ON}	32Ω
12V t_{ON}/t_{OFF}	23ns/15ns
5V R_{ON}	65Ω
5V t_{ON}/t_{OFF}	38ns/19ns
3.3V R_{ON}	125Ω
3.3V t_{ON}/t_{OFF}	70ns/32ns
Package	20 Ld 4x4 QFN

相关文献

- 技术摘要 TB363 “ 处理和加工对湿度敏感的表面安装器件（SMDs）的准则 ”
- 应用笔记 AN557 “ 模拟开关的建议测试过程 ”
- 应用笔记 AN520 “ CMOS 模拟多路复用器和开关；规格和应用注意事项 ”
- 应用笔记 AN1034 “ 模拟开关的多路复用器的应用 ”

特点

- 完全适用于 10%容差的 3.3V，5V，±5V 和 12V 的电源
- 最大接通电阻（R_{ON}），Vs=±4.5V…… 50Ω
- 最大接通电阻（R_{ON}），Vs=+3V…… 155Ω
- 与信道匹配的R_{ON}，Vs=±5V…… <2Ω
- 低电荷注入，Vs=±5V…… 1pC（最大）
- 单电源工作…… +2V 到+12V
- 双电源工作…… ±2V 到±6V
- 快速开关动作（Vs=+5V）

-- t_{ON}…… 38ns
-- t_{OFF}…… 19ns

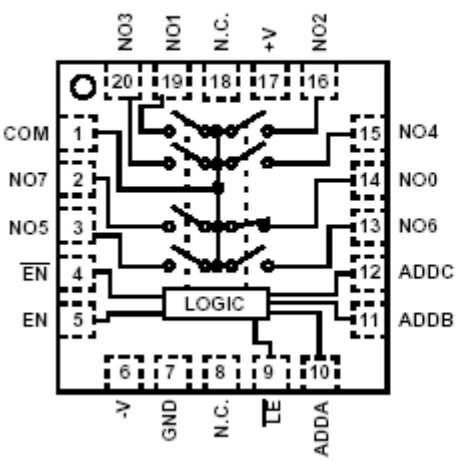
- 保证最大漏放电流…… 2.5nA
- 保证无断线
- 可兼容 TTL 和 CMOS
- 无铅封装

应用

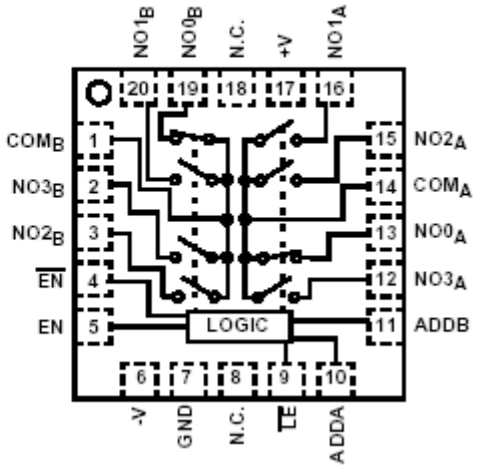
- 电池供电，手提和便携式设备
- 通信系统
  ——无线电收音机
  ——电信基础结构
  ——ADSL，VDSL 调制解调器
- 测试设备
  ——医学超声波
  ——心电图仪
  ——磁共振成像
  ——CT 和 PET 扫描器（MRI）
  ——自动测试设备
- 音频和视频转换
- 多种电路
  ——+3V/+5V 数模转换器和模数转换器
  ——抽样和保持电路
  ——运算放大器增益转换电路
  ——高频模拟开关
  ——高速多路复用
  ——积分复位电路

引脚图

ISL43681 (QFN)
TOP VIEW



ISL43741 (QFN)
TOP VIEW



真值表

ISL43681						
$\overline{LE}$	EN	$\overline{EN}$	ADDC	ADDB	ADDA	SWITCH ON
0	1	0	X	X	X	Last Switch Selected
X	0	X	X	X	X	NONE
X	X	1	X	X	X	NONE
1	1	0	0	0	0	NO0
1	1	0	0	0	1	NO1
1	1	0	0	1	0	NO2
1	1	0	0	1	1	NO3
1	1	0	1	0	0	NO4
1	1	0	1	0	1	NO5
1	1	0	1	1	0	NO6
1	1	0	1	1	1	NO7

注：逻辑“0”≤0.8V，逻辑“1”≥ 2.4V，V+在 2.7V 和 10V 之间。”X”=无影响。

ISL43741					
$\overline{LE}$	EN	$\overline{EN}$	ADDB	ADDA	SWITCH ON
0	1	0	X	X	Last Switch Selected
X	0	X	X	X	NONE
X	X	1	X	X	NONE
1	1	0	0	0	$NO0_A$, $NO0_B$
1	1	0	0	1	$NO1_A$, $NO1_B$
1	1	0	1	0	$NO2_A$, $NO2_B$
1	1	0	1	1	$NO3_A$, $NO3_B$

注：逻辑“0”≤0.8V，逻辑“1”≥ 2.4V，V+在 2.7V 和 10V 之间。”X”=无影响。

订购信息

PART NO. (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL43681IR (43681IR)	-40 to 85	20 Ld QFN	L20.4x4
ISL43681IRZ (43681IR) (Note)	-40 to 85	20 Ld QFN (Pb-free)	L20.4x4
ISL43741IR (43741IR)	-40 to 85	20 Ld QFN	L20.4x4
ISL43741IRZ (43741IR) (Note)	-40 to 85	20 Ld QFN (Pb-free)	L20.4x4

*Add "-T" suffix for tape and reel.

注：Intersil无铅产品采用特殊的无铅材料制成，模塑料／晶片的附属材料和100%无光泽锡盘引脚符合RoHS标准，兼容SnPb和无铅低温焊接操作。Intersil无铅产品在无铅峰值回流温度中属于MSL级别分类，完全满足和超过IPC/GEDEC JSTD-020的无铅要求。

引脚描述

引 脚	功 能
V+	正电源输入
V-	负电源输入。在单电源结构中接地。
GND	地
$\overline{EN}$	数字控制输入。正常工作情况下接地。接 V+时关闭所有开关。
EN	数字控制输入。正常工作情况下接 V+。接地时关闭所有开关。
$\overline{LE}$	数字控制输入。正常工作情况下接+V。接地时锁存最后的开关状态。
COM	模拟开关公共脚
NO	模拟开关常开脚
ADD	地址输入脚
N.C.	无内部连接

极限参数

V+到 V- …… -0.3V 至 15V
对 GND 的 V+ …… -0.3V 至 15V
对 GND 的 V- …… -15V 至 0.3V
输入电压
$\overline{LE}$, $\overline{EN}$,EN,NO,NC,ADD（注 1）…… -0.3 至（(V+）+0.3V）
输出电压
COM（注 1）…… -0.3 至（(V+）+0.3V）
连续电流（任一终端）…… ±30mA
峰值电流 NO，NC 或 COM
（脉冲 1ms，10%占空因数，最大值）…… ±100mA
静电释放额定值
HBM（每个 Mil-STD-883，依据 3015.7 标准）…… >2.5kV

工作条件

温度范围
ISL43681IR 和 ISL43741IR …… -40℃到 85℃

热信息

热阻（典型值，注 2） θ_{JA}(℃/W)
20 Ld 4×4 QFN 封装 …… 45
最大结温（塑料封装）…… 150℃
最大储存温度范围 …… -65℃到 150℃
最大引线温度（低温焊接 10s）…… 300℃
（仅限引线尖端）

注意：强度超出所列的极限参数可能导致器件的永久性损坏。这些仅仅是极限参数，并不意味着在极限条件下或在任何其它超出推荐工作条件所示参数的情况下器件能有效工作。

注：1. NO，NC，COM，ADD，EN， $\overline{EN}$ 或 $\overline{LE}$ 上超过 V+或 V- 的的信号受内部二极管的钳制。限制正向二极管电流为最大额定电流值。

2. θ_{JA}是在空气条件下，元件直接安装在高效导热性系数的测试板上测量得到的。详细内容参考技术摘要TB379。

电气指标：±5V 电源

测试条件： V_{SUPPLY}=±4.5V到±5.5V，GND =0V，V_{INH}=2.4V，V_{INL}=0.8V(注 3)，除非另有说明。

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) MIN	TYP	(NOTE 4) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	V-	-	V+	V
ON Resistance, R_{ON}	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = 3V (See Figure 6)	25	-	44	50	Ω
		Full	-	-	80	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = 3V (Note 5)	25	-	1.3	4	Ω
		Full	-	-	6	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = ±3V, 0V (Note 6)	25	-	7.5	9	Ω
		Full	-	-	12	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{EN}H}$, $I_{\overline{EN}L}$	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA
Input Current, I_{ENH}, $I_{\overline{LE}H}$	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-1.5	-	1.5	µA
Input Current, I_{ENL}, $I_{\overline{LE}L}$	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-4	-	4	µA

PARAMETER	TEST CONDITIONS		TEMP (°C)	(NOTE 4) MIN	TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS							
Enable Turn-ON Time, t_{ON}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)		25	-	35	50	ns
			Full	-	-	60	ns
Enable Turn-OFF Time, t_{OFF}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)		25	-	22	35	ns
			Full	-	-	40	ns
Address Transition Time, t_{TRANS}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)		25	-	43	60	ns
			Full	-	-	70	ns
Break-Before-Make Time, t_{BBM}	V_S = ±5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 3)		Full	2	7	-	ns
Latch Setup Time, t_S	(See Figure 4)		25	25	-	-	ns
			Full	35	-	-	ns
Latch Hold Time, t_H	(See Figure 4)		25	0	-	-	ns
			Full	0	-	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)		25	15	-	-	ns
			Full	25	-		ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)		25	-	0.3	1	pC
NO/NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)		25	-	3	-	pF
COM OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	ISL43681	25	-	21	-	pF
		ISL43741	25	-	12	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	ISL43681	25	-	26	-	pF
		ISL43741	25	-	18	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NOx} = $1V_{RMS}$ (See Figures 5, 7 and 20)		25	-	92	-	dB
Crosstalk, (Note 8) (ISL43741 only)			25	-	<-110	-	dB
All Hostile Crosstalk, (Note 8) (ISL43741 only)			25	-	-105	-	dB
POWER SUPPLY CHARACTERISTICS							
Power Supply Range			Full	±2	-	±6	V
Positive Supply Current, I+	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off		Full	-7	-	7	µA
Negative Supply Current, I-			Full	-1	-	1	µA

注：3．V_{IN}=使器件处于给定状态的输入逻辑电压

4．数据手册中使用了代数规则，负的最大值最小，正的最大值最大。

5．$\Delta R_{ON}=R_{ON}(MAX)-R_{ON}(MIN)$。

6．平直率定义为规定模拟信号范围内，导通电阻的最大和最小值之间的差值。

7．漏电参数在高温下测得，在 25℃下有相关保证。

8．在任意两个开关之间。

电气指标：+12V 电源

测试条件： V+=+10.8V到+13.2V，GND =0V，V_{INH}=4V，V_{INL}=0.8V(注 3)，除非另有说明。

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) MIN	TYP	(NOTE4) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V (See Figure 6)	25	-	37	45	Ω
		Full	-	-	55	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V (Note 5)	25	-	1.2	2	Ω
		Full	-	-	2	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V, 6V, 9V (Note 6)	25	-	5	7	Ω
		Full	-	-	7	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 13.2V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 12V, 1V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 13.2V, V_{COM} = 12V, 1V, V_{NO} or V_{NC} = 1V, 12V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 13.2V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 1V, 12V, or floating (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	3.7	3.3	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	2.7	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{ENH}}$, $I_{\overline{ENL}}$	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA
Input Current, I_{ENH}, $I_{\overline{LEH}}$	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+	Full	-1.5	-	1.5	µA
Input Current, I_{ENL}, $I_{\overline{LEL}}$	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+	Full	-4	-	4	µA
DYNAMIC CHARACTERISTICS						
Enable Turn-ON Time, t_{ON}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4 (See Figure 1)	25	-	24	40	ns
		Full	-	-	45	ns
Enable Turn-OFF Time, t_{OFF}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4 (See Figure 1)	25	-	15	30	ns
		Full	-	-	35	ns
Address Transition Time, t_{TRANS}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4 (See Figure 1)	25	-	27	50	ns
		Full	-	-	55	ns
Break-Before-Make Time Delay, t_D	V+ = 13.2V, R_L = 300Ω, C_L = 35pF, V_{NO} or V_{NC} = 10V, V_{IN} = 0 to 4 (See Figure 3)	Full	2	5	-	ns
Latch Setup Time, t_S	(See Figure 4)	25	25	-	-	ns
		Full	35	-	-	ns
Latch Hold Time, t_H	(See Figure 4)	25	0	-	-	ns
		Full	0	-	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)	25	15	-	-	ns
		Full	25	-	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	2.7	5	pC

PARAMETER	TEST CONDITIONS		TEMP (°C)	(NOTE 4) MIN	TYP	(NOTE4) MAX	UNITS
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz (See Figure 5,7 and 20)		25	-	92	-	dB
Crosstalk, (Note 8), (ISL43741 only)			25	-	<-110	-	dB
All Hostile Crosstalk, (Note 8) (ISL43741 only)			25	-	-105	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)		25	-	3	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	ISL43681	25	-	21	-	pF
		ISL43741	25	-	12	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	ISL43681	25	-	26	-	pF
		ISL43741	25	-	18	-	pF
POWER SUPPLY CHARACTERISTICS							
Power Supply Range			Full	2	-	12	V
Positive Supply Current, I+	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+, all channels on or off		Full	-7	-	7	µA
Positive Supply Current, I-			Full	-1	-	1	µA

电气指标：5V 电源

测试条件： V+=+4.5V到+5.5V，GND =0V，V_{INH}=2.4V，V_{INL}=0.8V(注 3)，除非另有说明。

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V (See Figure 6)	25	-	81	90	Ω
		Full	-	-	120	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V (Note 5)	25	-	2.2	4	Ω
		Full	-	-	6	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V (Note 6)	25	-	11.5	17	Ω
		Full	-	-	24	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} or V_{NC} = 4.5V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{ENH}}$, $I_{\overline{ENL}}$	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA
Input Current, I_{ENH}, $I_{\overline{EH}}$	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-1.5	-	1.5	µA
Input Current, I_{ENL}, $I_{\overline{EL}}$	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-4	-	4	µA

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
DYNAMIC CHARACTERISTICS						
Enable Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	43	60	ns
		Full	-	-	70	ns
Enable Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	20	35	ns
		Full	-	-	40	ns
Address Transition Time, t_{TRANS}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	51	70	ns
		Full	-	-	85	ns
Break-Before-Make Time, t_{BBM}	V+ = 5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 3)	Full	2	9	-	ns
Latch Setup Time, t_S	(See Figure 4)	25	25	-	-	ns
		Full	35	-	-	ns
Latch Hold Time, t_H	(See Figure 4)	25	0	-	-	ns
		Full	0	-	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)	25	15	-	-	ns
		Full	25	-	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	0.6	1.5	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NOx} = $1V_{RMS}$ (See Figures 5, 7 and 20)	25	-	92	-	dB
Crosstalk, (Note 8), (ISL43741 only)		25	-	<-110	-	dB
All Hostile Crosstalk, (Note 8), (ISL43741 only)		25	-	-105	1.5	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	2	-	12	V
Positive Supply Current, I+	V+ = 5.5V, V- = 0V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	Full	-7	-	7	µA
Positive Supply Current, I-		Full	-1	-	1	µA

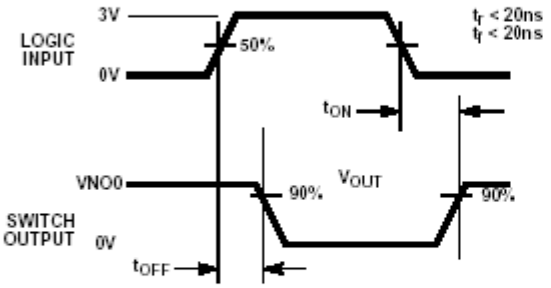
电气指标：3.3V 电源

测试条件： V+=+3.0V到+3.6V，V- =GND =0V，V_{INH}=2.4V，V_{INL}=0.8V(注 3)，除非另有说明。

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V (See Figure 6)	25	-	135	155	Ω
		Full	-	-	200	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V (Note 5)	25	-	3.4	8	Ω
		Full	-	-	10	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 0.5V, 1V, 2V (Note 6)	25	-	34	40	Ω
		Full	-	-	50	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.6V, V_{COM} = 0V, 4.5V, V_{NO} or V_{NC} = 3V, 1V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA

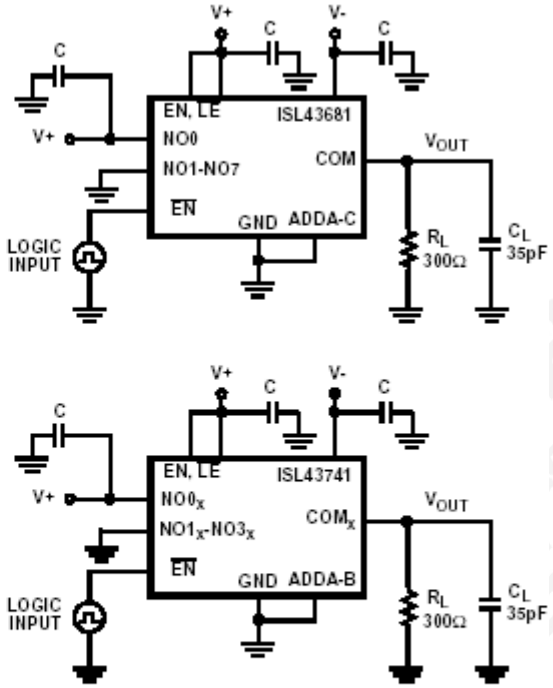
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 0V, 4.5V, V_{NO} or V_{NC} = 3V, 1V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.6V, V_{COM} = V_{NO} or V_{NC} = 3V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{EN}H}$, $I_{\overline{EN}L}$	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA
Input Current, I_{ENH}, $I_{\overline{LE}H}$	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+	Full	-1.5	-	1.5	µA
Input Current, I_{ENL}, $I_{\overline{LE}L}$	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+	Full	-4	-	4	µA
DYNAMIC CHARACTERISTICS						
Enable Turn-ON Time, t_{ON}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	82	100	ns
		Full	-	-	120	ns
Enable Turn-OFF Time, t_{OFF}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	37	50	ns
		Full	-	-	60	ns
Address Transition Time, t_{TRANS}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	96	120	ns
		Full	-	-	145	ns
Break-Before-Make Time, t_{BBM}	V+ = 3.6V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 3)	Full	3	13	-	ns
Latch Setup Time, t_S	(See Figure 4)	25	50	-	-	ns
		Full	60	-	-	ns
Latch Hold Time, t_H	(See Figure 4)	25	0	-	-	ns
		Full	0	-	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)	25	30	-	-	ns
		Full	40	-	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	0.3	1	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NO} or V_{NC} = $1V_{RMS}$ (See Figures 5, 7 and 20)	25	-	92	-	dB
Crosstalk, (Note 8), (ISL43741 only)		25	-	<-110	-	dB
All Hostile Crosstalk, (Note 8), (ISL43741 only)		25	-	-105	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	2	-	12	V
Positive Supply Current, I+	V+ = 3.6V, V- = 0V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	Full	-7	-	7	µA
Positive Supply Current, I-		Full	-1	-	1	µA

测试电路和波形图



Logic input waveform is inverted for switches that have the opposite logic sense.

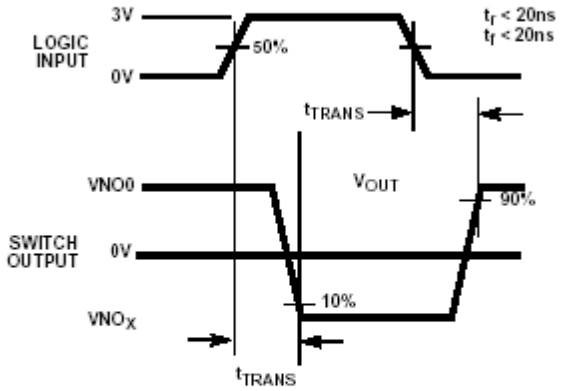
FIGURE 1A. ENABLE t_{ON}/t_{OFF} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

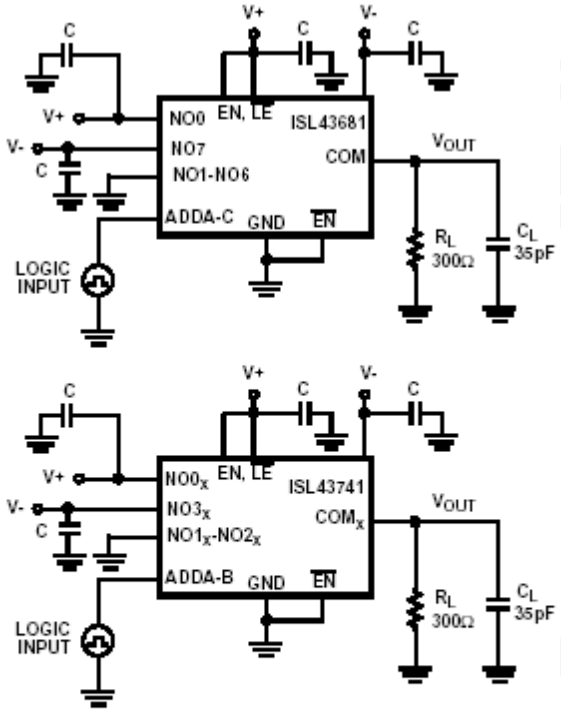
$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. ENABLE t_{ON}/t_{OFF} TEST CIRCUIT



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS t_{TRANS} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1D. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

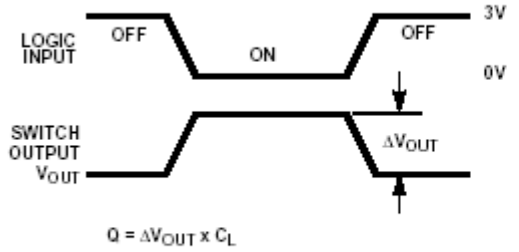
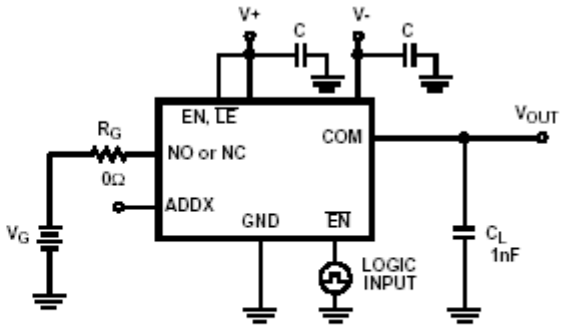


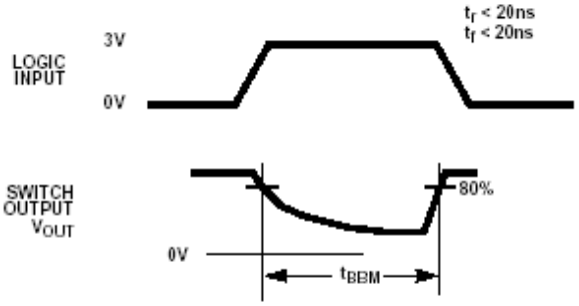
FIGURE 2A. Q MEASUREMENT POINTS

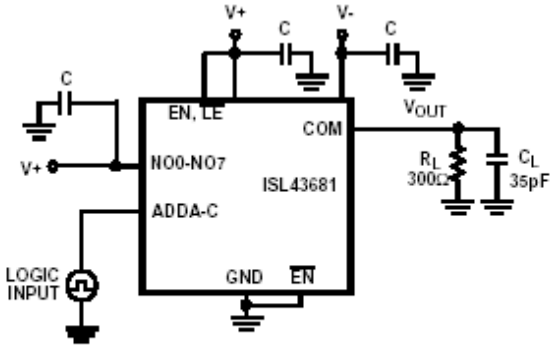


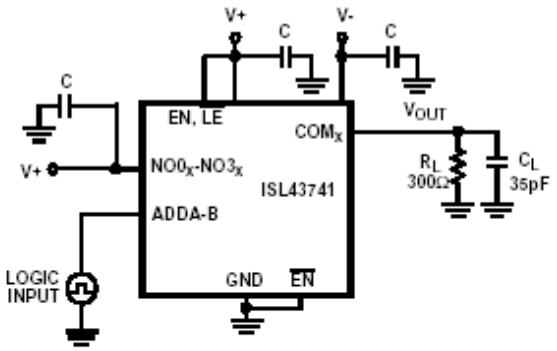
Repeat test for other switches.

FIGURE 2B. Q TEST CIRCUIT

FIGURE 2. CHARGE INJECTION





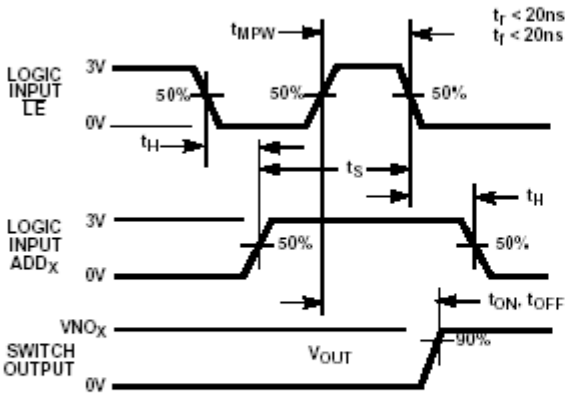


Repeat test for other switches. C_L includes fixture and stray capacitance.

FIGURE 3A. t_{BBM} MEASUREMENT POINTS

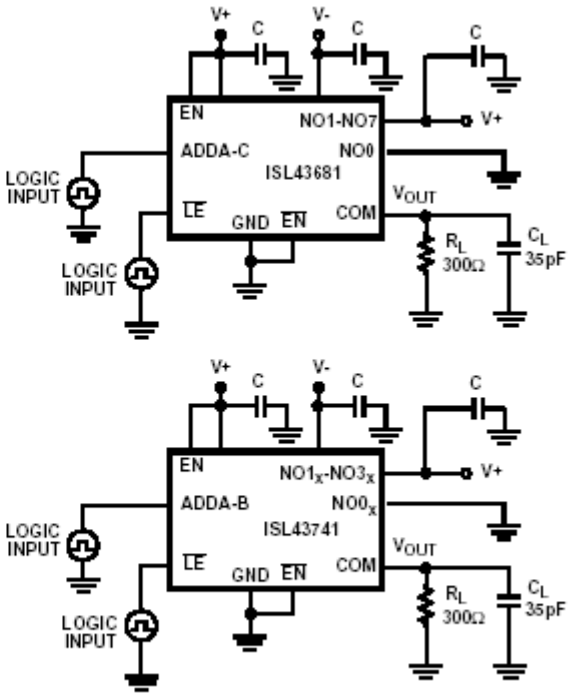
FIGURE 3B. t_{BBM} TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 4A. LATCH t_S, t_H, t_{MPW} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 4B. LATCH t_S, t_H, t_{MPW} TEST CIRCUIT

FIGURE 4. LATCH SETUP AND HOLD TIMES

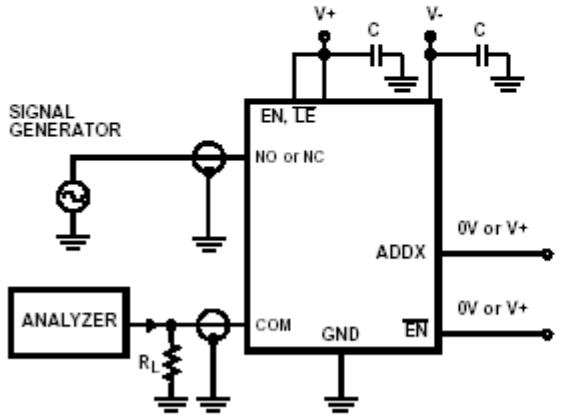


FIGURE 5. OFF ISOLATION TEST CIRCUIT

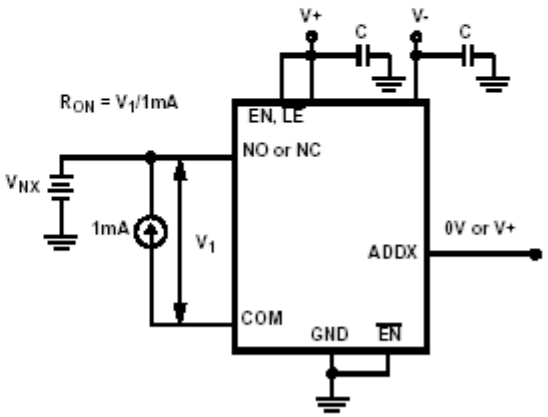


FIGURE 6. R_{ON} TEST CIRCUIT

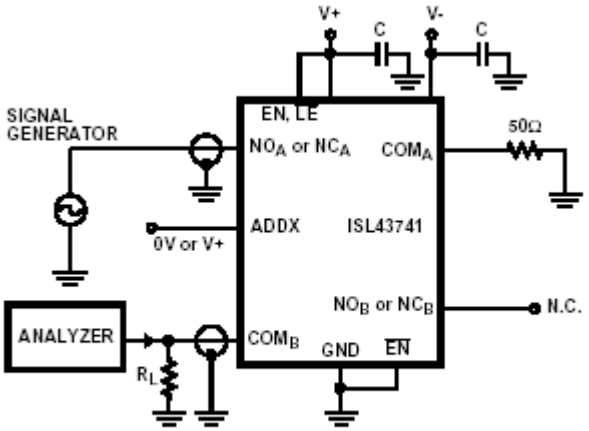


FIGURE 7. CROSSTALK TEST CIRCUIT

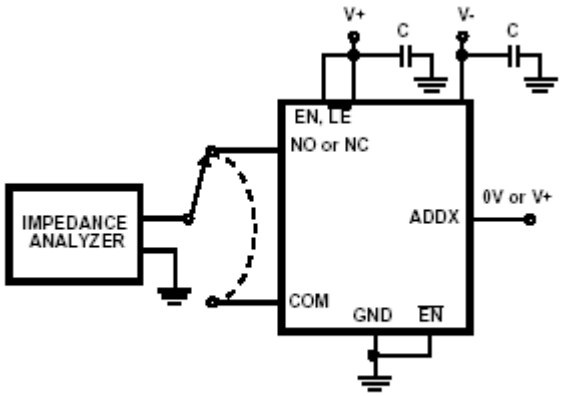


FIGURE 8. CAPACITANCE TEST CIRCUIT

详细描述

ISL43681 和ISL43741 多路复用器工作在±2V到±6V的双极性电源或 2V到 12V的单电源下，提供精确的开关能力，双 5V电源下有低的导通电阻（39Ω）和高速的工作能力（t_{ON}=38ns，t_{OFF}=19ns）。

它们设有抑制管脚，可同时打开所有的信号通道。它们还有一个锁存引脚，可锁住最后的开关地址。

器件特别适合于使用±5V电源供电的应用。±5V电源下，它的性能（R_{ON}，漏放电流，电荷注入等）是同系列中最好的。

它的宽的带宽，非常高的断开隔离和串话干扰抑制同样有利于高频应用。

电源排序和过压保护

和所有的 CMOS 器件一样，适当的电源排序可保护器件免受可能使集成电路受到永久性损坏的过量输入电流的冲击。接 V+和接 V-的所有的输入/输出管脚都包括 ESD 保护二极管（见图 9）。为防止二极管的正向偏置，在输入信号前必须加上 V+和 V- ，且输入信号电压必须保持在 V+和 V- 之间。如果这些条件不能满足，可采用下面两种保护方法之一。

通过在输入端串联一个 1kΩ的电阻，逻辑输入很容易被保护（见图 9）。电阻限制了输入电流，使其保持在引起永久破坏的门限之下，次微安输入电流在正常工作下产生一个无关紧要的电压降。

该方法不适用于信号通道的输入。给开关输入增加一个串联电阻阻扰了使用一个低R_{ON}开关的目的，因此，两个小信号二极管能够与电源脚串联来为所有管脚提供过压保护（见图 9）。这些附加的二极管使模拟信号的值限制在比V+低 1V，比V- 高 1V之间。低漏放电流性能不受这一方法的影响，但开关电阻可能会增加，特别是在低电源电压下。

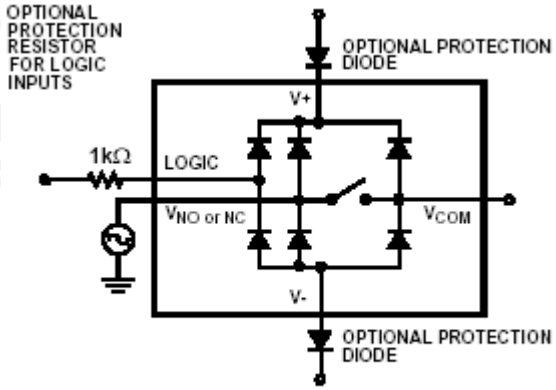


FIGURE 9. INPUT OVERVOLTAGE PROTECTION

电源供电考虑

ISL43681 和 ISL43741 的结构是典型的 CMOS 模拟开关，因为它们有 3 个电源引脚：V+,V-,和 GND。V+和 V- 驱动内部 CMOS 开关，决定它们的模拟电压极限值，因此模拟信号通路和 GND 之间没有连接。不象用 13V 最大电源电压供电的其他模拟开关，ISL43681 和 ISL43741 的 15V 最大电源电压为 10%容差的 12V 电源（±6V 或 12V 单电源）提供足够的空间，也为过冲和噪声尖峰信号提供足够的空间。

工作在双极性或单电源下，该开关系列的性能都很好。所需的最小电源电压为 2V 或±2V。还必须注意的是输入信号范围，开关次数和较低电源电压下的导通电阻降低。详细内容请参考电气指标表和典型性能曲线图。

V+和 GND 也为内部逻辑（因此设置数字开关点）和电平移位器供电。电平移位器将输入逻辑电平转换为开关的 V+和 V- 信号，来驱动模拟开关门接线端。

逻辑电平门限

V+和GND为内部逻辑级供电，因此V- 对逻辑门限没有影响。该开关系列在V+电压范围为 2.7V到 10V的情况下，可兼容TTL电平（0.8V和 2.4V）。12V下，V_{IH}电平约为 3.3V。这仍比CMOS保证高电平输出所需的最小电平 4V低，但噪声边缘减少了。为了达到 12V电源的最好结果，使用一个逻辑系列提供高于 4V的V_{OH}。

当数字输入电压不在供电范围内时，数字输入段拉制电源电流。使数字输入信号由 GND 变为 V+有快速的转换时间，可以最大限度地减少功耗。

高频性能

在 50Ω系统中，信号响应一般是平展的，即使超过 100MHz（参见图 18 和 19）。图 18 和 19 也说明了对变化的模拟信号电平，频率响应是一致的。

断开开关的操作相当于一个电容，可通过高频而减少衰减，使信号馈通，由开关的输入变为它的输出。断开隔离是馈通的电阻，串话干扰指示了从一个开关到另一开关的馈通量。图 20 列出了这一系列提供的高断开隔离和串话干扰抑制。10MHz 下，在 50Ω系统中断开隔离约为 55dB，频率每增加 10，断开隔离就减少大约 20dB。由于分压器对开关断开电阻和负载电阻的作用，更高的负载电阻会减少断开隔离和串话干扰抑制。

漏电考虑

反向 ESD 保护二极管在每个模拟信号管脚和 V+与 V- 之间是内部相连的。如果任何一个模拟信号超过 V+或 V- ，其中一个二极管就会导通。

实际上，所有的模拟漏放电流都由对 V+或 V- 的 ESD 二极管产生。尽管在给出信号脚上的 ESD 二极管是相同的且很好地平衡，但它们的反向偏置是不同的。每个的偏置由 V+或 V- ，和模拟信号决定。这意味着它们的漏放随信号的变化而变化。两个二极管中对 V+和 V- 管脚漏放的不同，构成了模拟信号通路漏放电流。所有的模拟漏放电流在每个管脚和其中一个电源终端中流动，不到达其他开关终端。这就是为什么给出开关的两边都可以显示相同或相反极性的漏放电流的原因。模拟信号通路和 GND 之间没有连接。

典型性能曲线图

T_A=25℃，除非另有说明。

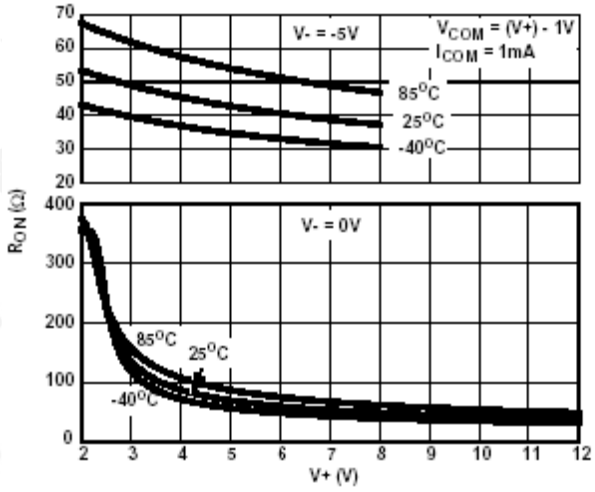


FIGURE 10. ON RESISTANCE vs SUPPLY VOLTAGE

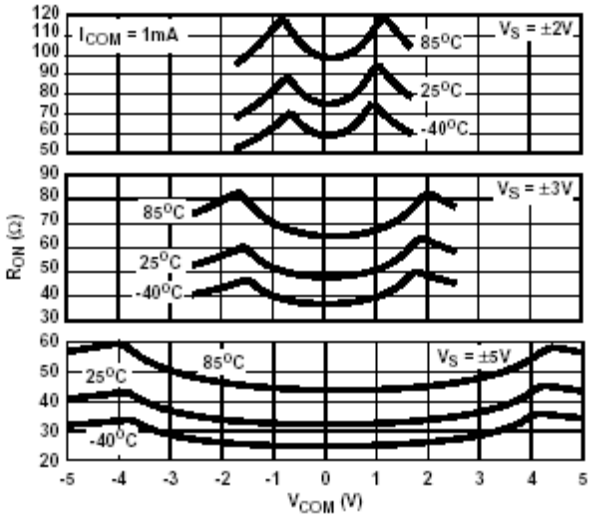


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

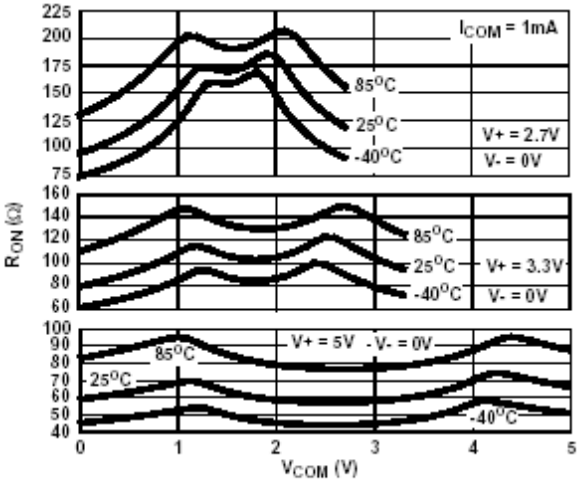


FIGURE 12. ON RESISTANCE vs SWITCH VOLTAGE

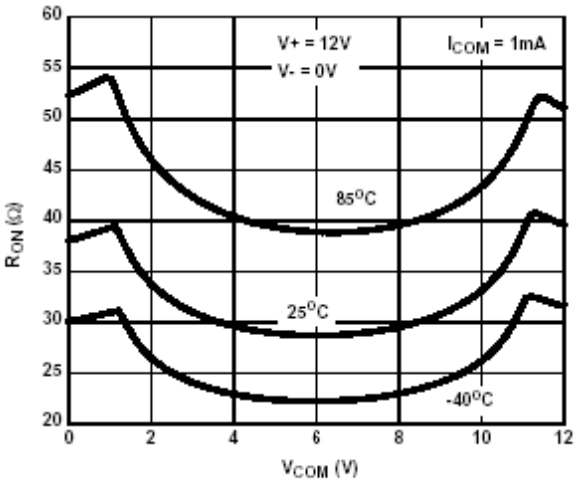


FIGURE 13. ON RESISTANCE vs SWITCH VOLTAGE

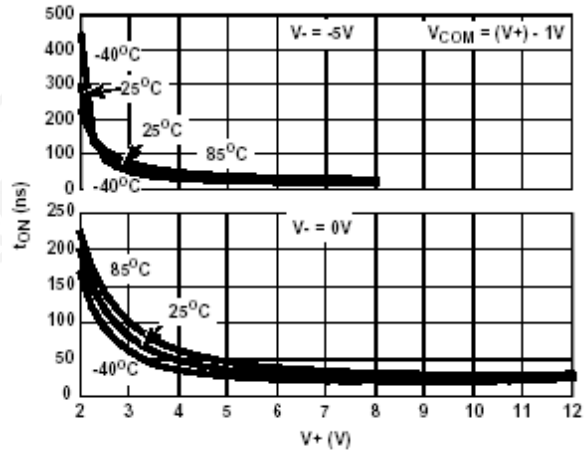


FIGURE 14. ENABLE TURN - ON TIME vs SUPPLY VOLTAGE

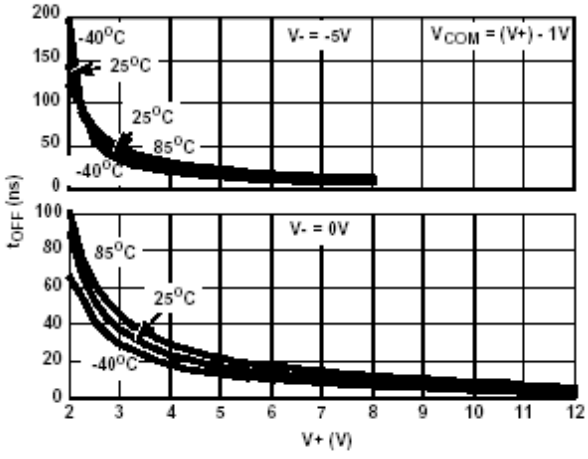


FIGURE 15. ENABLE TURN - OFF TIME vs SUPPLY VOLTAGE

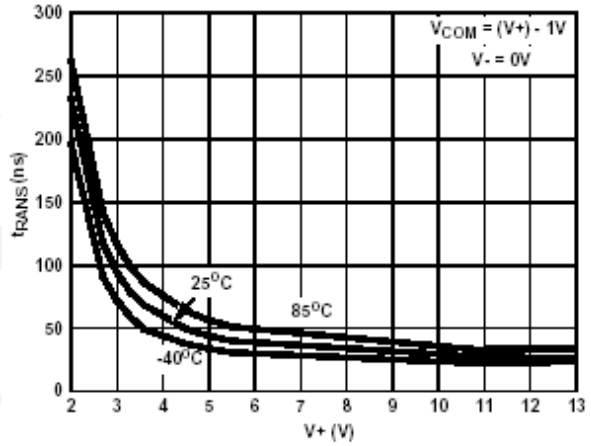


FIGURE 16. ADDRESS TRANS TIME vs SINGLE SUPPLY VOLTAGE

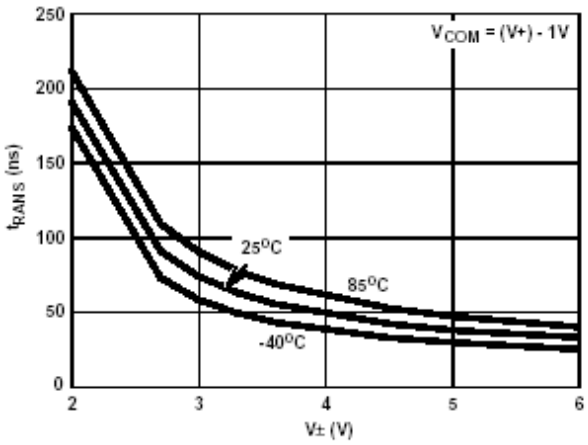


FIGURE 17. ADDRESS TRANS TIME vs DUAL SUPPLY VOLTAGE

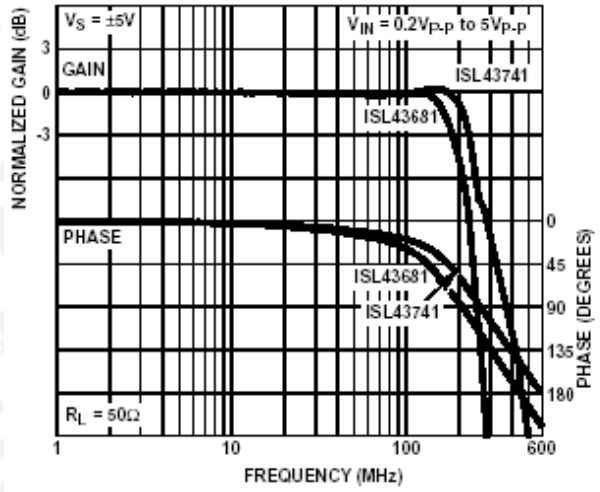


FIGURE 18. FREQUENCY RESPONSE

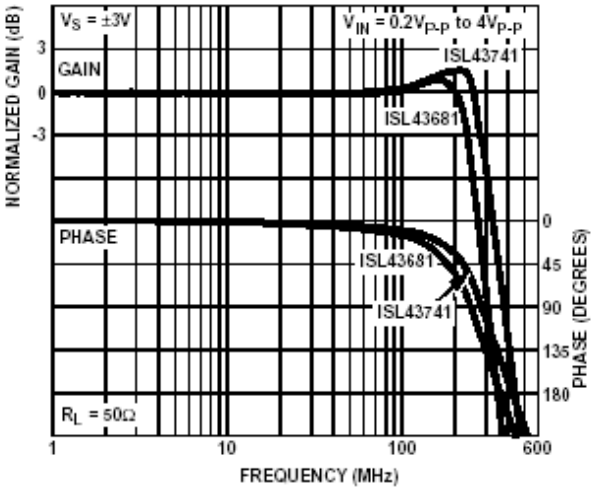


FIGURE 19. FREQUENCY RESPONSE

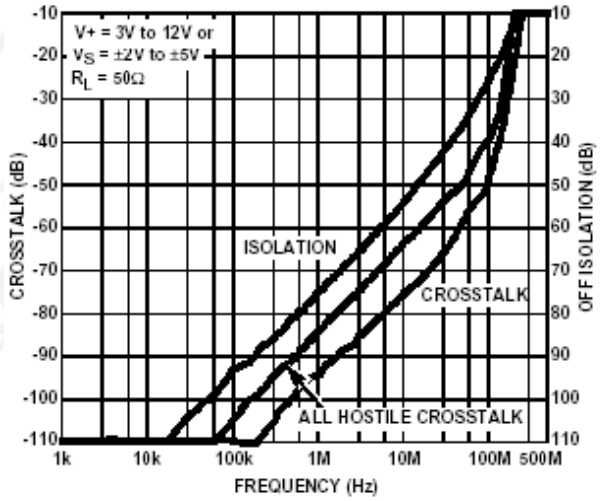


FIGURE 20. CROSSTALK AND OFF ISOLATION

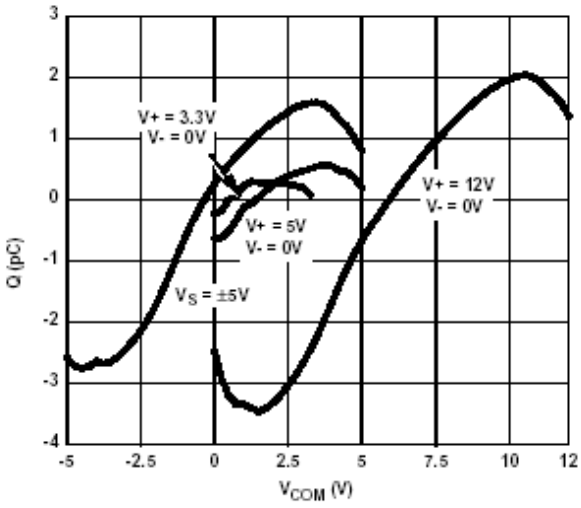
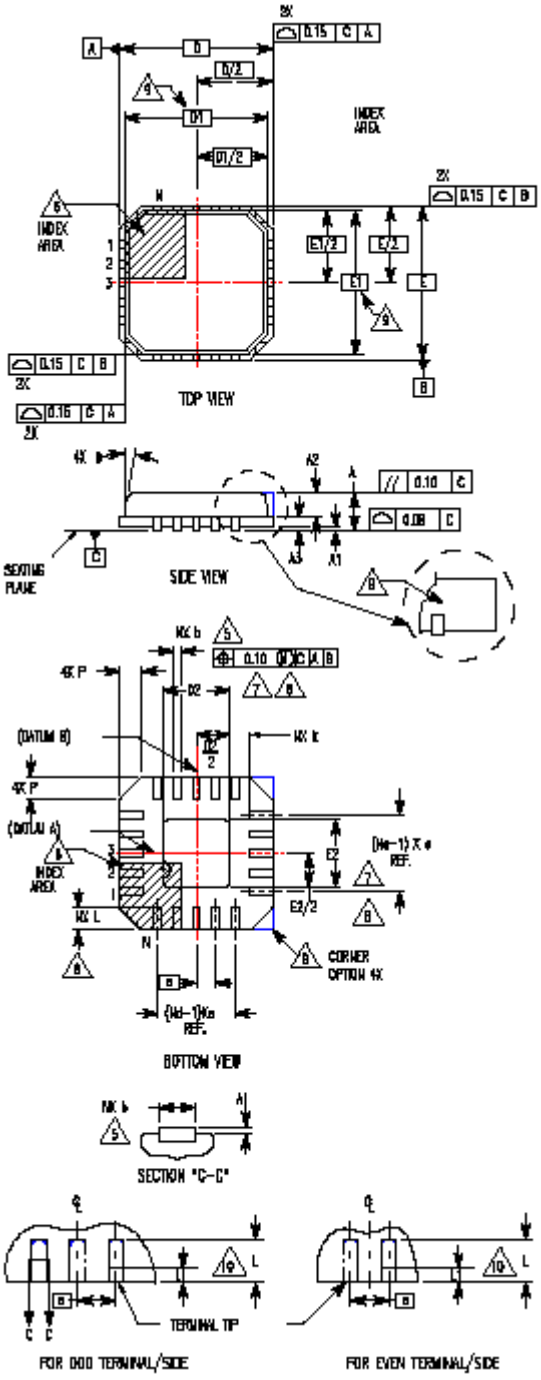


FIGURE 21. CHARGE INJECTION vs SWITCH VOLTAGE

模片特性
基片电位（加电）：GND
工艺：硅门控 CMOS

晶体管数量：
ISL43681：193
ISL43741：193

四芯线平板无铅塑料封装（QFN）
微引线构造塑料封装（MLFP）



L20.4x4
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
(COMPLIANT TO JEDEC MO-220VGGD-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		20		2
Nd		5		3
Ne	5	5		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

声明：本资料仅供参考。如有不同之处，请以相应英文资料为准。

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