FAIRCHILD SEMICONDUCTOR™

July 1988
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# 100350
# Low Power Hex D-Type Latch

## General Description

The 100350 contains six D-type latches with true and complement outputs, a pair of common Enables ($\overline{E}_a$ and $\overline{E}_b$), and a common Master Reset (MR). A Q output follows its D input when both $\overline{E}_a$ and $\overline{E}_b$ are LOW. When either $\overline{E}_a$ or $\overline{E}_b$ (or both) are HIGH, a latch stores the last valid data present on its D input before $\overline{E}_a$ or $\overline{E}_b$ went HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

## Features

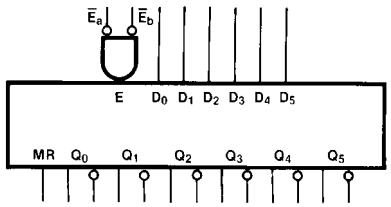
- 20% power reduction of the 100150
- 2000V ESD protection
- Pin/function compatible with 100150
- Voltage compensated operating range = –4.2V to –5.7V

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 100350PC | N24E | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide |
| 100350QC | V28A | 28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square |

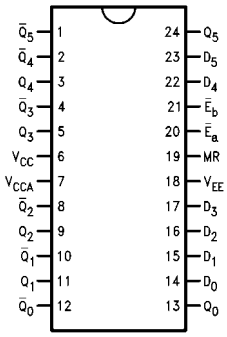
Devises also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbol

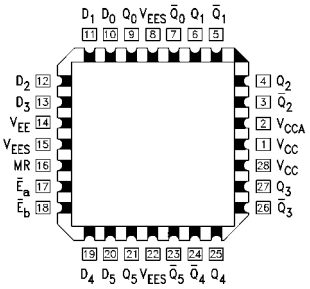



## Connection Diagrams

**24-Pin DIP**




**28-Pin PLCC**




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $D_0$–$D_5$ | Data Inputs |
| $\overline{E}_a$, $\overline{E}_b$ | Common Enable Inputs (Active LOW) |
| MR | Asynchronous Master Reset Input |
| $Q_0$–$Q_5$ | Data Outputs |
| $\overline{Q}_0$–$\overline{Q}_5$ | Complementary Data Outputs |

## Truth Tables

(Each Latch)

**Latch Operation**

| Inputs | | | | Outputs |
|---|---|---|---|---|
| $D_n$ | $\overline{E}_a$ | $\overline{E}_b$ | MR | $Q_n$ |
| L | L | L | L | L |
| H | L | L | L | H |
| X | H | X | L | Latched (Note 1) |
| X | X | H | L | Latched (Note 1) |

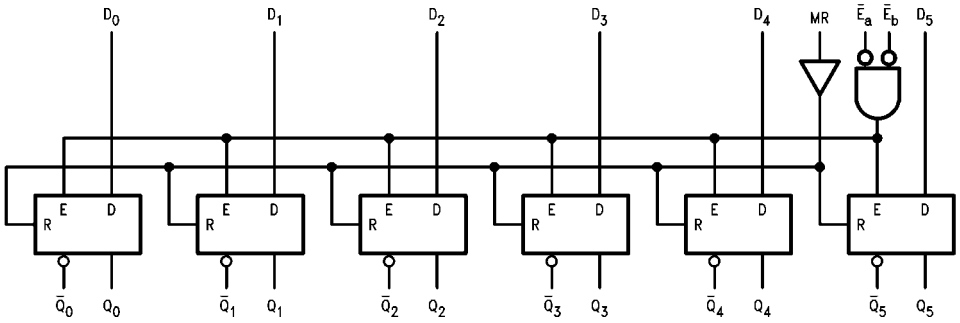
**Asynchronous Operation**

| Inputs | | | | Outputs |
|---|---|---|---|---|
| $D_n$ | $\overline{E}_a$ | $\overline{E}_b$ | MR | $Q_n$ |
| X | X | X | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

**Note 1:** Retains data present before $\overline{E}$ positive transition

## Logic Diagram



## Absolute Maximum Ratings(Note 2)

Above which the useful life may be impaired.

| | |
|---|---|
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Maximum Junction Temperature ($T_J$) | +150°C |
| $V_{EE}$ Pin Potential to Ground Pin | −7.0V to +0.5V |
| Input Voltage (DC) | $V_{EE}$ to +0.5V |
| Output Current (DC Output HIGH) | −50 mA |
| ESD (Note 3) | ≥2000V |

## Recommended Operating Conditions

| | |
|---|---|
| Case Temperature ($T_C$) | 0°C to +85°C |
| Supply Voltage ($V_{EE}$) | −5.7V to −4.2V |

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** ESD testing conforms to MIL-STD-883, Method 3015.

## DC Electrical Characteristics (Note 4)

$V_{EE}$ = −4.5V to −5.7V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1025 | −955 | −870 | mV | $V_{IN}$ = $V_{IH\ (Max)}$ | Loading with |
| $V_{OL}$ | Output LOW Voltage | −1830 | −1705 | −1620 | | or $V_{IL\ (Min)}$ | 50Ω to −2.0V |
| $V_{OHC}$ | Output HIGH Voltage | −1035 | | | mV | $V_{IN}$ = $V_{IH\ (Min)}$ | Loading with |
| $V_{OLC}$ | Output LOW Voltage | | | −1610 | | or $V_{IL\ (Max)}$ | 50Ω to −2.0V |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −870 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1830 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | µA | $V_{IN}$ = $V_{IL\ (Min)}$ | |
| $I_{IH}$ | Input HIGH Current MR | | | 240 | µA | $V_{IN}$ = $V_{IH\ (Max)}$ | |
| | $D_n$ | | | 240 | | | |
| | $\overline{E}_a$, $\overline{E}_b$ | | | 240 | | | |
| $I_{EE}$ | Power Supply Current | | | | mA | Inputs Open | |
| | | −89 | | −44 | | $V_{EE}$ = −4.2V to −4.8V | |
| | | −93 | | −44 | | $V_{EE}$ = −4.2V to −5.7V | |

**Note 4:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## DIP AC Electrical Characteristics

$V_{EE}$ = −4.2V to −5.7V, $V_{CC}$ = $V_{CCA}$ = GND

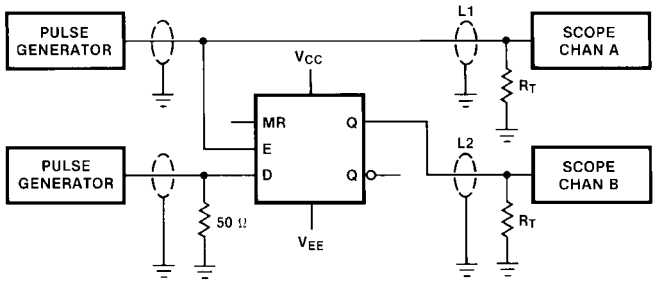
| Symbol | Parameter | $T_C$ = 0°C | | $T_C$ = +25°C | | $T_C$ = +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay | | | | | | | | |
| $t_{PHL}$ | $D_n$ to Output | 0.50 | 1.40 | 0.50 | 1.40 | 0.50 | 1.50 | ns | |
| | (Transparent Mode) | | | | | | | | Figures 1, 2 |
| $t_{PLH}$ | Propagation Delay | 0.75 | 1.85 | 0.75 | 1.85 | 0.75 | 2.05 | ns | |
| $t_{PHL}$ | $\overline{E}_a$, $\overline{E}_b$ to Output | | | | | | | | |
| $t_{PLH}$ | Propagation Delay | 0.90 | 2.10 | 0.90 | 2.10 | 0.90 | 2.10 | ns | Figures 1, 3 |
| $t_{PHL}$ | MR to Output | | | | | | | | |
| $t_{TLH}$ | Transition Time | 0.35 | 1.30 | 0.35 | 1.30 | 0.35 | 1.30 | ns | Figures 1, 2 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | | | | | | | | |
| $t_S$ | Setup Time | | | | | | | | |
| | $D_0$–$D_5$ | 1.00 | | 1.00 | | 1.00 | | ns | Figures 3, 4 |
| | MR (Release Time) | 1.60 | | 1.60 | | 1.60 | | | |
| $t_H$ | Hold Time, $D_0$–$D_5$ | 0.40 | | 0.40 | | 0.40 | | ns | Figure 4 |
| $t_{PW}$(L) | Pulse Width LOW | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 |
| | $\overline{E}_a$, $\overline{E}_b$ | | | | | | | | |
| $t_{PW}$(H) | Pulse Width HIGH, MR | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

## PLCC AC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, $V_{CC}$ = $V_{CCA}$ = GND

| Symbol | Parameter | $T_C$ = 0°C | | $T_C$ = +25°C | | $T_C$ = +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$D_n$ to Output<br>(Transparent Mode) | 0.50 | 1.20 | 0.50 | 1.20 | 0.50 | 1.30 | ns | Figures 1, 2 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{E}_a$, $\overline{E}_b$ to Output | 0.75 | 1.65 | 0.75 | 1.65 | 0.75 | 1.85 | ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>MR to Output | 0.90 | 1.90 | 0.90 | 1.90 | 0.90 | 1.90 | ns | Figures 1, 3 |
| $t_{TLH}$<br>$t_{THL}$ | Transition Time<br>20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | Figures 1, 2 |
| $t_S$ | Setup Time<br>$D_0$–$D_5$<br>MR (Release Time) | 0.90<br>1.50 | | 0.90<br>1.50 | | 0.90<br>1.50 | | ns | Figures 3, 4 |
| $t_H$ | Hold Time, $D_0$–$D_5$ | 0.30 | | 0.30 | | 0.30 | | ns | Figure 4 |
| $t_{PW}$(L) | Pulse Width LOW<br>$\overline{E}_a$, $\overline{E}_b$ | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 |
| $t_{PW}$(H) | Pulse Width HIGH, MR | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

## Test Circuit




**Note:**

- $V_{CC}$, $V_{CCA}$ = +2V, $V_{EE}$ = –2.5V
- L1 and L2 = equal length 50Ω impedance lines
- $R_T$ = 50Ω terminator internal to scope
- Decoupling 0.1 µF from GND to $V_{CC}$ and $V_{EE}$
- All unused outputs are loaded with 50Ω to GND
- $C_L$ = Fixture and stray capacitance ≤ 3 pF

**FIGURE 1. AC Test Circuit**

## Switching Waveforms

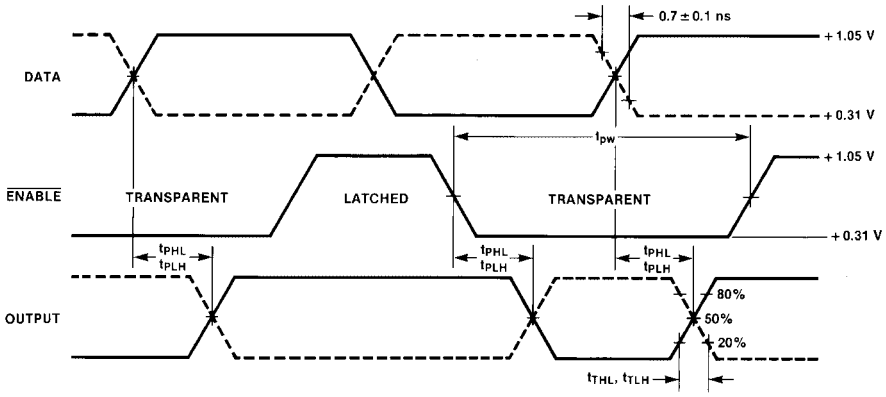



**FIGURE 2. Enable Timing**

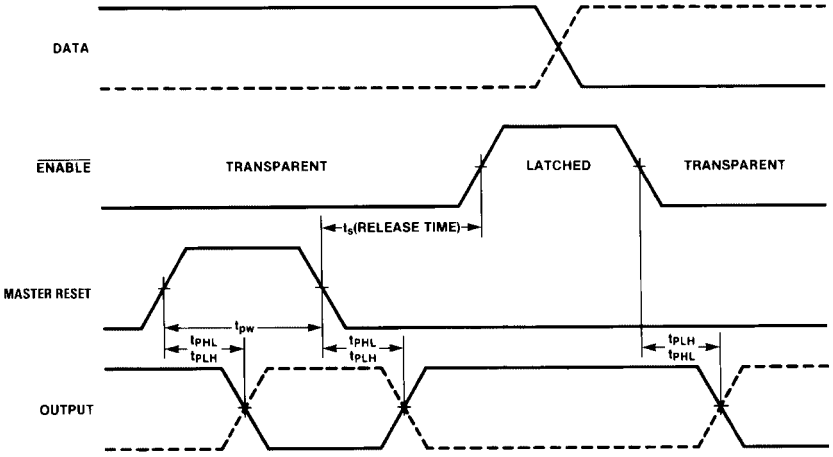
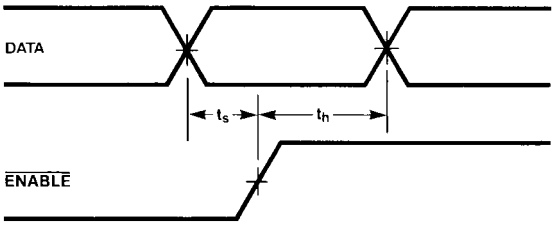



**FIGURE 3. Reset Timing**




**Notes:**

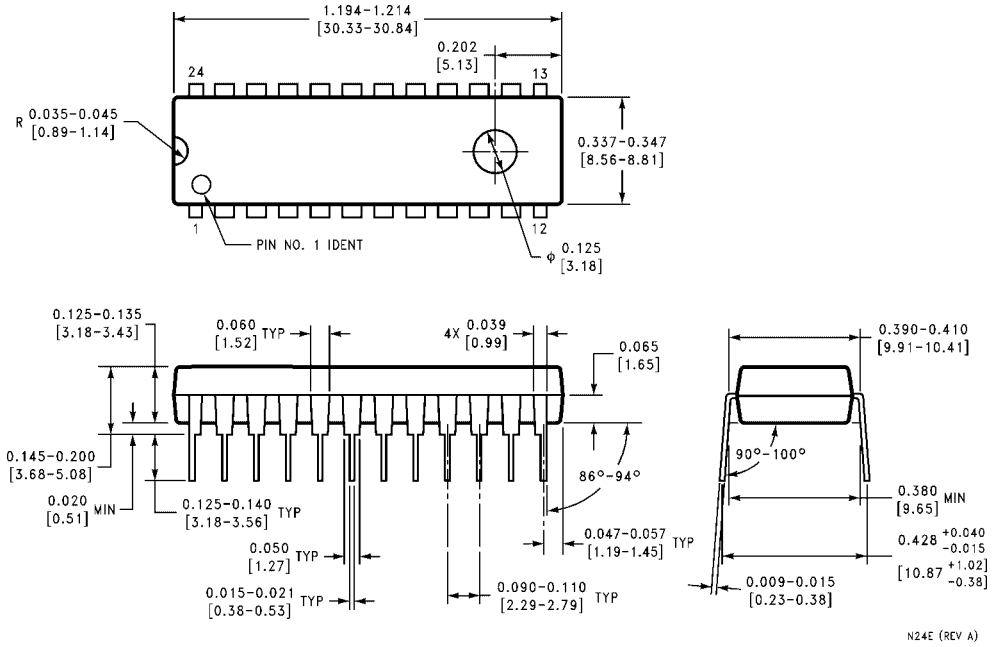
$t_S$ is the minimum time before the transition of the enable that information must be present at the data input.

$t_H$ is the minimum time after the transition of the enable that information must remain unchanged at the data input.

**FIGURE 4. Data Setup and Hold Time**

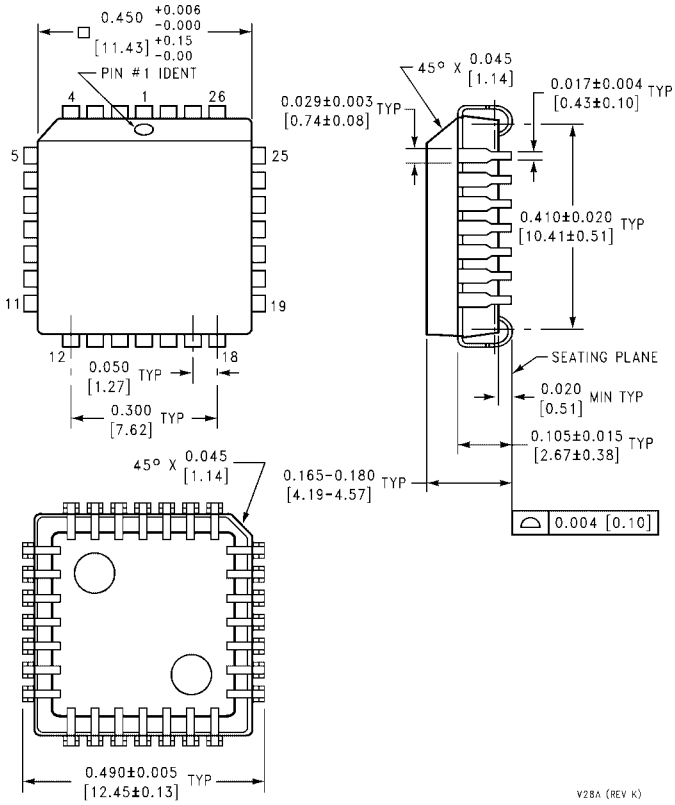
100350

## Physical Dimensions inches (millimeters) unless otherwise noted




**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide**
**Package Number N24E**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square**
**Package Number V28A**