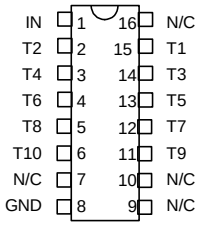
10-TAP DIP DELAY LINE
$T_D/T_R = 5$
(SERIES 1519)

data delay devices, inc.

FEATURES

- 10 taps of equal delay increment
- Delays as large as 300ns available
- Low DC resistance
- Standard 14-pin DIP package
- Epoxy encapsulated
- Meets or exceeds MIL-D-23859C

PACKAGES



1519-xxz
xx = Delay (T_D)
z = Impedance Code

FUNCTIONAL DESCRIPTION

The 1519-series device is a fixed, single-input, ten-output, passive delay line. The signal input (IN) is reproduced at the outputs (T1-T10) in equal increments. The delay from IN to T10 (T_D) is given by the device dash number. The characteristic impedance of the line is given by the letter code that follows the dash number (See Table). The rise time (T_R) of the line is 20% of T_D, and the 3dB bandwidth is given by 1.75 / T_D.

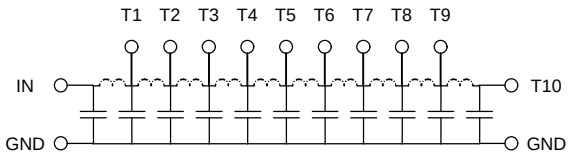
PIN DESCRIPTIONS

IN	Signal Input
T1-T10	Tap Outputs
GND	Ground

SERIES SPECIFICATIONS

- **Dielectric breakdown:** 50 Vdc
- **Distortion @ output:** 10% max.
- **Operating temperature:** -55°C to +125°C
- **Storage temperature:** -55°C to +125°C
- **Temperature coefficient:** 100 PPM/°C

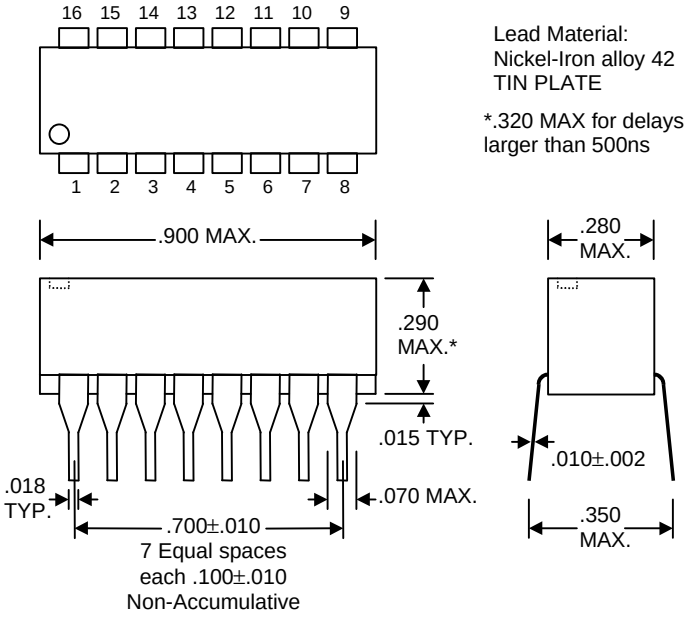
Functional Diagram



DASH NUMBER SPECIFICATIONS

Part Number	Delay (ns)	Imped (Ω)	RDC (Ω)	Part Number	Delay (ns)	Imped (Ω)	RDC (Ω)	Part Number	Delay (ns)	Imped (Ω)	RDC (Ω)
1519-20A	20 ± 1.0	50	1.0	1519-100C	100 ± 5.0	200	6.0	1519-360E	360 ± 18.0	300	21.0
1519-25A	25 ± 1.3	50	1.0	1519-120C	120 ± 6.0	200	6.5	1519-450E	450 ± 22.5	300	24.0
1519-30A	30 ± 1.5	50	1.2	1519-160C	160 ± 8.0	200	7.0	1519-600E	600 ± 30.0	300	40.0
1519-40A	40 ± 2.0	50	1.5	1519-180C	180 ± 9.0	200	8.5	1519-40F	40 ± 2.0	400	8.5
1519-45A	45 ± 2.3	50	1.5	1519-200C	200 ± 10.0	200	9.0	1519-80F	80 ± 4.0	400	9.0
1519-50A	50 ± 2.5	50	1.5	1519-240C	240 ± 12.0	200	9.5	1519-120F	120 ± 6.0	400	9.0
1519-60A	60 ± 3.0	50	1.5	1519-300C	300 ± 15.0	200	16.0	1519-160F	160 ± 8.0	400	16.0
1519-75A	75 ± 3.8	50	1.8	1519-400C	400 ± 20.0	200	18.0	1519-200F	200 ± 10.0	400	18.0
1519-100A	100 ± 5.0	50	2.0	1519-50D	50 ± 2.5	250	5.5	1519-240F	240 ± 12.0	400	20.0
1519-10B	10 ± 1.0	100	1.0	1519-75D	75 ± 3.8	250	6.0	1519-320F	320 ± 16.0	400	26.0
1519-20B	20 ± 1.0	100	1.5	1519-100D	100 ± 5.0	250	7.0	1519-360F	360 ± 18.0	400	28.0
1519-30B	30 ± 1.5	100	1.5	1519-125D	125 ± 6.3	250	8.0	1519-480F	480 ± 24.0	400	38.0
1519-40B	40 ± 2.0	100	1.8	1519-150D	150 ± 7.5	250	8.5	1519-600F	600 ± 30.0	400	45.0
1519-50B	50 ± 2.5	100	2.0	1519-200D	200 ± 10.0	250	10.0	1519-800F	800 ± 40.0	400	40.0
1519-60B	60 ± 3.0	100	3.0	1519-225D	225 ± 12.0	250	11.0	1519-50G	50 ± 2.5	500	6.0
1519-80B	80 ± 4.0	100	3.5	1519-300D	300 ± 15.0	250	17.0	1519-100G	100 ± 5.0	500	10.0
1519-90B	90 ± 4.5	100	3.5	1519-375D	375 ± 18.8	250	20.0	1519-150G	150 ± 7.5	500	16.0
1519-100B	100 ± 5.0	100	4.0	1519-500D	500 ± 25.0	250	24.0	1519-200G	200 ± 10.0	500	30.0
1519-120B	120 ± 6.0	100	4.0	1519-30E	30 ± 1.5	300	5.0	1519-250G	250 ± 12.5	500	25.0
1519-150B	150 ± 7.5	100	5.0	1519-60E	60 ± 3.0	300	6.0	1519-300G	300 ± 15.0	500	26.0
1519-200B	200 ± 10.0	100	6.0	1519-90E	90 ± 4.5	300	7.0	1519-400G	400 ± 20.0	500	42.0
1519-250B	250 ± 12.5	100	7.0	1519-120E	120 ± 6.0	300	8.0	1519-450G	450 ± 22.5	500	45.0
1519-20C	20 ± 1.0	200	3.0	1519-150E	150 ± 7.5	300	9.0	1519-500G	500 ± 25.0	500	55.0
1519-40C	40 ± 2.0	200	4.0	1519-180E	180 ± 9.0	300	11.0	1519-600G	600 ± 30.0	500	58.0
1519-60C	60 ± 3.0	200	4.5	1519-240E	240 ± 12.0	300	16.0	1519-750G	750 ± 37.5	500	50.0
1519-80C	80 ± 4.0	200	5.5	1519-270E	270 ± 13.5	300	18.0	1519-1000G	1000 ± 50	500	65.0

PACKAGE DIMENSIONS



Lead Material:
Nickel-Iron alloy 42
TIN PLATE

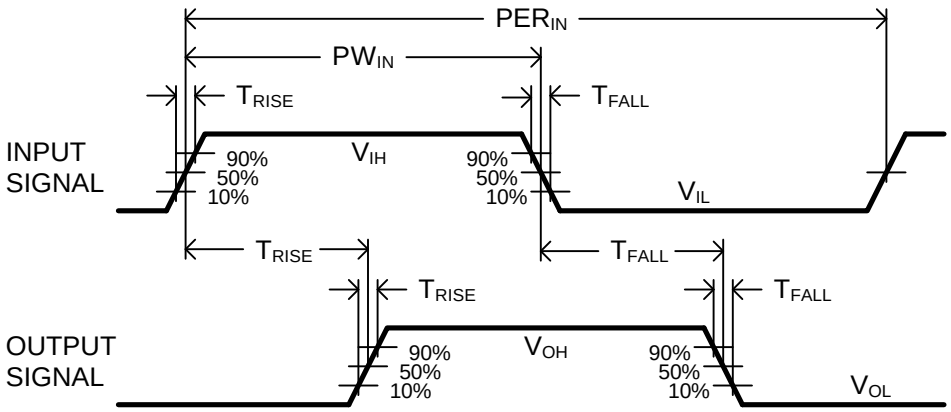
*.320 MAX for delays larger than 500ns

PASSIVE DELAY LINE TEST SPECIFICATIONS

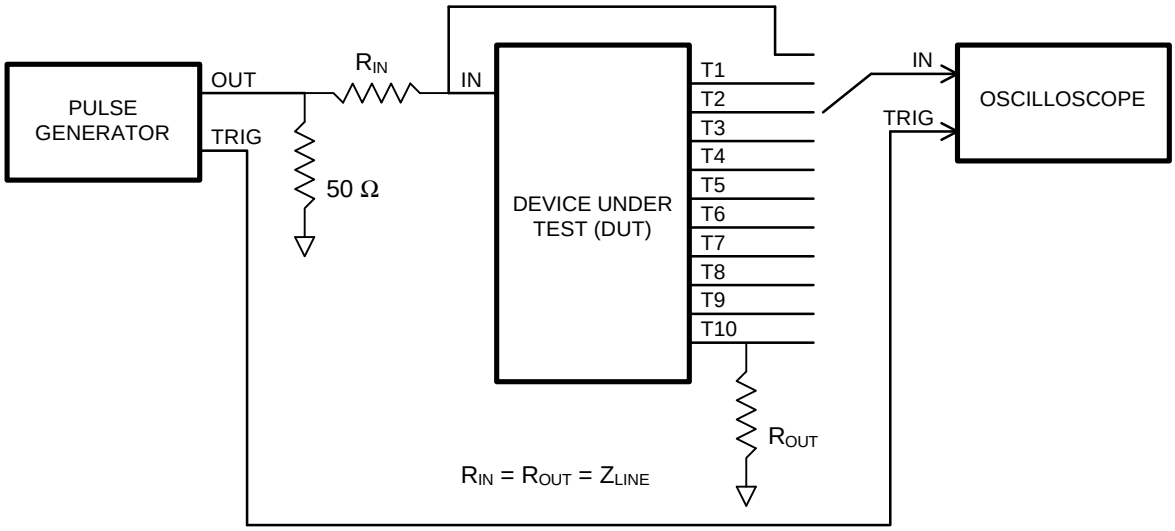
TEST CONDITIONS

INPUT:		**OUTPUT:**	
Ambient Temperature:	25°C ± 3°C	**R_{load}:**	10MΩ
Input Pulse:	High = 3.0V typical	**C_{load}:**	10pf
	Low = 0.0V typical	**Threshold:**	50% (Rising & Falling)
Source Impedance:	50Ω Max.		
Rise/Fall Time:	3.0 ns Max. (measured at 10% and 90% levels)		
Pulse Width (T_D <= 75ns):	PW_{IN} = 100ns		
Period (T_D <= 75ns):	PER_{IN} = 1000ns		
Pulse Width (T_D > 75ns):	PW_{IN} = 2 x T_D		
Period (T_D > 75ns):	PER_{IN} = 10 x T_D		

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Timing Diagram For Testing



Test Setup