



STS20NHS3LL

N-channel 30V - 0.0032Ω - 20A - SO-8™
STripFET™III Power MOSFET plus monolithic schottky

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STS20NHS3LL	30V	0.0042Ω	20A ⁽¹⁾

1. This value is rated accordingly to R_{thj-pcb}

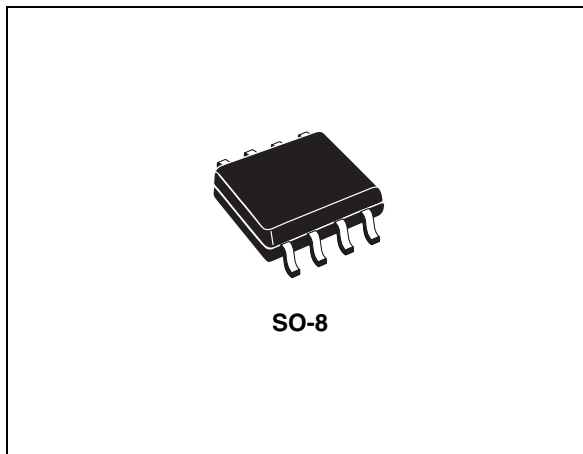
- Optimal R_{DS(on)} x Q_g trade-off @ 4.5V
- Reduced switching losses
- Reduced conduction losses
- Improved junction-case thermal resistance

Description

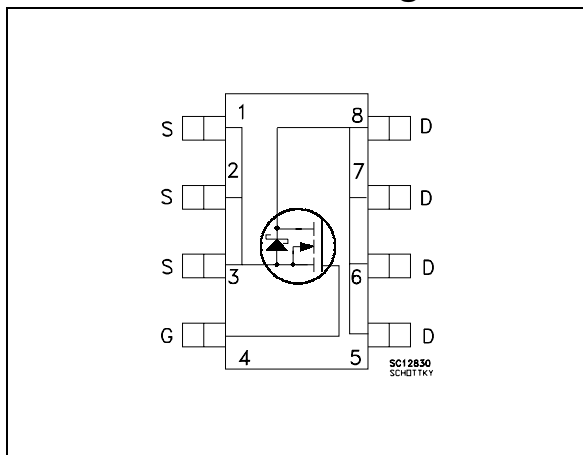
This product utilizes the latest advanced design rules of ST's proprietary STripFET™ technology and a proprietary process for integrating a monolithic Schottky diode. The new Power MOSFET is optimized for the most demanding synchronous switch function in DC-DC converter for Computer and Telecom.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STS20NHS3LL	20HS3LL-	SO-8	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	± 16	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	20	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	12.6	A
$I_{DM}^{(2)}$	Drain current (pulsed)	80	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	2.7	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. This value is rated accordingly to $R_{thj-pcb}$

2. Pulse width limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	47	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4 board, 2oz Cu. ($t < 10\text{sec.}$)

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, not repetitive (pulse width limited by T_{jmax})	10	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 24\text{V}$)	1.8	J

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 24V$			500	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1mA$	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 10A$ $V_{GS} = 4.5V, I_D = 10A$		0.0032 0.004	0.0042 0.0057	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10V, I_D = 15A$		44		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1MHz, V_{GS} = 0$		4200		pF
C_{oss}	Output capacitance			700		pF
C_{rss}	Reverse transfer capacitance			46.2		pF
Q_g	Total gate charge	$V_{DD} = 15V, I_D = 20A$		27	35	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5V,$		8.5		nC
Q_{gd}	Gate-drain charge	(see Figure 13)		7.2		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=15V$, $I_D=10A$, $R_G=4.7\Omega$, $V_{GS}=4.5V$ (see Figure 12)		16 45		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=15V$, $I_D=10A$, $R_G=4.7\Omega$, $V_{GS}=4.5V$ (see Figure 12)		68 8		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				20 80	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=5A$, $V_{GS}=0$			0.75	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=20A$, $di/dt = 100A/\mu s$, $V_{DD}=25V$, $T_j=150^\circ C$ (see Figure 17)		30 30 2		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

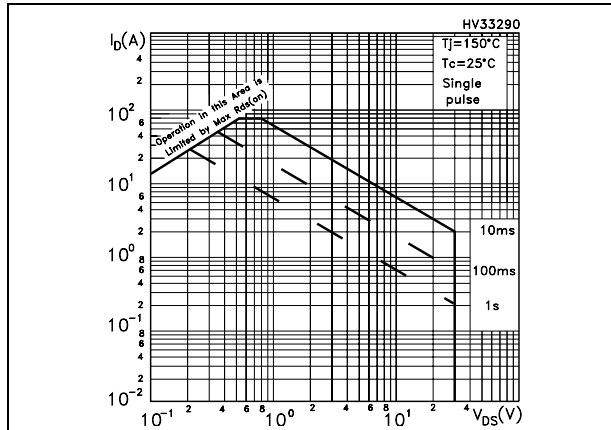


Figure 2. Thermal impedance

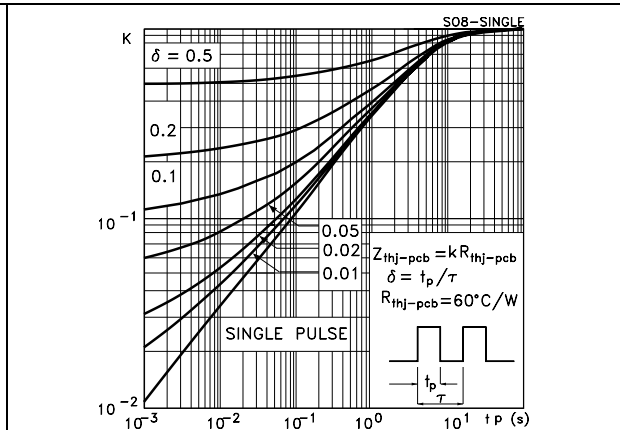


Figure 3. Output characteristics

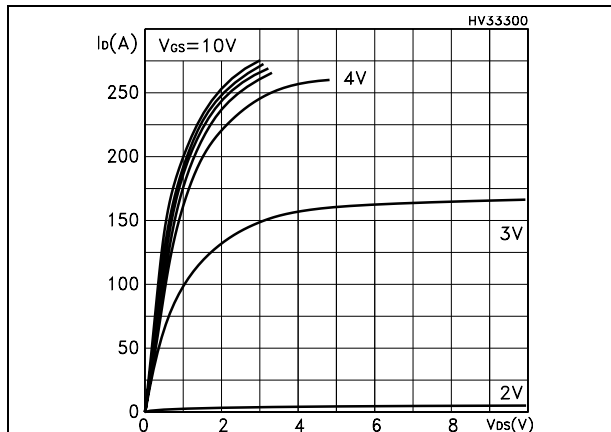


Figure 4. Transfer characteristics

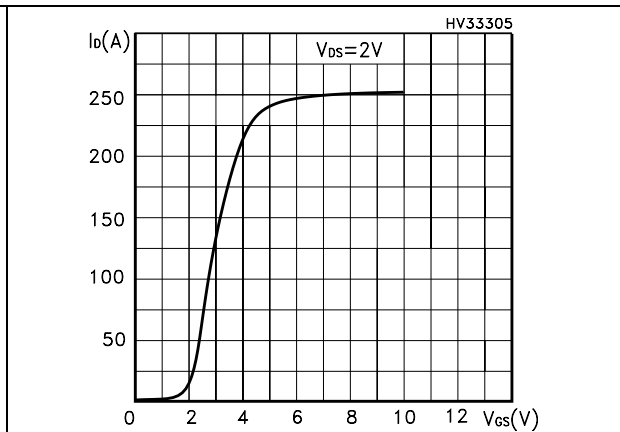


Figure 5. Normalized $B_{V_{DS}}$ vs. temperature

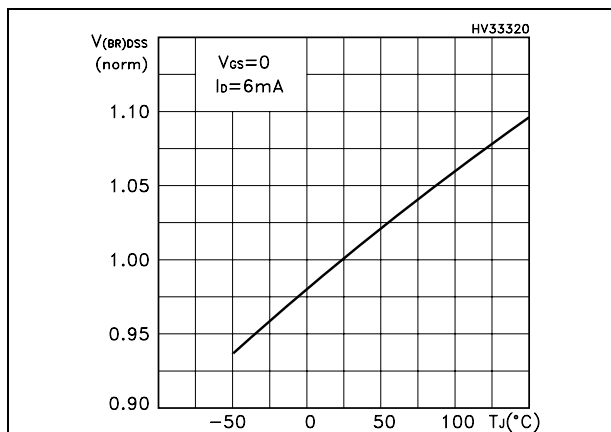


Figure 6. Static drain-source on resistance

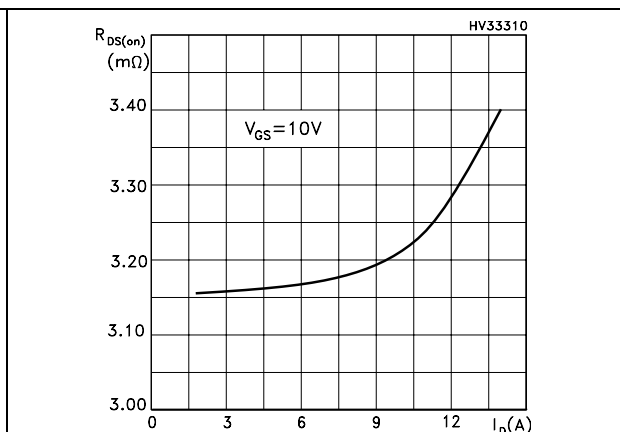


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

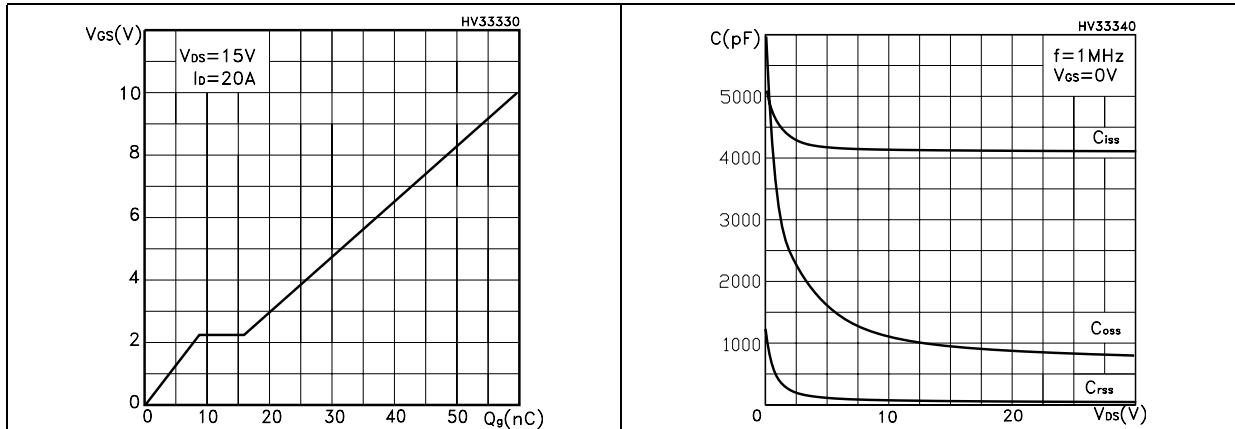


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

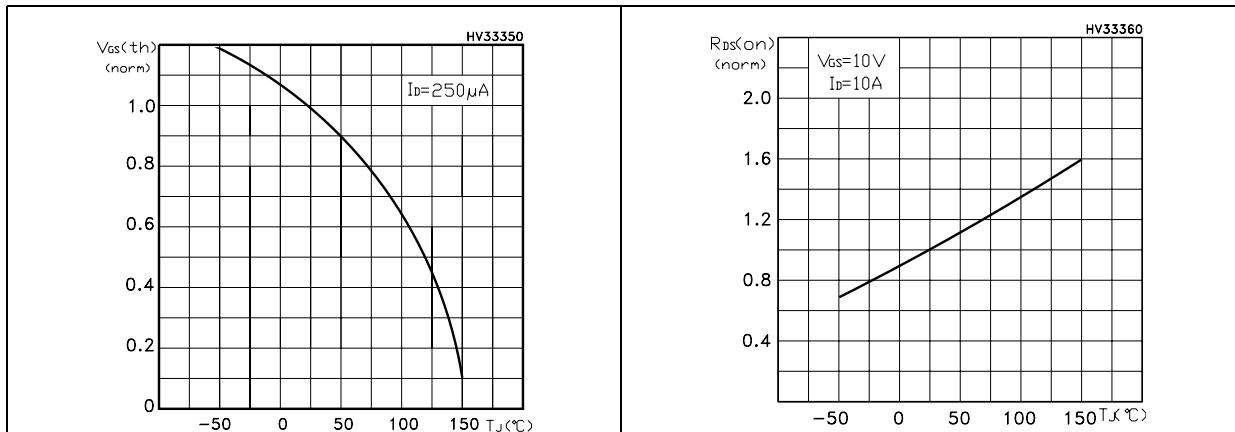
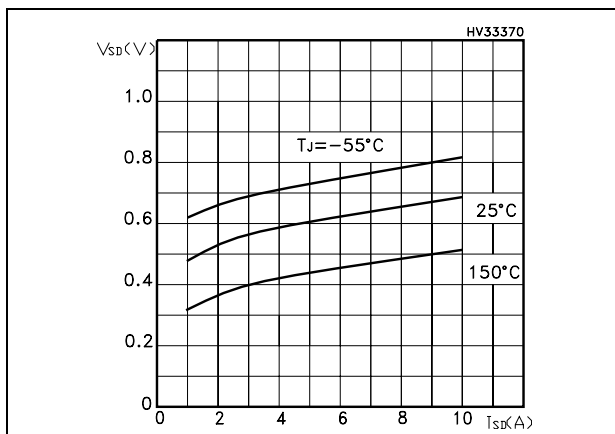


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

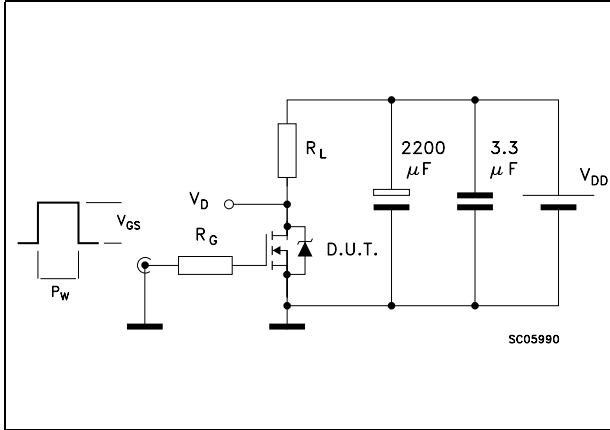


Figure 13. Gate charge test circuit

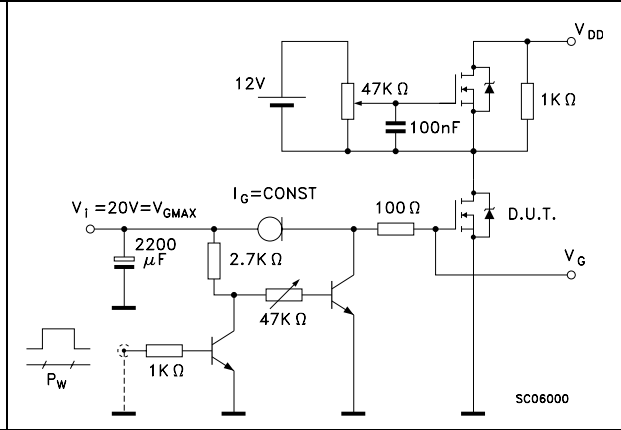


Figure 14. Test circuit for inductive load switching and diode recovery times

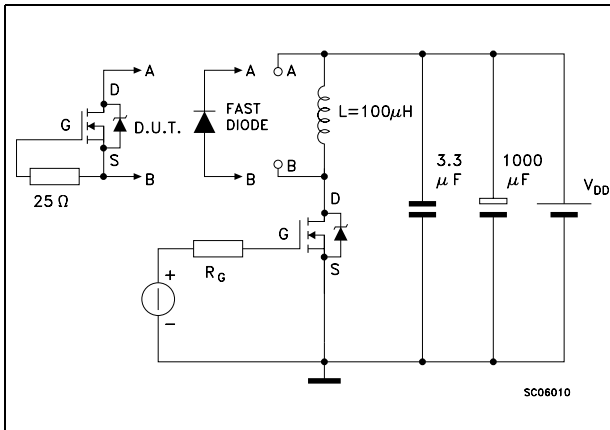


Figure 15. Unclamped inductive load test circuit

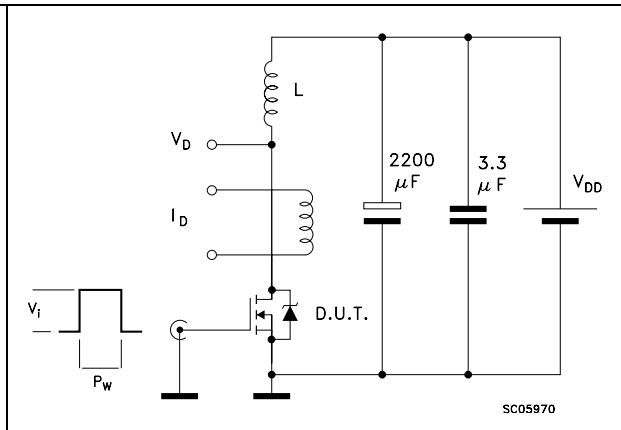


Figure 16. Unclamped inductive waveform

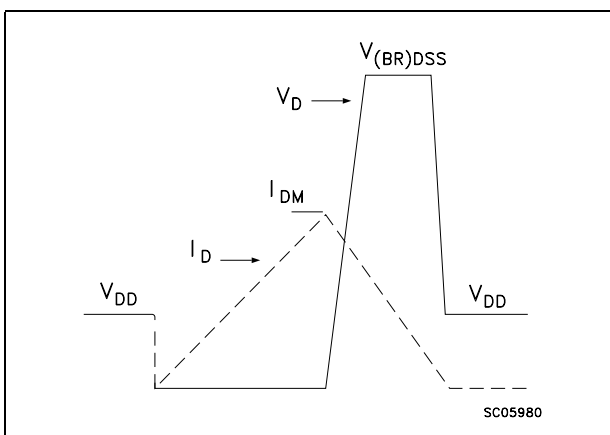
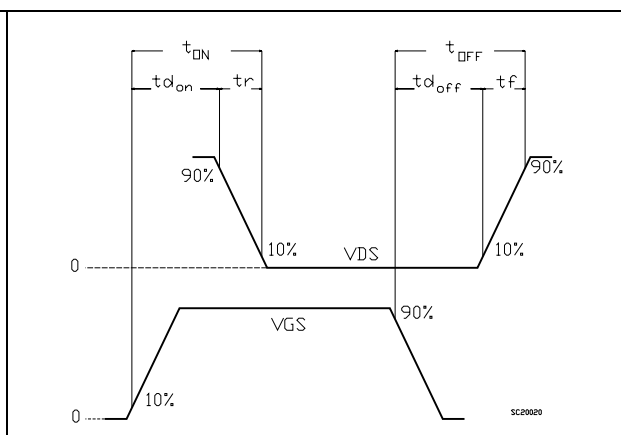


Figure 17. Switching time waveform

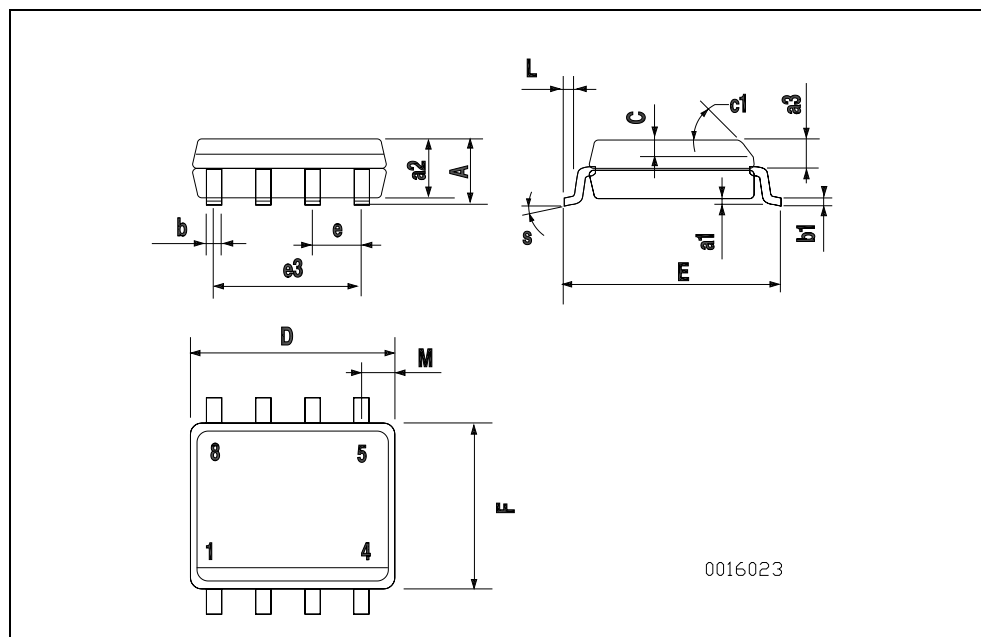


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 8. Revision history

Date	Revision	Changes
24-May-2005	1	Initial release.
19-Dec-2005	2	Inserted curves
05-Jan-2006	3	Modified value on <i>On/off states</i>
18-Jul-2006	4	The document has been reformatted
31-Jan-2007	5	Typo mistake on <i>Table 1</i> .

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