

NOT RECOMMENDED FOR NEW DESIGNS

MOTOROLA SC (DIODES/OPTO) 25E D ■ 6367255 0080908 0 ■ T-25-15

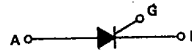
Silicon Controlled Rectifiers Reverse Blocking Triode Thyristors

... multi-purpose PNP silicon controlled rectifiers suited for industrial, consumer, and military applications. Offered in a choice of space-saving, economical packages for mounting versatility.

- Uniform Low-Level Noise-Immune Gate Triggering — $I_{GT} = 10 \text{ mA (Typ) @ } T_C = 25^\circ\text{C}$
- Low Forward "On" Voltage — $V_T = 1 \text{ V (Typ) @ 5 Amp @ } 25^\circ\text{C}$
- High Surge-Current Capability — $I_{TSM} = 100 \text{ Amp Peak}$
- Shorted Emitter Construction

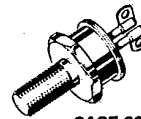
**2N4168
thru
2N4174
2N4184
thru
2N4190**

**SCRs
8 AMPERES RMS
50 thru 600 VOLTS**



MAXIMUM RATINGS (Apply over operating temperature range and for all case types unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Forward and Reverse Blocking Voltage, Note 1	V _{DRM} or V _{RRM}	50 100 200 400 600	Volts
Forward Current RMS	I _{T(RMS)}	8	Amps
*Peak Forward Surge Current (One cycle, 60 Hz, T _J = -40 to +100°C)	I _{TSM}	100	Amps
Circuit Fusing (t = 8.3 ms)	I ² t	40	A ² s
*Peak Gate Power	P _{GM}	5	Watts
*Average Gate Power	P _{G(AV)}	0.5	Watt
*Peak Gate Current	I _{GM}	2	Amps
Peak Gate Voltage, Note 2	V _{GM}	10	Volts
*Operating Temperature Range	T _J	-40 to +100	°C
*Storage Temperature Range	T _{stg}	-40 to +150	°C
Stud Torque		15	in. lb.



**CASE 86-01
STYLE 1
2N4168 thru 2N4174**



**CASE 87L-02
STYLE 1
2N4184 thru 2N4190**

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	2.5*	°C/W
Thermal Resistance, Case to Ambient (See Figure 11) 2N4183-98	$R_{\theta CA}$	50	—	°C/W

*Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM} , gate open) $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	I_{DRM}, I_{RRM}	— —	— —	10 2	μA mA
Gate Trigger Current (Continuous dc), Note 1 ($V_D = 7 \text{ Vdc}$, $R_L = 100 \Omega$) *($V_D = 7 \text{ Vdc}$, $R_L = 100 \Omega$, $T_C = -40^\circ\text{C}$)	I_{GT}	— —	10	30 60	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 7 \text{ Vdc}$, $R_L = 100 \Omega$) *($V_D = 7 \text{ Vdc}$, $R_L = 100 \Omega$, $T_C = -40^\circ\text{C}$) *($V_D = 7 \text{ Vdc}$, $R_L = 100 \Omega$, $T_C = 100^\circ\text{C}$)	V_{GT}	— — 0.2	0.75	1.5 2.5	Volts
*Forward "On" Voltage (pulsed, 1 ms max, duty cycle $\leq 1\%$) ($I_{TM} = 15.7 \text{ A}$)	V_{TM}	—	1.4	2	Volts
Holding Current ($V_D = 7 \text{ Vdc}$, gate open) *($V_D = 7 \text{ Vdc}$, gate open, $T_C = -40^\circ\text{C}$)	I_H	— —	10	30 60	mA
Turn-On Time ($t_d + t_r$) ($I_G = 20 \text{ mA}$, $I_F = 5 \text{ Adc}$, $V_D = \text{Rated } V_{DRM}$)	t_{on}	—	1	—	μs
Turn-Off Time ($I_F = 5 \text{ Adc}$, $I_R = 5 \text{ Adc}$) ($I_F = 5 \text{ Adc}$, $I_R = 5 \text{ Adc}$, $T_C = 100^\circ\text{C}$, $V_D = \text{Rated } V_{DRM}$) ($dv/dt = 30 \text{ V}/\mu\text{s}$)	t_{off}	— —	15 25	—	μs
Forward Voltage Application Rate (Exponential) (Gate open, $T_C = 100^\circ\text{C}$, $V_D = \text{Rated } V_{DRM}$)	dv/dt	—	50	—	$\text{V}/\mu\text{s}$

*Indicates JEDEC Registered Data

Note 1. For optimum operation, i.e. faster turn-on, lower switching losses, best dv/dt capability, recommended $I_{GT} = 200 \text{ mA}$ minimum.

TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 - PULSE CURRENT TRIGGERING

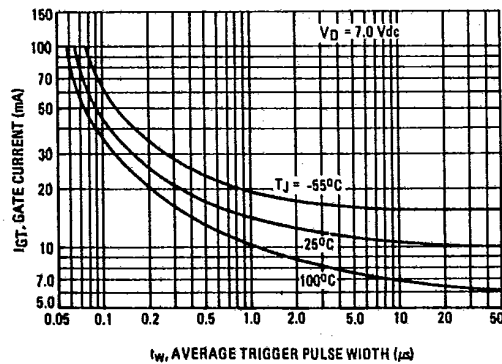
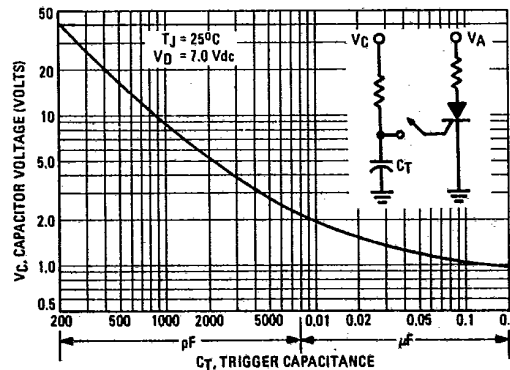


FIGURE 2 - CAPACITIVE DISCHARGE TRIGGERING



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CURRENT DERATING

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FIGURE 3 - MAXIMUM CASE TEMPERATURE

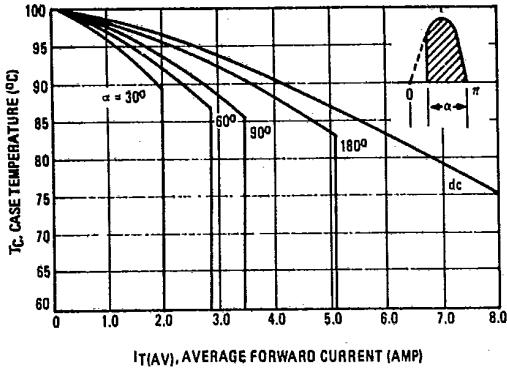
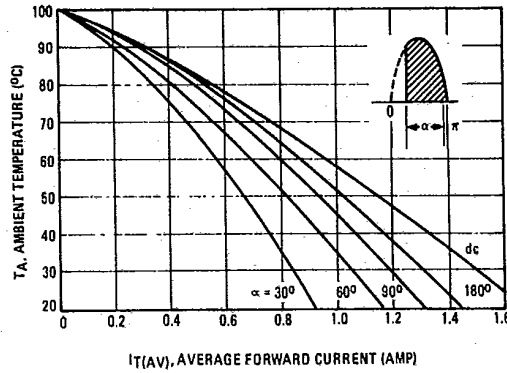


FIGURE 4 - MAXIMUM AMBIENT TEMPERATURE



MOTOROLA SC (DIODES/OPTO)

25E D

FIGURE 5 - POWER DISSIPATION

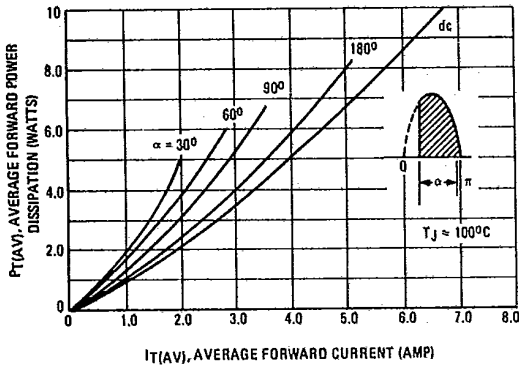
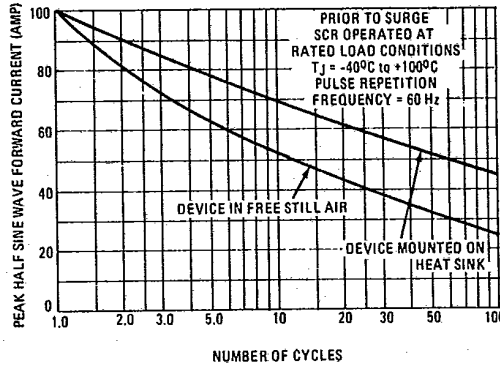
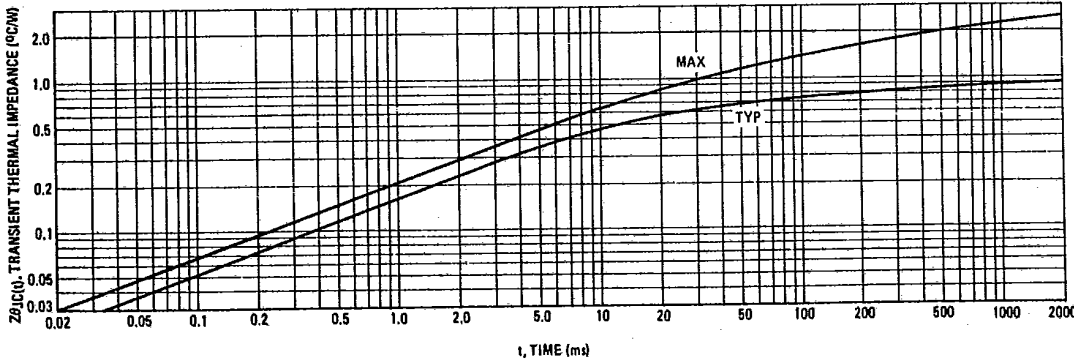


FIGURE 6 - MAXIMUM SURGE CAPABILITY



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FIGURE 7 - THERMAL RESPONSE



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FIGURE 8 - FORWARD VOLTAGE

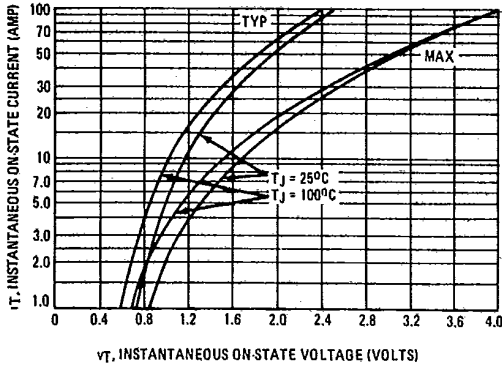


FIGURE 9 - HOLDING CURRENT

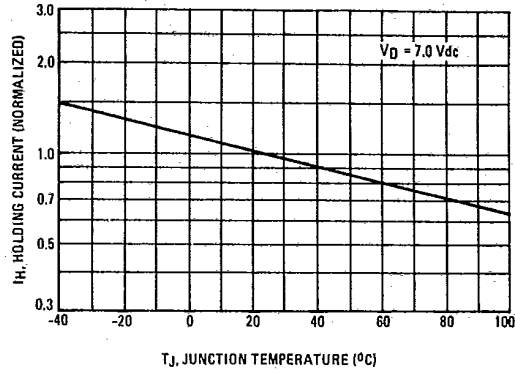


FIGURE 10 - TYPICAL THERMAL RESISTANCE OF PLATES

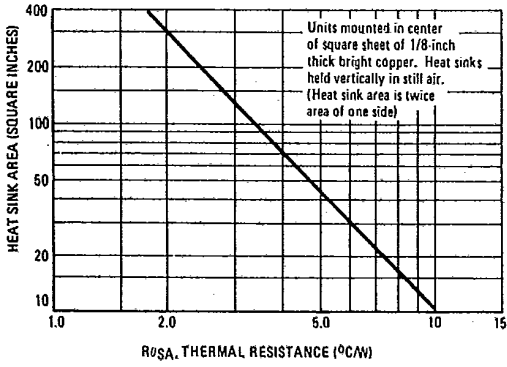
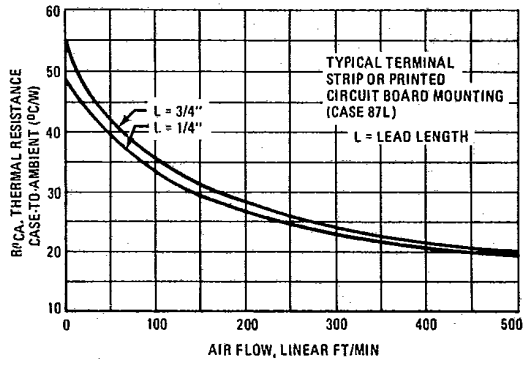


FIGURE 11 - CASE-TO-AMBIENT THERMAL RESISTANCE



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