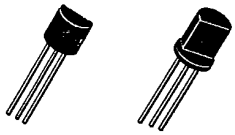
Unijunction Transistors and Switches

T-25-09

2N6027, 2N6028, GES6027, GES6028

Programmable Unijunction Transistor



TO-92 TO-98

Features:
- Planar Passivated Structure
- Low Leakage Current
- Low Peak Point Current
- Low Forward Voltage
- Fast, High Energy Trigger Pulse
- Programmable η
- Programmable R_{BB}
- Programmable I_P
- Programmable I_V
- Low Cost

Applications:
- SCR Trigger
- Pulse and Timing Circuits
- Oscillators
- Sensing Circuits
- Sweep Circuits

The GE/RCA 2N6027, 2N6028 and GES6027, GES6028 PUTS are PNP three-terminal planar passivated devices available in the standard plastic TO-98 and TO-92 packages. The terminals are designated as anode, anode gate and cathode.

The devices have been characterized as Programmable Unijunction Transistors (PUT), offering many advantages over conventional unijunction transistors. The designer can select R_1 and R_2 to program unijunction characteristics such as η, R_{BB}, I_P and I_V to meet his particular needs.

PUTs are specifically characterized for long interval timers and other applications requiring low leakage and low peak point current. PUTs similar types have been characterized for general use wheren the low peak point current of the 2N6028 and others is not essential. Applications of the PUT include timers, high gain phase control circuits and relaxation oscillators.

Operation of the PUT as a unijunction is easily understood. Figure 1(a) shows a basic unijunction circuit. Figure 2(a) shows identically the same circuit except that the unijunction transistor is replaced by the PUT plus resistors R_1 and R_2. Comparing the equivalent circuits of Figure 1(b) and 2(b), it is seen that both circuits have a diode connected to a voltage divider. When this diode becomes forward biased in the unijunction transistor, R_1 becomes strongly modulated to a lower resistance value. This generates a negative resistance characteristic between the emitter E and base one (B_1. For the PUT, the resistors R_1 and R_2 control the voltage at which the diode (anode to gate) becomes forward biased. After the diode conducts, the regeneration inherent in a PNPN device causes the PUT to switch on. This generates a negative resistance characteristic from anode to cathode (Figure 2(b) simulating the modulation of R_1 for a conventional unijunction.

Resistors R_{B2} and R_{B1} (Figure 1(a)) are generally unnecessary when the PUT replaces a conventional UJT. This is illustrated in Figure 2(c). Resistor R_{B1} is often used to bypass the interbase current of the unijunction which would otherwise trigger the SCR. Since R_1 in the case of the PUT, can be returned directly to ground there is not current to bypass at the SCR gate. Resistor R_{B2} is used for temperature compensation and for limiting the dissipation in the UJT during capacitor discharge. Since R_2 (Figure 2) is *not* modulated, R_{B2} can be absorbed into it.

These types are supplied in JEDEC TO-92 package (GES6027, GES6028) and in JEDEC TO-98 package (2N6027, 2N6028).

Devices in TO-98 package are supplied with and without seating flange (see Dimensional Outline).

File Number **2050**

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

GATE-CATHODE FORWARD VOLTAGE*	+100V
GATE-CATHODE REVERSE VOLTAGE*	−100V
GATE-ANODE REVERSE VOLTAGE*	+100V
ANODE-CATHODE VOLTAGE*	±100V
DC ANODE CURRENT* (Note 1)	150 mA
PEAK ANODE, RECURRENT FORWARD	
(100μs pulse width, 1% duty cycle)	1 A
(20μs pulse width, 1% duty cycle)*	2 A
PEAK ANODE, NON-RECURRENT FORWARD (10μsec)	5 A
GATE CURRENT*	±20 mA
CAPACITIVE DISCHARGE ENERGY (Note 2)	250μJ
DISSIPATION (Total Average Power)(Note 1)	300 mW
OPERATING AMBIENT TEMPERATURE RANGE (Note 1)	−50° to +100°C

* In accordance with JEDEC registration data format.
NOTES:
1. Derate currents and powers 1%/°C above 25°C.
2. E = 1/2 CV2 capacitor discharge energy with no current limiting

3

ELECTRICAL CHARACTERISTICS, At Ambient Temperature (T_A) = 25°C Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	LIMITS				UNITS
		2N6027 GES6027		2N6028 GES6028		
		MIN.	MAX.	MIN.	MAX	
Forward Voltage* (I_F = 50mA)	V_F	–	1.5	–	1.5	V
Pulse Output Voltage*	V_O	6	–	6	–	
Offset Voltage* (V_S = 10 V) R_G = MΩ	V_T	0.2	1.6	0.2	1.6	
R_G = 10 kΩ		0.2	0.6	0.2	0.6	
Peak Current* (V_S = 10 V) R_G = 1 MΩ	I_P	–	2	–	0.15	μA
R_G = 10kΩ		–	5	–	1	
Valley Current* (V_S = 10V) R_G = 1 MΩ	I_V	–	50	–	25	
R_G = 10 kΩ		70	–	25	–	
R_G = 200 Ω		1.5	–	1	–	mA
Anode Gate-Anode Leakage Current (V_S = 40 V)* T = 25°C	I_{GAO}	–	10	–	10	nA
T = 75°C		–	100	–	100	
Gate to Cathode Leakage Current V_S = 40 V, Anode-cathode short	I_{GKS}	–	100	–	100	
Pulse Voltage Rate of Rise	t_r	–	80	–	80	ns

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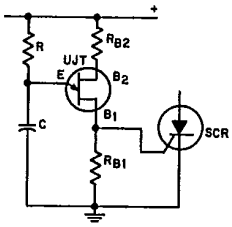
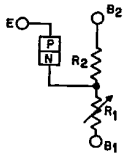


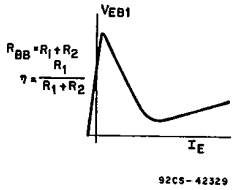
Typical circuit

(a)



Unijunction transistor equivalent circuit

(b)



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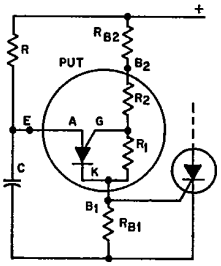
Negative resistance characteristic

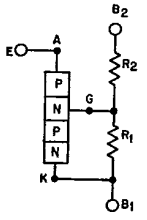
(c)

Fig. 1—Unijunction transistor



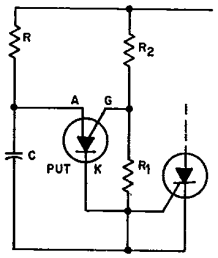
Programmable unijunction transistor replacing unijunction transistor in typical circuit, Fig. 1, a.

(a)



Programmable unijunction transistor equivalent circuit

(b)



92CS-42330

Simplified, typical circuit, Fig. 1, a utilizing programmable unijunction transistor.

(c)

Fig. 2—Programmable unijunction transistor equivalent of unijunction transistor.

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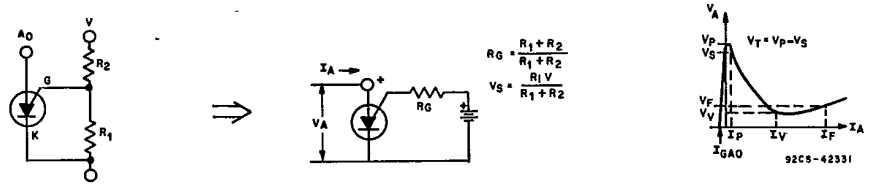

Fig. 3—Offset voltage, peak current, and voltage current measurement circuits and waveform.

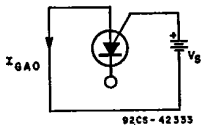

Fig. 4—Anode gate-anode leakage current measurement circuit.

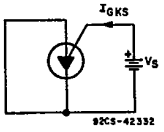

Fig. 5—Gate to cathode leakage current measurement circuit.

Fig. 6—Pulse output voltage and pulse voltage rate-of-rise measurement circuit and waveform.

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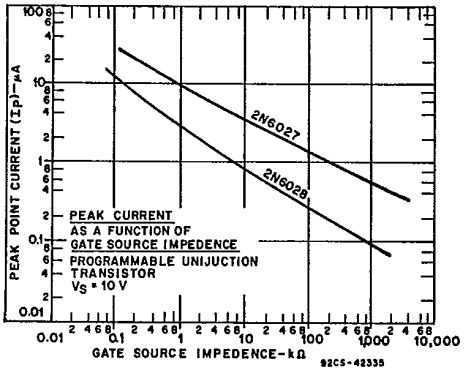

Fig. 7—Typical peak point current characteristics.

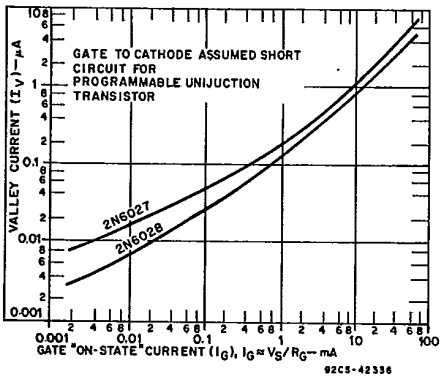

Fig. 8—Typical valley current characteristics.

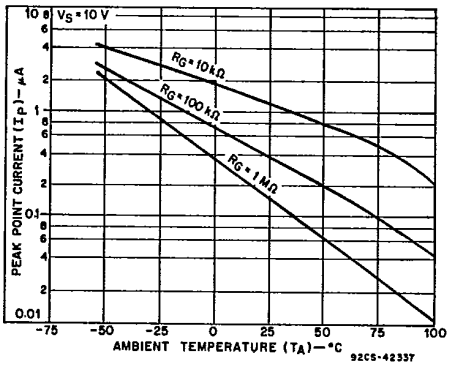

Fig. 9—Typical peak point current characteristics.

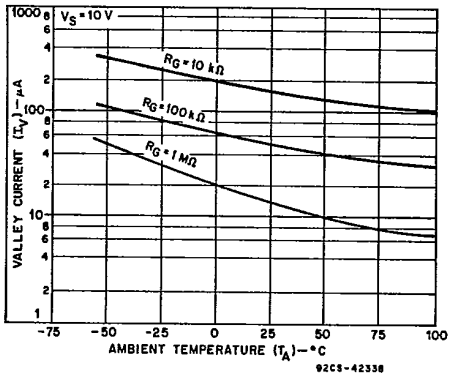

Fig. 10—Typical valley current characteristics.

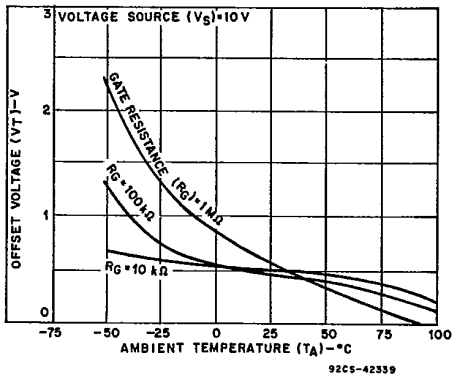

Fig. 11—Typical offset voltage characteristics.

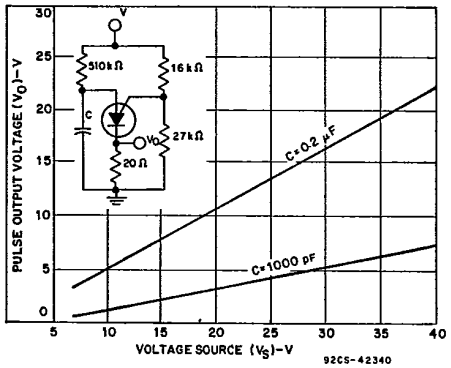

Fig. 12—Typical pulse voltage characteristics.

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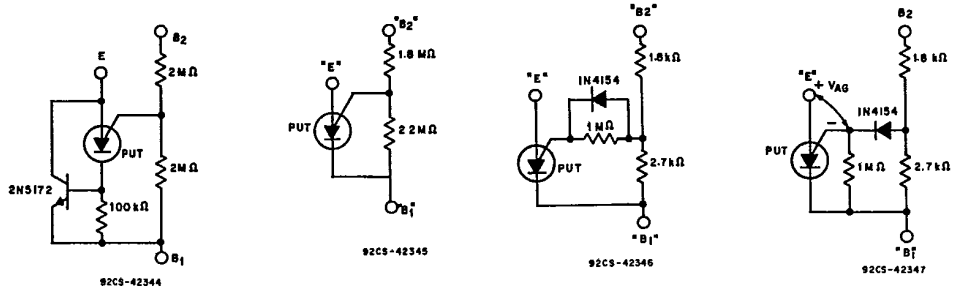
Here are four ways to use the PUT as a unijunction. Note the flexibility due to "programmability." Applications from long time interval latching timers to wide range relaxation oscillators are possible.



Low Ip; very high Iv, temperature and V_{BB} compensation

Low Ip and Iv

Low Ip; medium Iv, temperature, V_G compensation

Low Ip, medium Iv

Fig. 13—Typical programmable unijunction transistor circuits.

This sampling circuit lowers the effective peak current of the output PUT, Q2. By allowing the capacitor to charge with high gate voltage and periodically lowering gate voltage, when Q1 fires, the timing reistor can be a value which supplies a much lower current than I_P. The triggering requirement here is that minimum charge to trigger flow through the timing resistor during the period of the Q1 oscillator. This is not capacitor size dependent, only capacitor leakage and stability dependent.

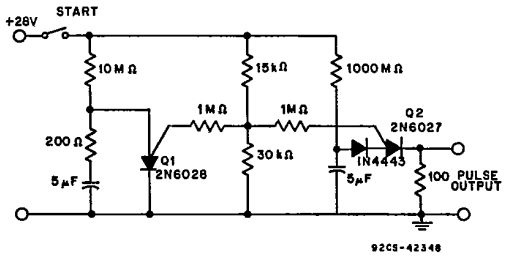


Fig. 14—Hour time-delay sampling circuit.

Here is a handy circuit which operates as an oscillator *and* a timer. The 2N6028 is normally on due to excess holding current through the 100 kohm resistor. When the switch is momentarily closed, the 10 μF capacitor is charged to a full 15 volts and 2N6028 starts oscillating (1.8 Meg and 820 pF). The circuit latches when 2N2926 zener breaks down again.

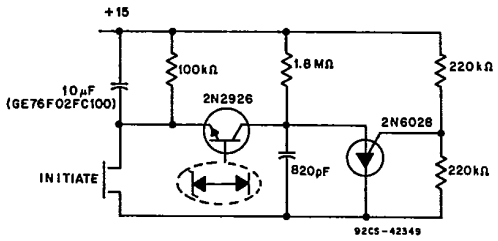


Fig. 15—1-second, 1kHz oscillator circuit.

TERMINAL CONNECTIONS

TO-92 and TO-98 Packages
Lead 1 - Anode
Lead 2 - Gate
Lead 3 - Cathode