2N6071A/B Series

Preferred Device

Sensitive Gate Triacs

Silicon Bidirectional Thyristors

Designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Sensitive Gate Triggering Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions
- Gate Triggering 4 Mode — 2N6071A,B, 2N6073A,B, 2N6075A,B
- Blocking Voltages to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Device Marking: Device Type, e.g., 2N6071A, Date Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage(1) (T_J = −40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open) 2N6071A,B 2N6073A,B 2N6075A,B	V_{DRM}, V_{RRM}	 200 400 600	Volts
*On-State RMS Current (T_C = 85°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	4.0	Amps
*Peak Non–repetitive Surge Current (One Full cycle, 60 Hz, T_J = +110°C)	I_{TSM}	30	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	3.7	A^2s
*Peak Gate Power (Pulse Width ≤ 1.0 μs, T_C = 85°C)	P_{GM}	10	Watts
*Average Gate Power (t = 8.3 ms, T_C = 85°C)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Voltage (Pulse Width ≤ 1.0 μs, T_C = 85°C)	V_{GM}	5.0	Volts
*Operating Junction Temperature Range	T_J	–40 to +110	°C
*Storage Temperature Range	T_{stg}	–40 to +150	°C
Mounting Torque (6-32 Screw)(2)	—	8.0	in. lb.

*Indicates JEDEC Registered Data.

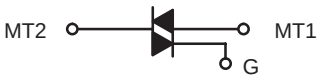
(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

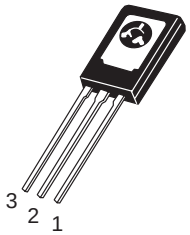
(2) Torque rating applies with use of a compression washer. Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.

ON Semiconductor

http://onsemi.com

TRIACS
4 AMPERES RMS
200 thru 600 VOLTS





TO–225AA
(formerly TO–126)
CASE 077
STYLE 5

PIN ASSIGNMENT	
1	Main Terminal 1
2	Main Terminal 2
3	Gate

ORDERING INFORMATION

Device	Package	Shipping
2N6071A	TO225AA	500/Box
2N6071B	TO225AA	500/Box
2N6073A	TO225AA	500/Box
2N6073B	TO225AA	500/Box
2N6075A	TO225AA	500/Box
2N6075B	TO225AA	500/Box

Preferred devices are recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
*Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, V_{RRM}; Gate Open)	T_J = 25°C T_J = 110°C	I_{DRM}, I_{RRM}	— —	— —	10 2	μA mA
ON CHARACTERISTICS						
*Peak On-State Voltage(1) (I_{TM} = ±6 A Peak)		V_{TM}	—	—	2	Volts
*Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = –40°C) All Quadrants		V_{GT}	—	1.4	2.5	Volts
Gate Non–Trigger Voltage (Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = 110°C) All Quadrants		V_{GD}	0.2	—	—	Volts
*Holding Current (Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = ±1 Adc)	(T_J = –40°C) (T_J = 25°C)	I_H	— —	— —	30 15	mA
Turn-On Time (I_{TM} = 14 Adc, I_{GT} = 100 mAdc)		t_{gt}	—	1.5	—	μs

			QUADRANT (Maximum Value)			
	Type	**I_{GT} @ T_J**	**I mA**	**II mA**	**III mA**	**IV mA**
Gate Trigger Current (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 100 ohms)	2N6071A 2N6073A 2N6075A	+25°C	5	5	5	10
		–40°C	20	20	20	30
	2N6071B 2N6073B 2N6075B	+25°C	3	3	3	5
		–40°C	15	15	15	20

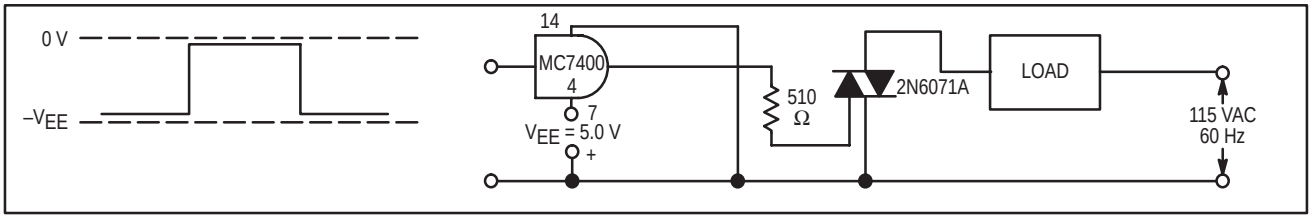
DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Commutation Voltage @ V_{DRM}, T_J = 85°C, Gate Open, I_{TM} = 5.7 A, Exponential Waveform, Commutating di/dt = 2.0 A/ms	dv/dt(c)	—	5	—	V/μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

SAMPLE APPLICATION:
TTL-SENSITIVE GATE 4 AMPERE TRIAC
TRIGGERS IN MODES II AND III

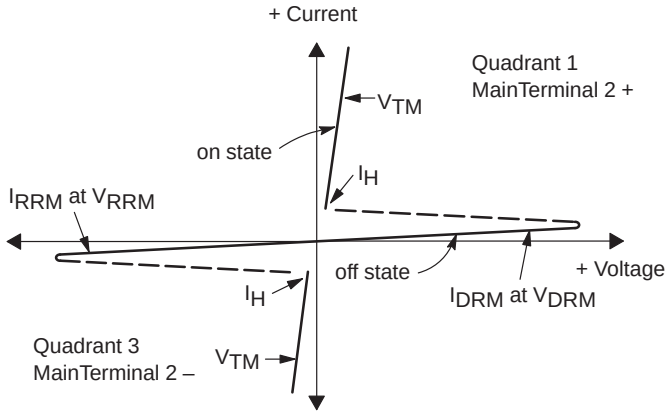


Trigger devices are recommended for gating on Triacs. They provide:

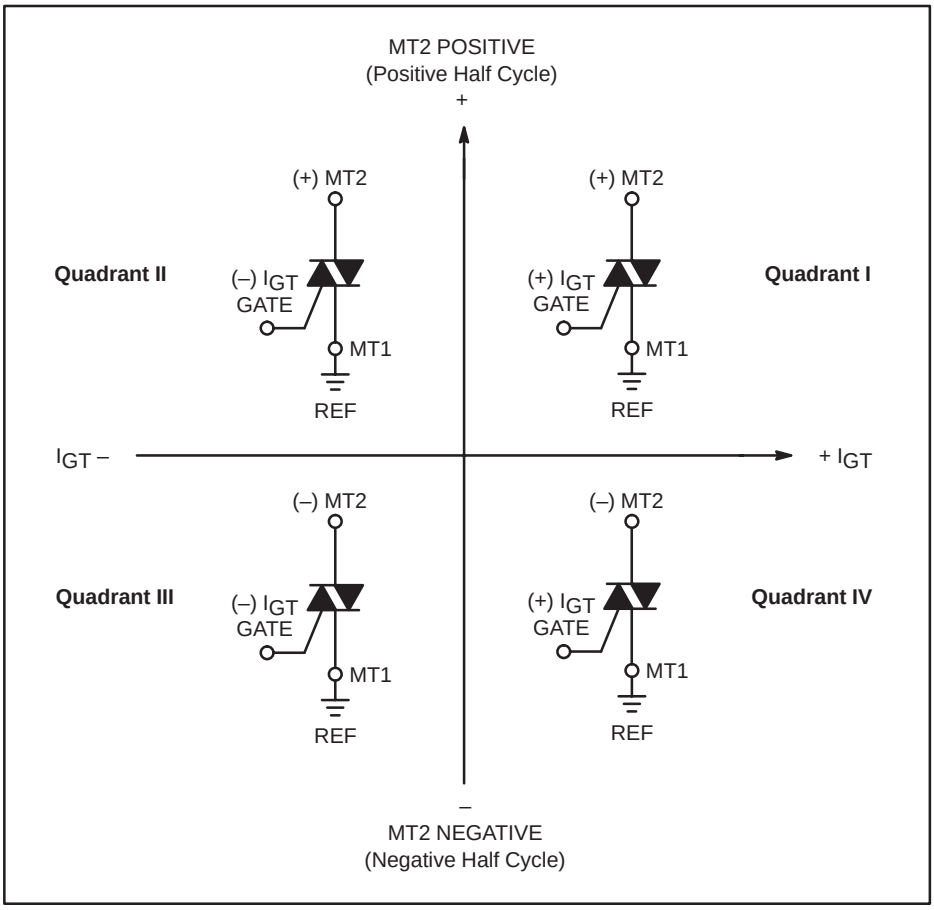
1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in–phase signals (using standard AC lines) quadrants I and III are used.

SENSITIVE GATE LOGIC REFERENCE

IC Logic Functions	Firing Quadrant			
	I	II	III	IV
TTL		2N6071A Series	2N6071A Series	
HTL		2N6071A Series	2N6071A Series	
CMOS (NAND)	2N6071B Series			2N6071B Series
CMOS (Buffer)		2N6071B Series	2N6071B Series	
Operational Amplifier	2N6071A Series			2N6071A Series
Zero Voltage Switch		2N6071A Series	2N6071A Series	

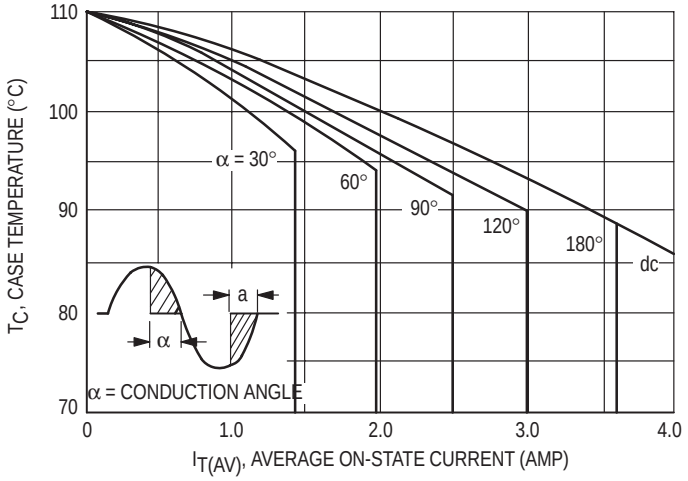


Figure 1. Average Current Derating

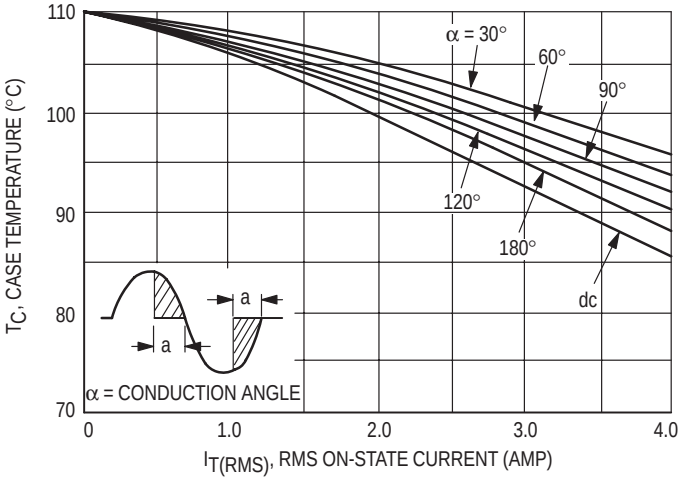


Figure 2. RMS Current Derating

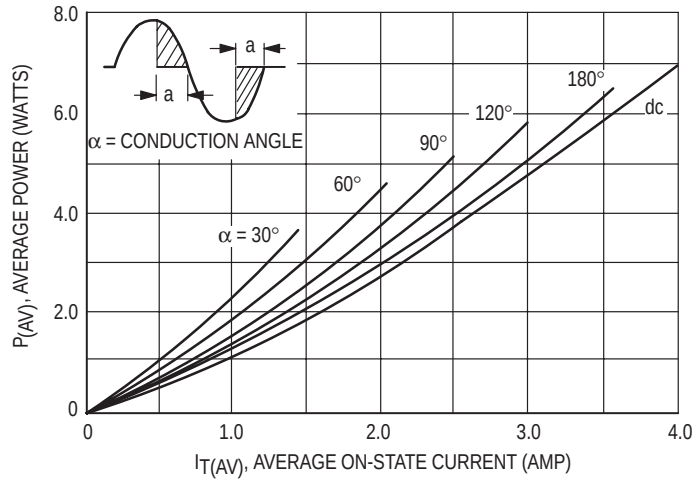


Figure 3. Power Dissipation

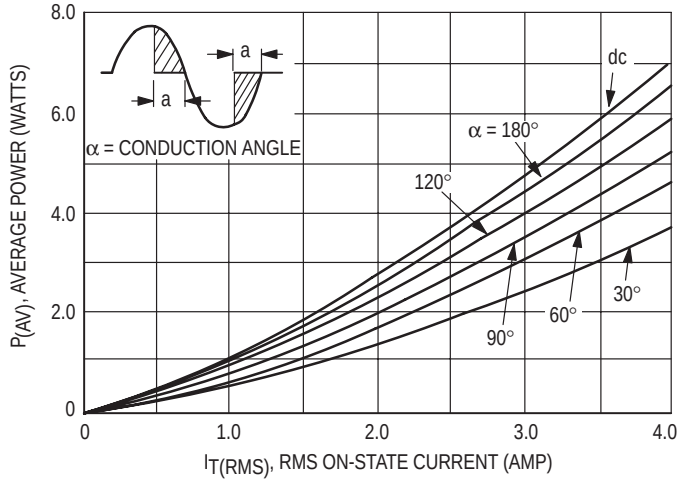


Figure 4. Power Dissipation

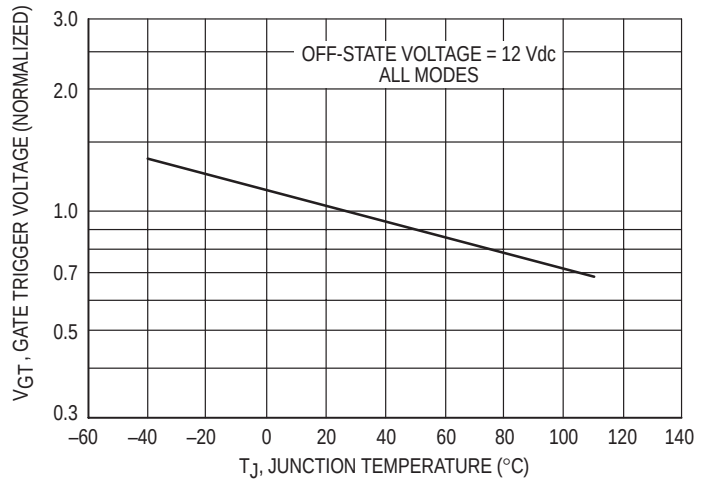


Figure 5. Typical Gate–Trigger Voltage

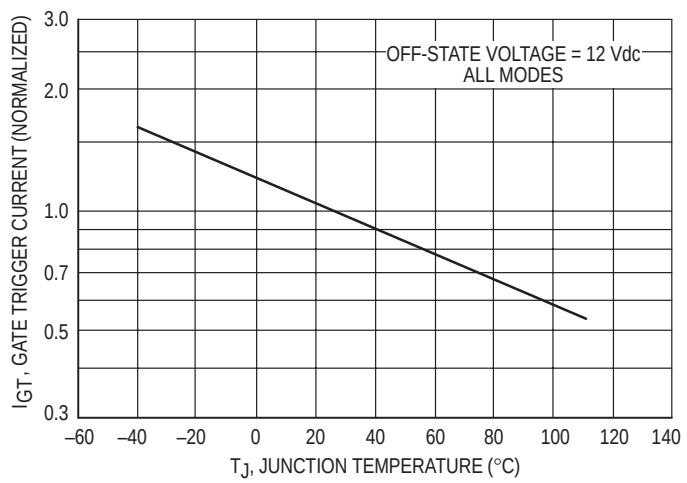


Figure 6. Typical Gate–Trigger Current

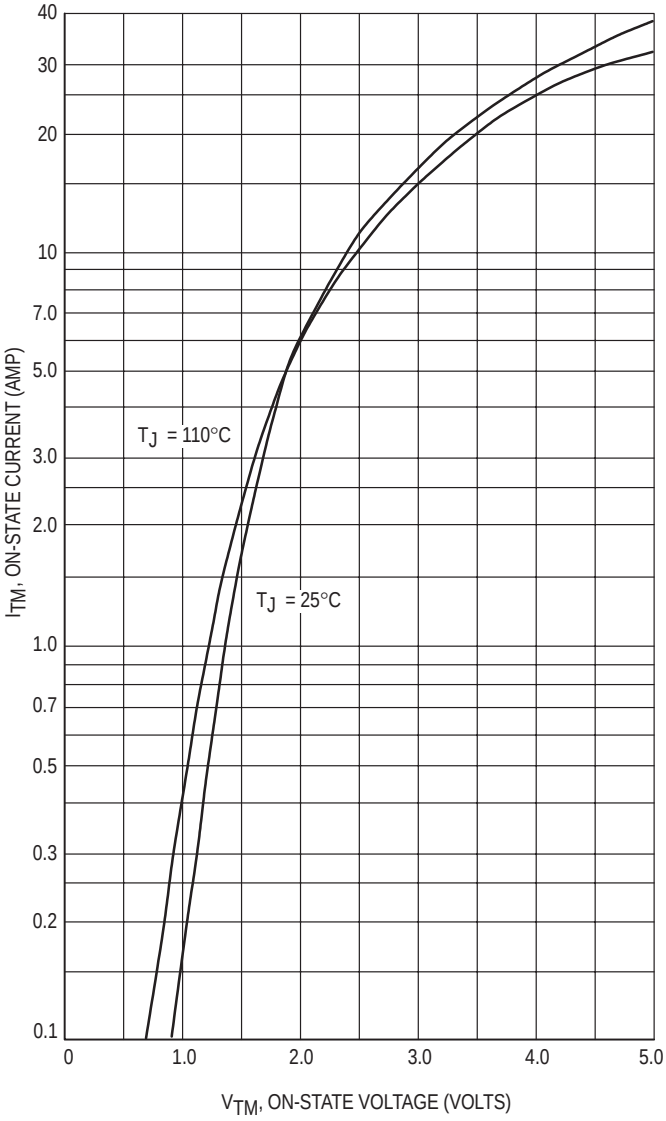


Figure 7. Maximum On–State Characteristics

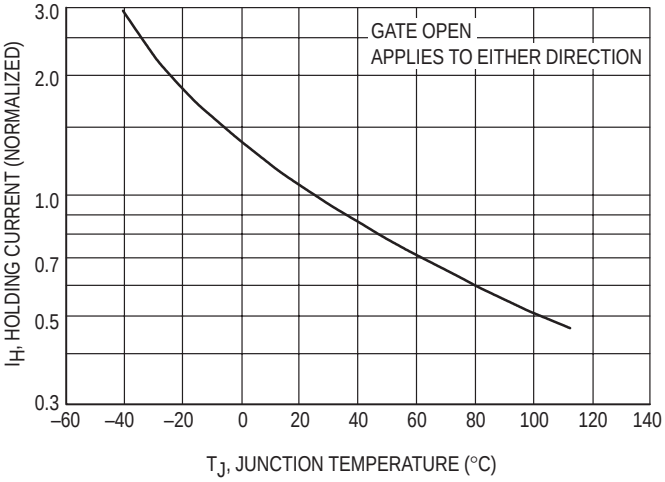


Figure 8. Typical Holding Current

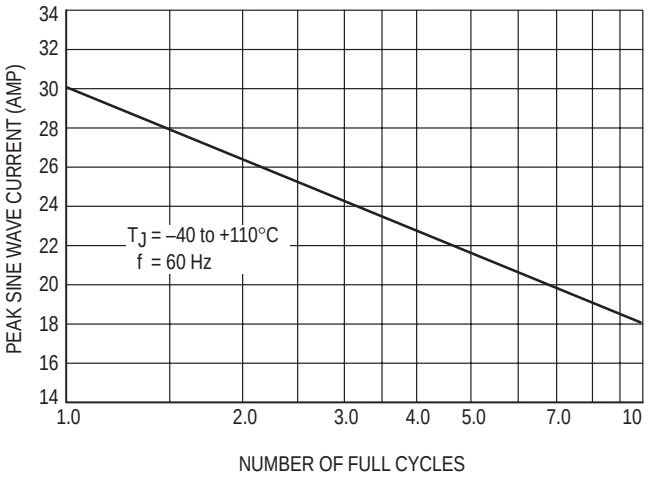


Figure 9. Maximum Allowable Surge Current

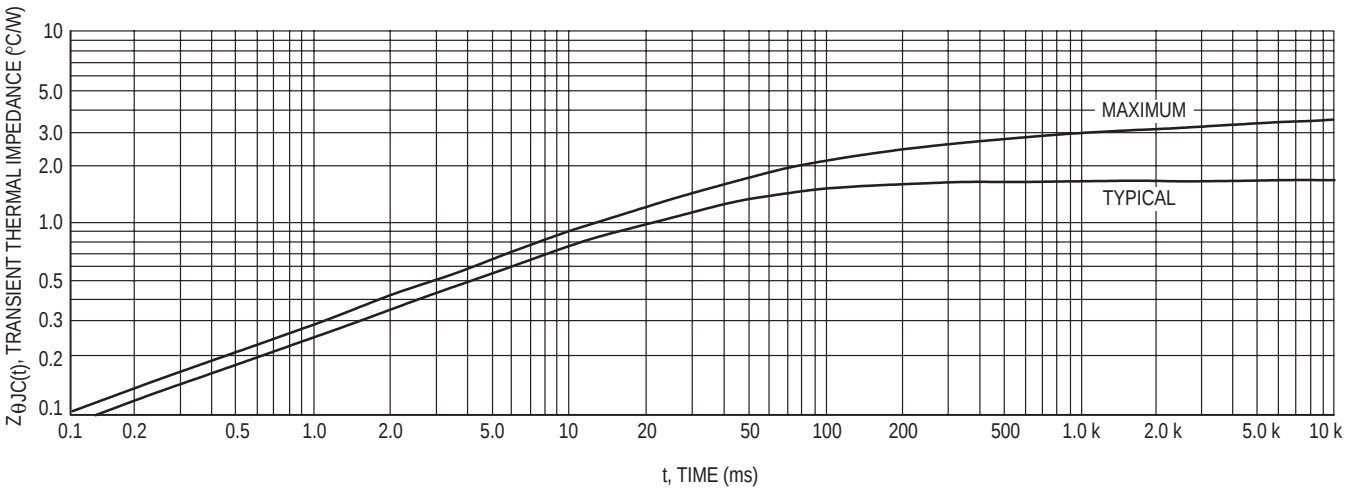
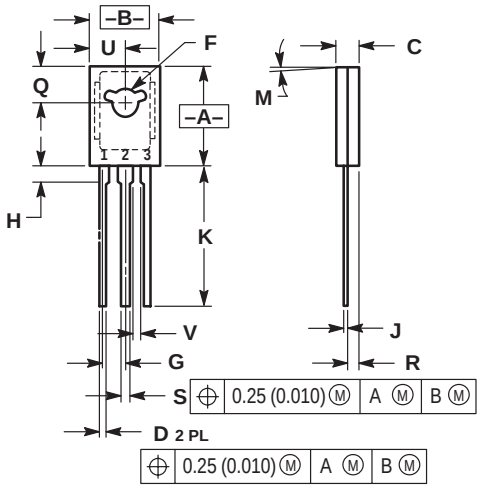


Figure 10. Thermal Response

PACKAGE DIMENSIONS

TO–225AA
(formerly TO–126)
CASE 077–09
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	—	1.02	—

STYLE 5:
PIN 1. MT 1
2. MT 2
3. GATE

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