2N6071A/B Series

Preferred Device

Sensitive Gate Triacs

Silicon Bidirectional Thyristors

Designed primarily for full-wave AC control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

Features

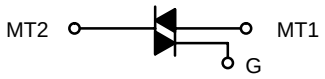
- Sensitive Gate Triggering Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions
- Gate Triggering: 4 Mode − 2N6071A, B; 2N6073A, B; 2N6075A, B
- Blocking Voltages to 600 V
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Device Marking: Device Type, e.g., 2N6071A, Date Code

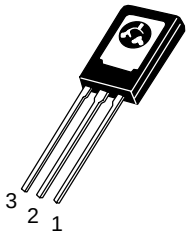
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

TRIACS
4.0 A RMS, 200 − 600 V



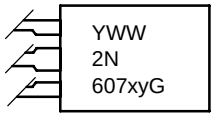


REAR VIEW SHOW TAB

TO−225
CASE 077
STYLE 5

MARKING DIAGRAM

1. Cathode
2. Anode
3. Gate



x	= 1, 3, 5
y	= A, B
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

© Semiconductor Components Industries, LLC, 2006

April, 2006 − Rev. 7

Publication Order Number:
2N6071/D

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (Note 1) (T_J = −40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open) 2N6071A,B 2N6073A,B 2N6075A,B	V_{DRM}, V_{RRM}	 200 400 600	V
*On-State RMS Current (T_C = 85°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	4.0	A
*Peak Non−repetitive Surge Current (One Full cycle, 60 Hz, T_J = +110°C)	I_{TSM}	30	A
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	3.7	A^2s
*Peak Gate Power (Pulse Width ≤ 1.0 μs, T_C = 85°C)	P_{GM}	10	W
*Average Gate Power (t = 8.3 ms, T_C = 85°C)	$P_{G(AV)}$	0.5	W
*Peak Gate Voltage (Pulse Width ≤ 1.0 μs, T_C = 85°C)	V_{GM}	5.0	V
*Operating Junction Temperature Range	T_J	−40 to +110	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
Mounting Torque (6-32 Screw) (Note 2)	−	8.0	in. lb.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.
2. Torque rating applies with use of a compression washer. Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds	T_L	260	°C

*Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted; Electricals apply in both directions)

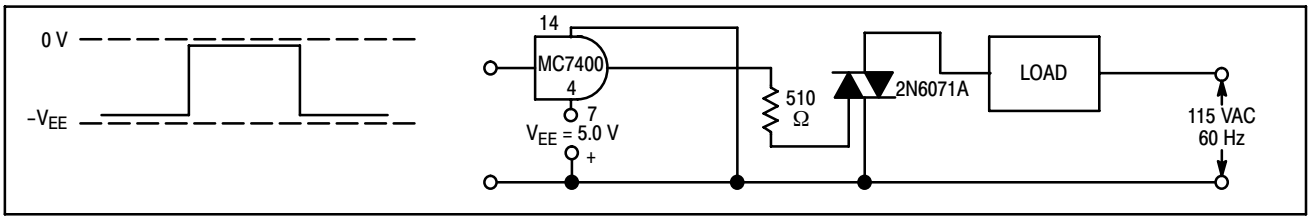
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
*Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, $V_{RRM;}$ Gate Open) T_J = 25°C	$I_{DRM,}$ I_{RRM}	–	–	10	μA
T_J = 110°C		–	–	2	mA
ON CHARACTERISTICS					
*Peak On-State Voltage (Note 3) (I_{TM} = ±6.0 A Peak)	V_{TM}	–	–	2	V
*Gate Trigger Voltage (Continuous DC), All Quadrants (Main Terminal Voltage = 12 Vdc, R_L = 100 Ω, T_J = −40°C)	V_{GT}	–	1.4	2.5	V
Gate Non−Trigger Voltage, All Quadrants (Main Terminal Voltage = 12 Vdc, R_L = 100 Ω, T_J = 110°C)	V_{GD}	0.2	–	–	V
*Holding Current (Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = ±1 Adc) T_J = −40°C	I_H	–	–	30	mA
T_J = 25°C		–	–	15	
Turn-On Time (I_{TM} = 14 Adc, I_{GT} = 100 mAdc)	t_{gt}	–	1.5	–	μs

	Type	I_{GT} @ T_J	QUADRANT (Maximum Value) I mA	II mA	III mA	IV mA
Gate Trigger Current (Continuous DC) (Main Terminal Voltage = 12 Vdc, R_L = 100 Ω)	2N6071A 2N6073A 2N6075A	+25°C	5	5	5	10
		−40°C	20	20	20	30
	2N6071B 2N6073B 2N6075B	+25°C	3	3	3	5
		−40°C	15	15	15	20

DYNAMIC CHARACTERISTICS					
Critical Rate of Rise of Commutation Voltage @ V_{DRM}, T_J = 85°C, Gate Open, I_{TM} = 5.7 A, Exponential Waveform, Commutating di/dt = 2.0 A/ms	dv/dt(c)	–	5	–	V/μs

3. Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.
*Indicates JEDEC Registered Data.

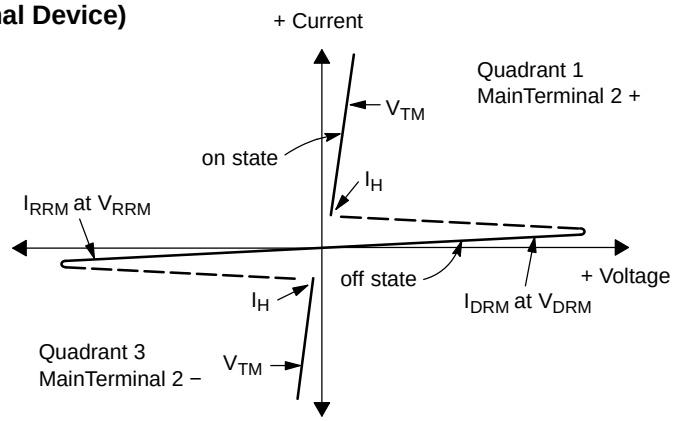
SAMPLE APPLICATION:
TTL-SENSITIVE GATE 4 AMPERE TRIAC
TRIGGERS IN MODES II AND III



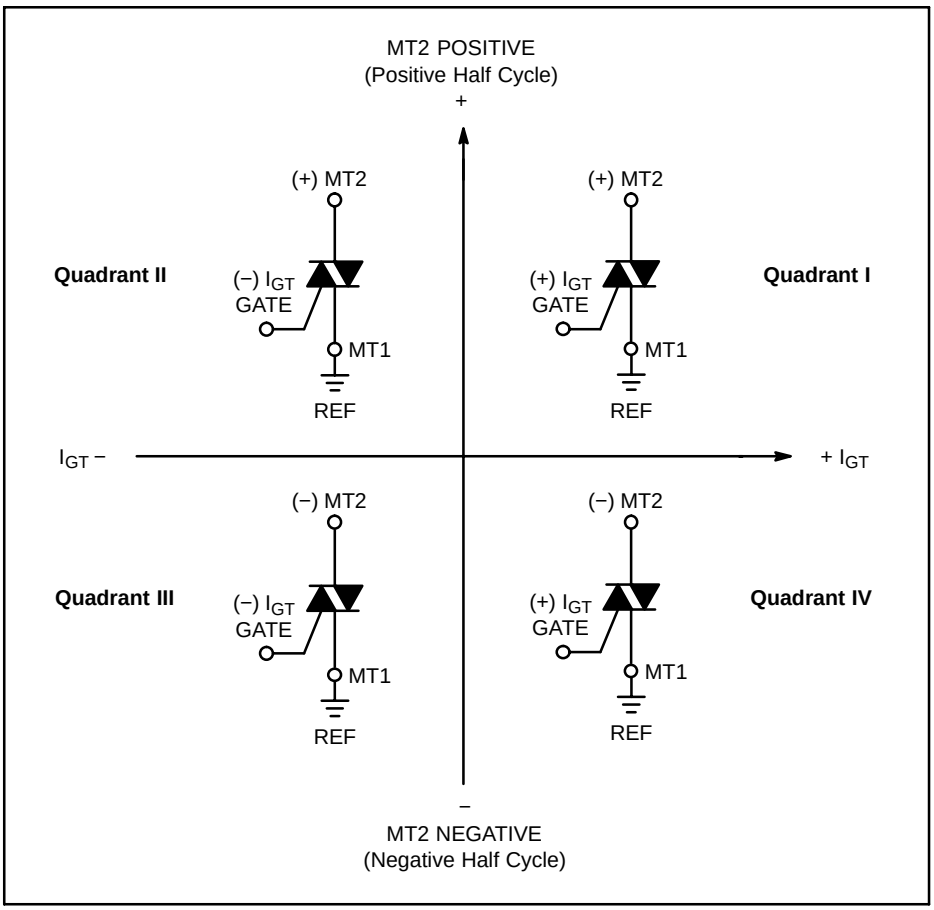
Trigger devices are recommended for gating on Triacs. They provide:
1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in−phase signals (using standard AC lines) quadrants I and III are used.

SENSITIVE GATE LOGIC REFERENCE

IC Logic Functions	Firing Quadrant			
	I	II	III	IV
TTL		2N6071A Series	2N6071A Series	
HTL		2N6071A Series	2N6071A Series	
CMOS (NAND)	2N6071B Series			2N6071B Series
CMOS (Buffer)		2N6071B Series	2N6071B Series	
Operational Amplifier	2N6071A Series			2N6071A Series
Zero Voltage Switch		2N6071A Series	2N6071A Series	

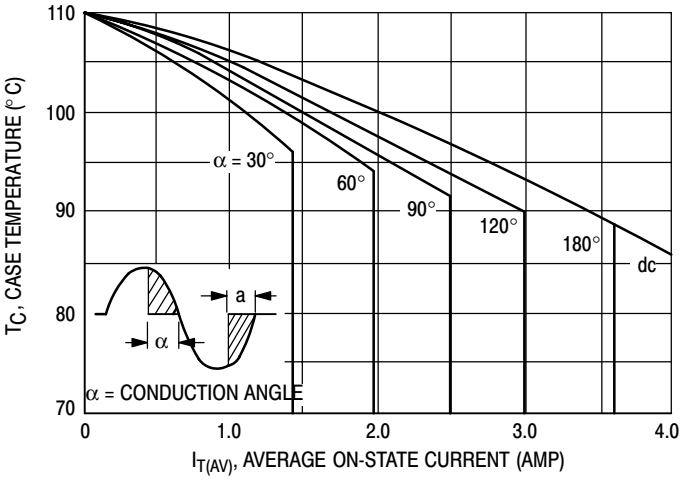


Figure 1. Average Current Derating

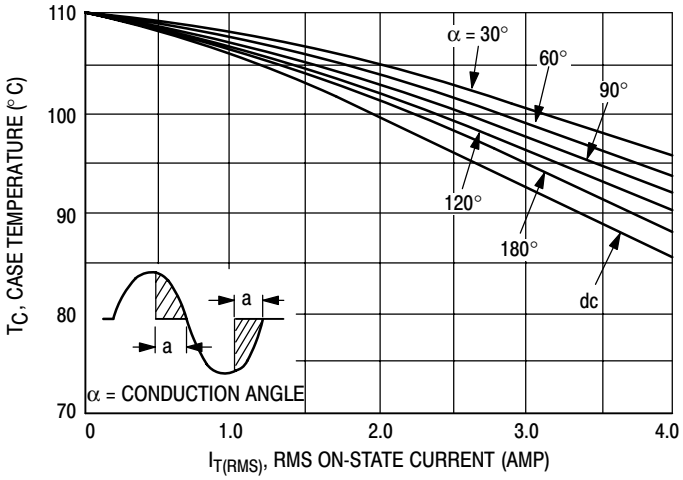


Figure 2. RMS Current Derating

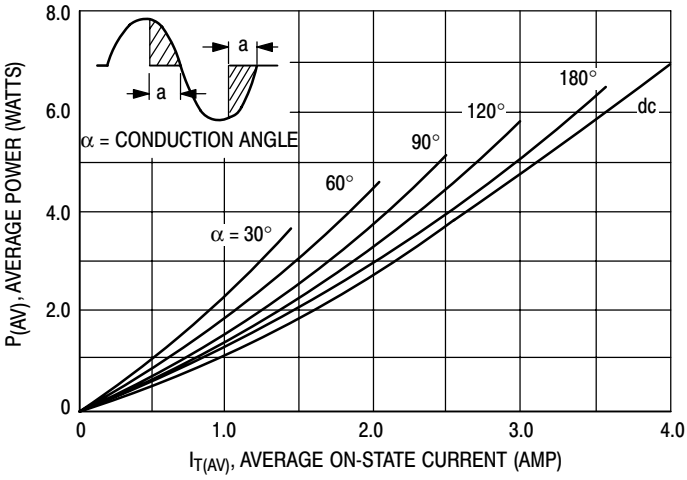


Figure 3. Power Dissipation

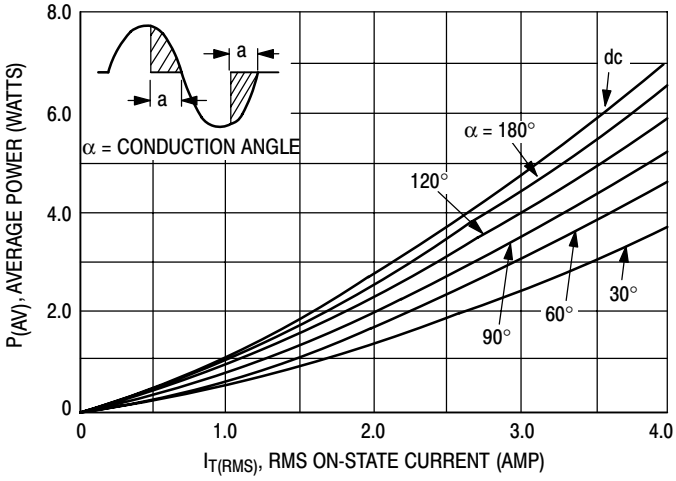


Figure 4. Power Dissipation

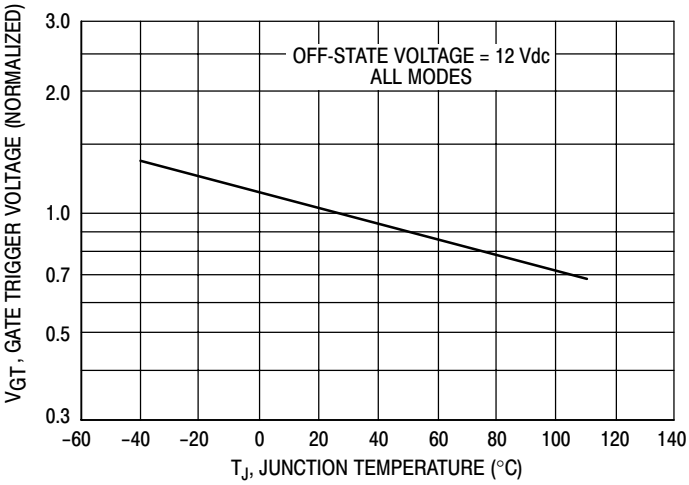


Figure 5. Typical Gate−Trigger Voltage

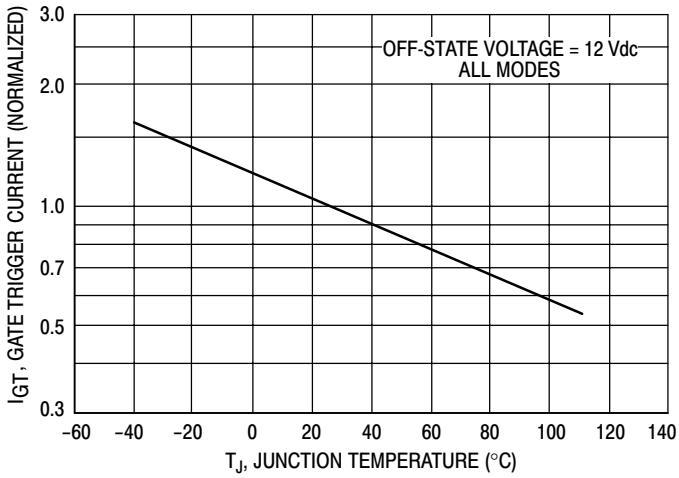


Figure 6. Typical Gate−Trigger Current

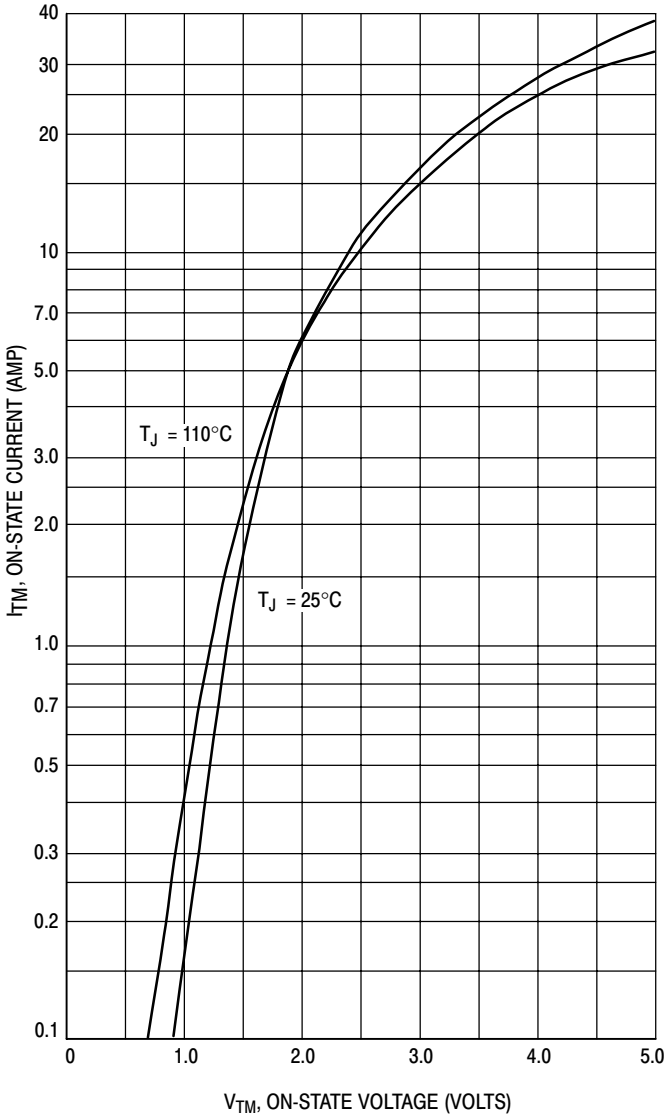


Figure 7. Maximum On−State Characteristics

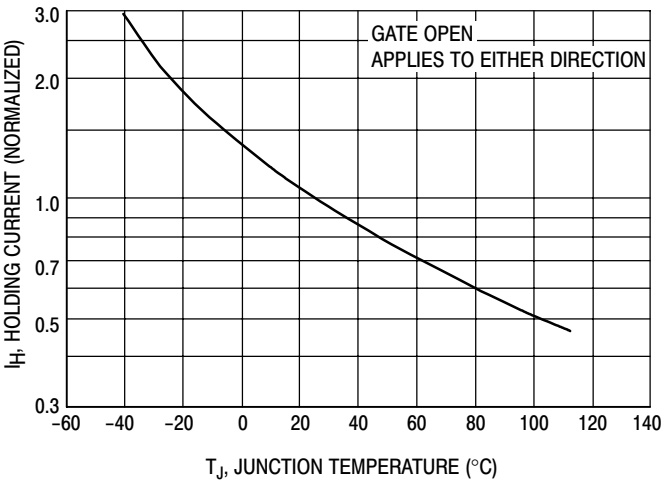


Figure 8. Typical Holding Current

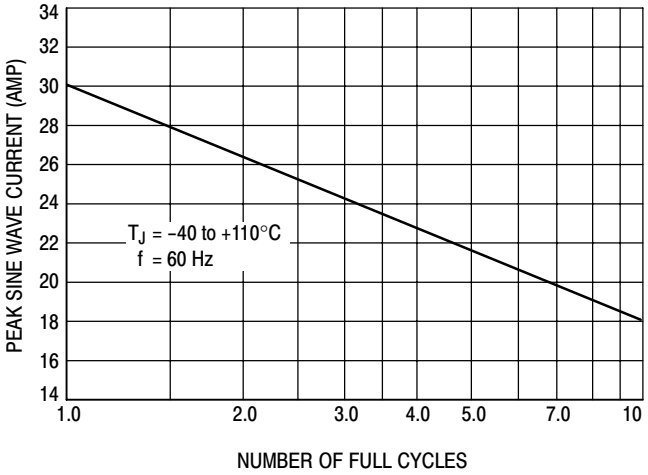


Figure 9. Maximum Allowable Surge Current

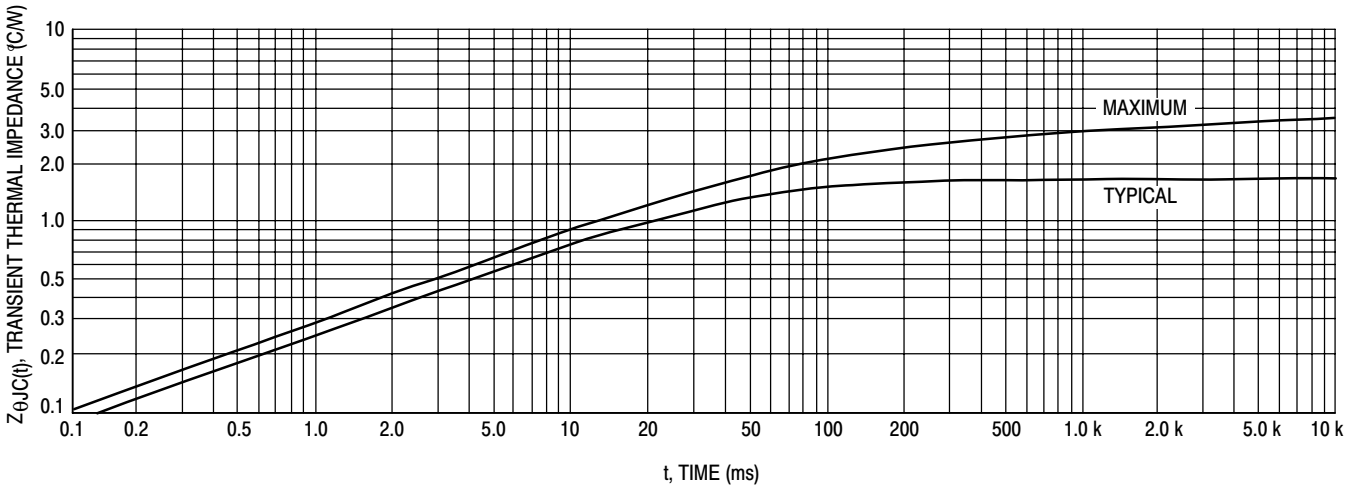


Figure 10. Thermal Response

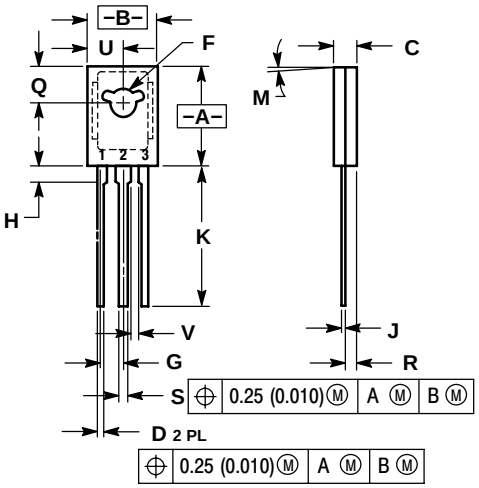
ORDERING INFORMATION

Device	Package	Shipping†
2N6071A	TO−225	500 Units / Box
2N6071AG	TO−225 (Pb−Free)	
2N6071B	TO−225	
2N6071BG	TO−225 (Pb−Free)	
2N6071BT	TO−225	
2N6071BTG	TO−225 (Pb−Free)	
2N6073A	TO−225	
2N6073AG	TO−225 (Pb−Free)	
2N6073B	TO−225	
2N6073BG	TO−225 (Pb−Free)	
2N6075A	TO−225	
2N6075AG	TO−225 (Pb−Free)	
2N6075B	TO−225	
2N6075BG	TO−225 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TO−225
CASE 77−09
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 077−01 THRU −08 OBSOLETE, NEW STANDARD 077−09.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

STYLE 5:
PIN 1. MT 1
2. MT 2
3. GATE

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.