Data Sheet November 1998 File Number 1594.2

8A, 100V, 0.180 Ohm, N-Channel Power MOSFET

The 2N6796 is an N-Channel enhancement mode silicon gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

Ordering Information

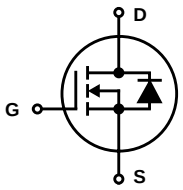
PART NUMBER	PACKAGE	BRAND
2N6796	TO-205AF	2N6796

NOTE: When ordering, use the entire part number.

Features

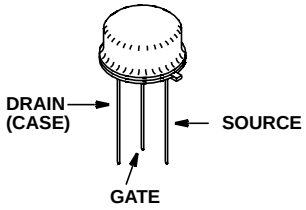
- 8A, 100V
- $r_{DS(ON)} = 0.180\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-205AF



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		2N6796	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100	V
Continuous Drain Current (Note 1)	I_D	8	A
$T_C = 100^oC$	I_D	5	A
Pulsed Drain Current (Note 1)	I_{DM}	32	A
Gate to Source Voltage (Note 1)	V_{GS}	±20	V
Continuous Source Current (Body Diode)	I_S	8	A
Pulse Source Current (Body Diode)	I_{SM}	32	A
Maximum Power Dissipation (Figure 1)	P_D	25	W
Linear Derating Factor (Figure 1)		0.20	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V	100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 0.5mA	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V	-	-	250	µA
		V_{DS} = 80V, V_{GS} = 0V, $T_C = 125^oC$	-	-	1000	µA
On-State Drain Current (Note 2)	$V_{DS(ON)}$	I_D = 8A, V_{GS} = 10V	-	-	1.56	V
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 5A, V_{GS} = 10V	-	0.14	0.180	Ω
		I_D = 5A, V_{GS} = 10V, $T_C = 125^oC$	-	-	0.350	Ω
Diode Forward Voltage (Note 2)	V_{SD}	$T_C = 25^oC$, I_S = 8A, V_{GS} = 0V	0.75	-	1.5	V
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 5V, I_D = 5A	3	5.5	9	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \cong$ 30V, I_D = 5A, R_G = 50Ω (Figure 17) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	-	30	ns
Rise Time	t_r		-	-	75	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	40	ns
Fall Time	t_f		-	-	45	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz, (Figure 11)	350	600	900	pF
Output Capacitance	C_{OSS}		150	300	500	pF
Reverse Transfer Capacitance	C_{RSS}		50	100	150	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	5	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	175	$^oC/W$
Safe Operating Area	SOA	V_{DS} = 80V, I_D = 310mA	25	-	-	W
		V_{DS} = 3.12V, I_D = 8A	25	-	-	W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, I_{SD} = 8A, dI_{SD}/dt = 100A/µs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 150^oC$, I_{SD} = 8A, dI_{SD}/dt = 100A/µs	-	1.5	-	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

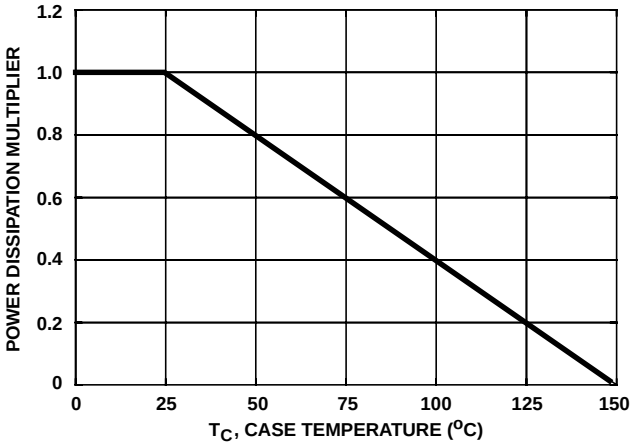


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

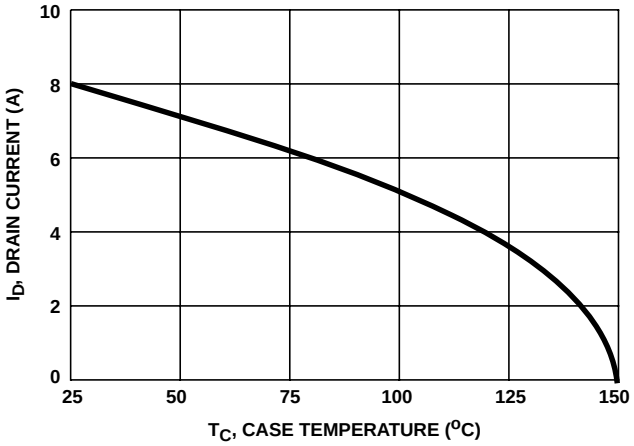


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

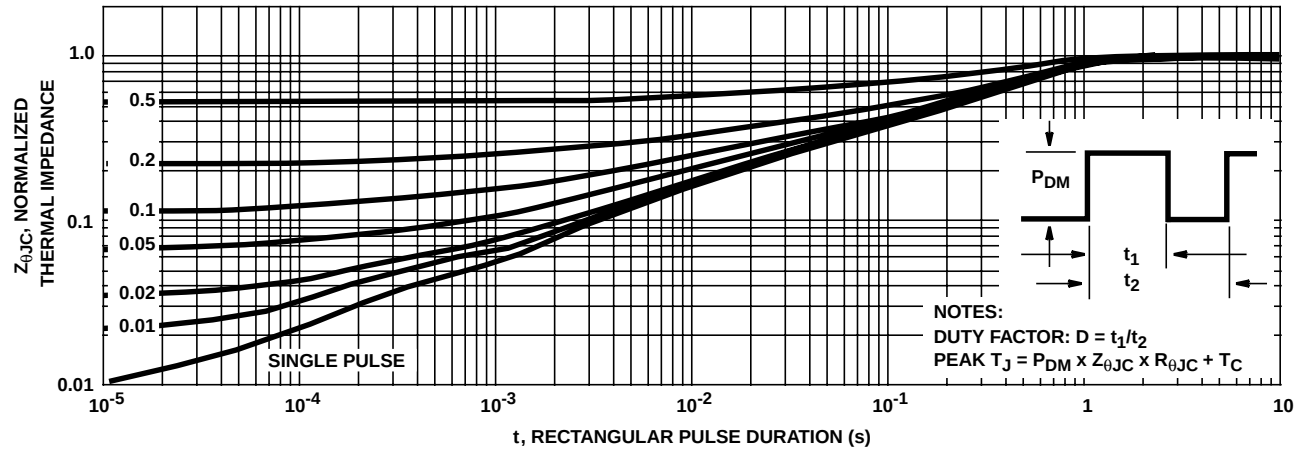


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

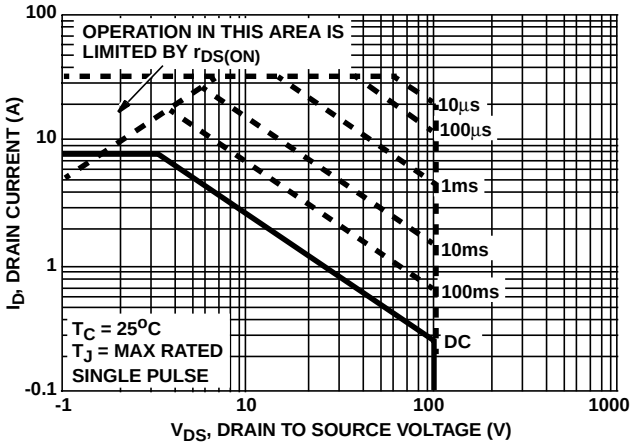


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

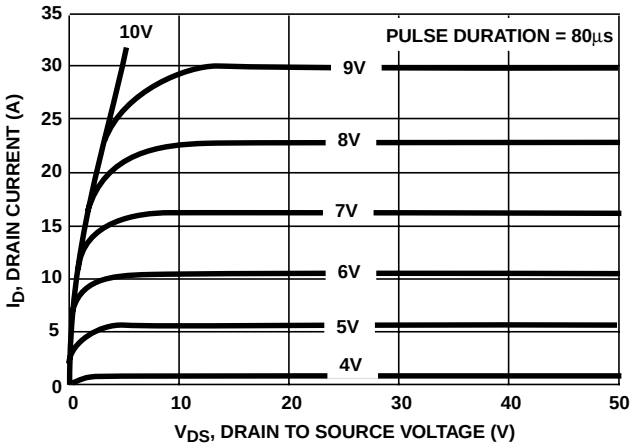


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

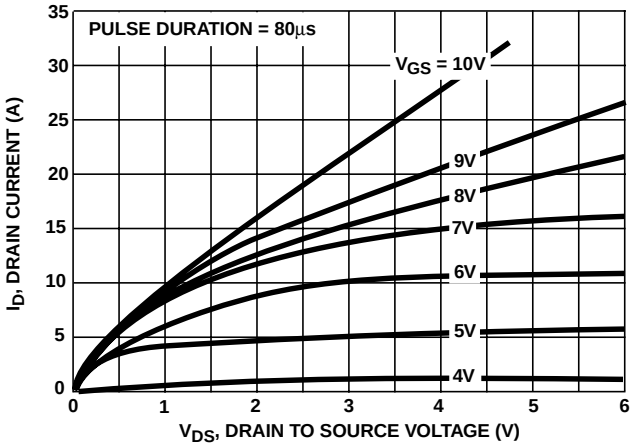


FIGURE 6. SATURATION CHARACTERISTICS

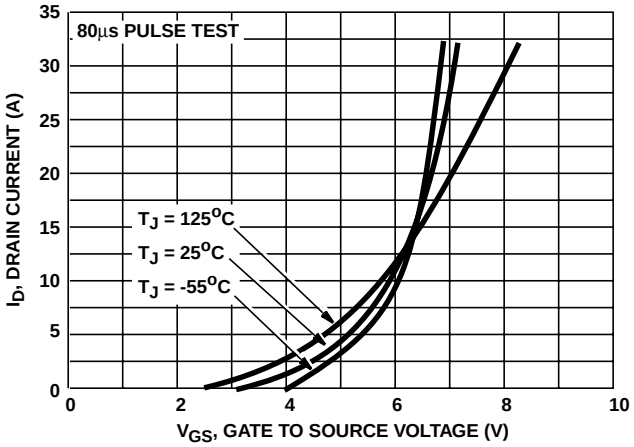
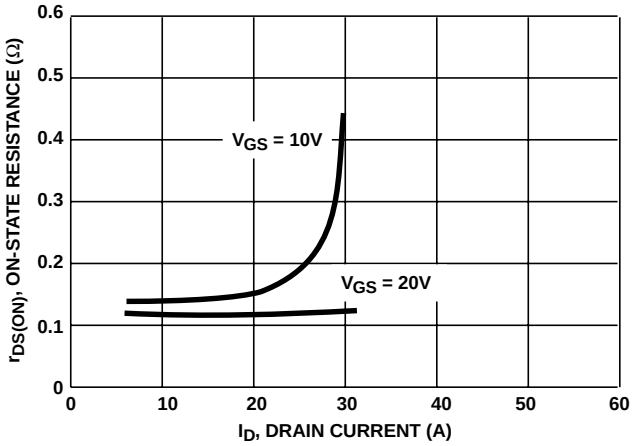


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2μs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

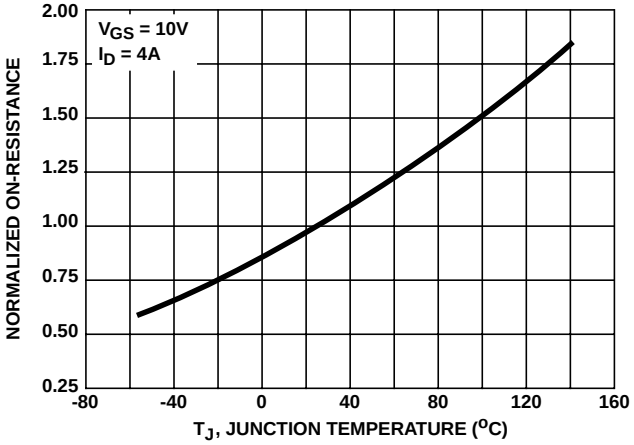


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

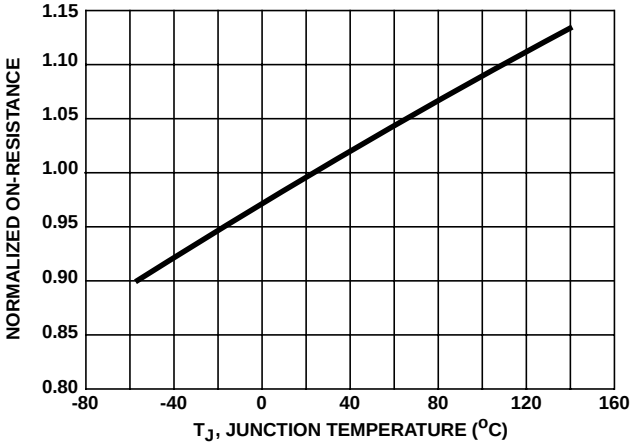


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

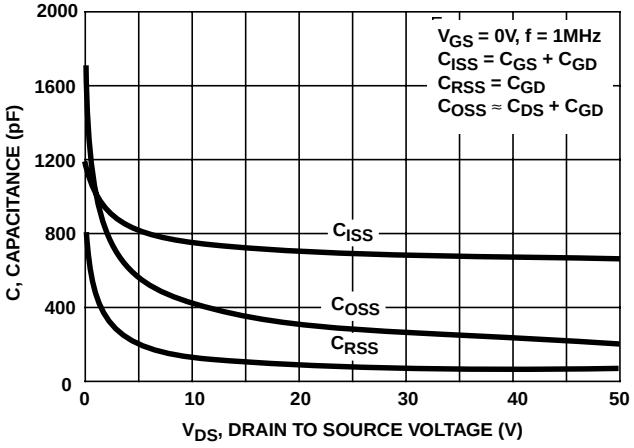


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

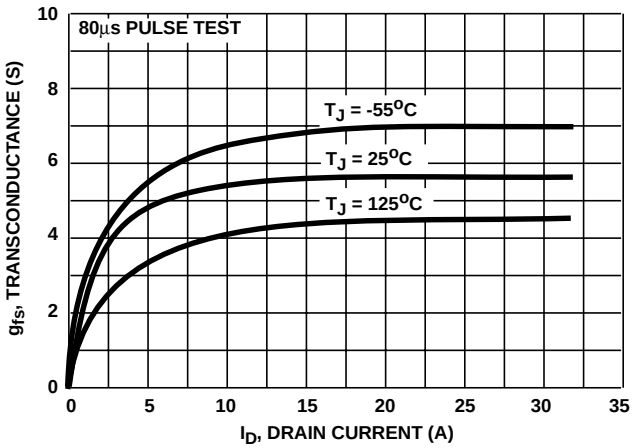


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

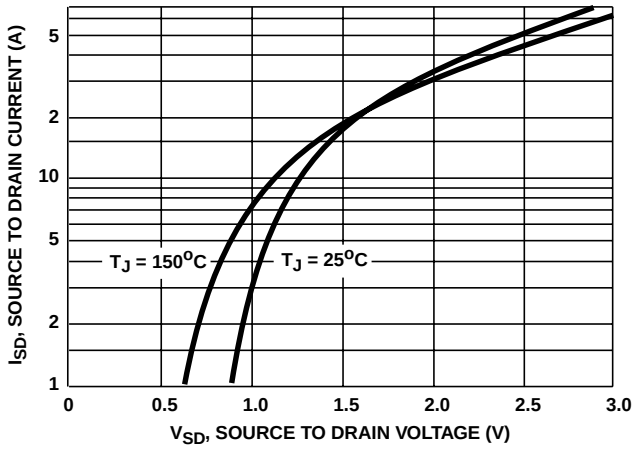


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

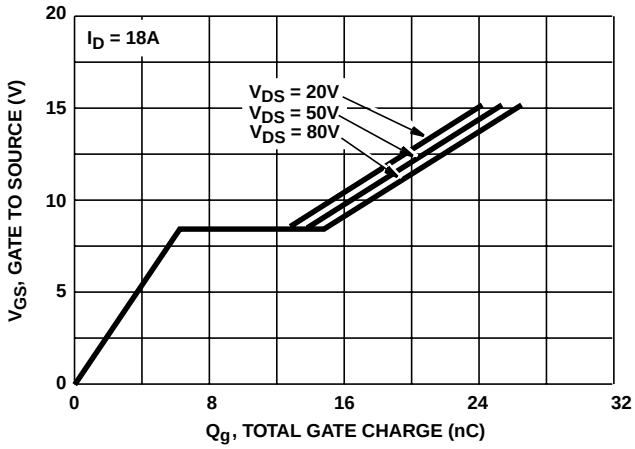


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

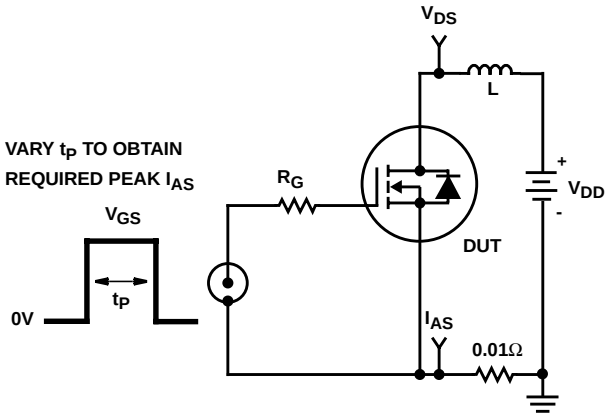


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

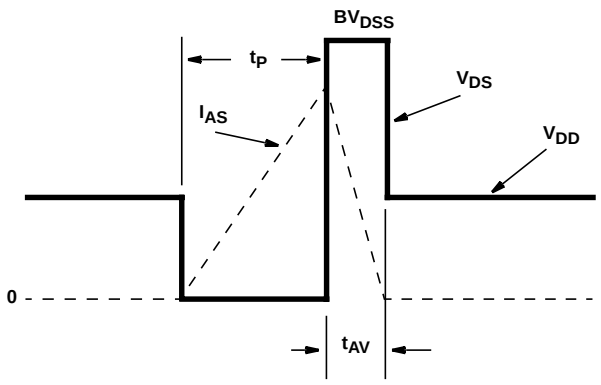


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

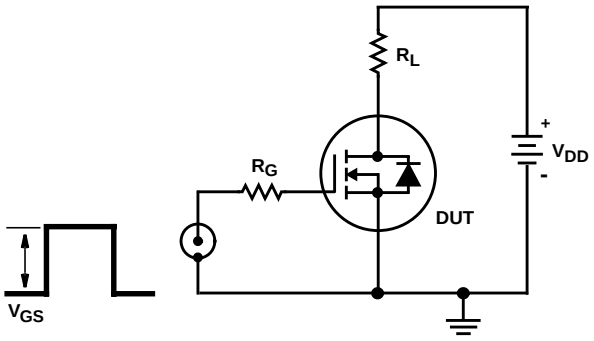


FIGURE 17. SWITCHING TIME TEST CIRCUIT

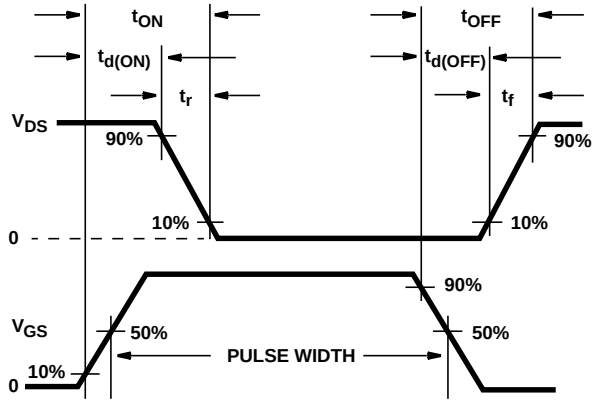


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

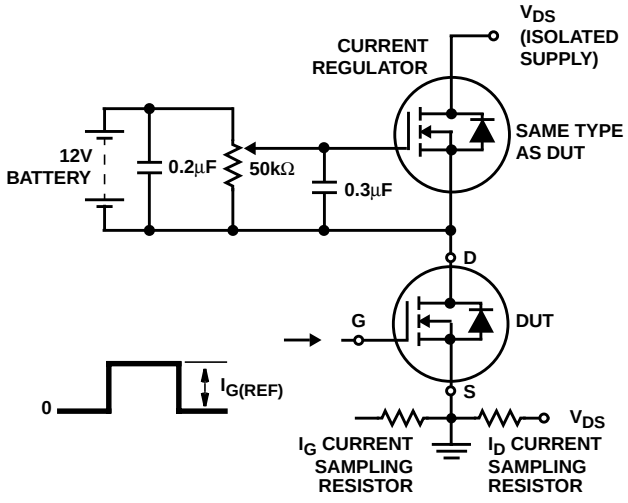


FIGURE 19. GATE CHARGE TEST CIRCUIT

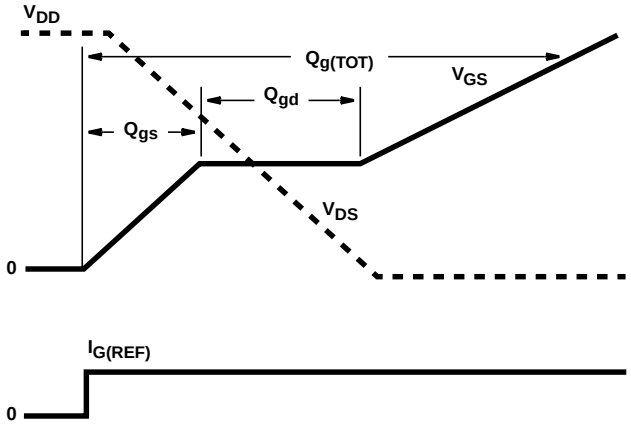
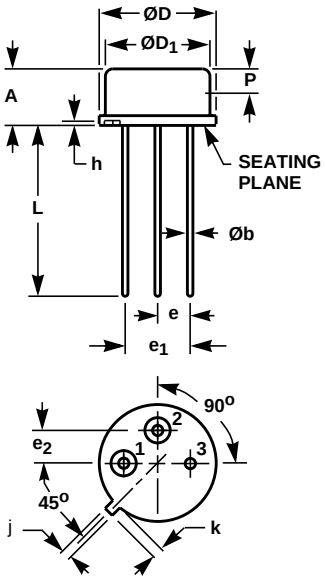


FIGURE 20. GATE CHARGE WAVEFORMS

TO-205AF

3 LEAD JEDEC TO-205AF HERMETIC METAL CAN PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.160	0.180	4.07	4.57	-
Øb	0.016	0.021	0.41	0.53	2, 3
ØD	0.350	0.370	8.89	9.39	-
$ØD_1$	0.315	0.335	8.01	8.50	-
e	0.095	0.105	2.42	2.66	4
e_1	0.190	0.210	4.83	5.33	4
e_2	0.095	0.105	2.42	2.66	4
h	0.010	0.020	0.26	0.50	-
j	0.028	0.034	0.72	0.86	-
k	0.029	0.045	0.74	1.14	-
L	0.500	0.560	12.70	14.22	3
P	0.075	-	1.91	-	5

NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC TO-205AF outline dated 11-82.
2. Lead dimension (without solder).
3. Solder coating may vary along lead length, add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.100 inches (2.54mm) from bottom of seating plane.
5. This zone controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 inches (0.254mm).
6. Lead no. 3 butt welded to stem base.
7. Controlling dimension: Inch.
8. Revision 3 dated 6-94.

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