

2N7012, 2N7013

N-Channel Enhancement Mode Transistors

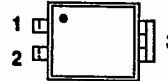
T-39-05

4-PIN DIP
(Similar to TO-250)

TOP VIEW

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
2N7012	60	0.35	1.2
2N7013	40	0.35	1.2



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		2N7012	2N7013	
Drain-Source Voltage	V_{DS}	60	40	V
Gate-Source Voltage	V_{GS}	± 20	± 20	
Continuous Drain Current	$T_A = 25^\circ\text{C}$	1.2	1.2	A
	$T_A = 100^\circ\text{C}$	0.80	0.80	
Pulsed Drain Current ¹	I_{DM}	10	10	
Power Dissipation	$T_A = 25^\circ\text{C}$	1.0	1.0	W
	$T_A = 100^\circ\text{C}$	0.4	0.4	
Operating Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$
Lead Temperature (^{1/16"} from case for 10 sec.)	T_L	300		

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	$R_{\theta JA}$		120	K/W

¹Pulse width limited by maximum junction temperature.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS		UNIT
				MIN	MAX	
STATIC						
Drain-Source Breakdown Voltage	2N7012 2N7013	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA		60 40	V
Gate Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1000 μA		2.0	4.0
Gate-Body Leakage		I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100 nA
Zero Gate Voltage Drain Current		I _{DSS}	V _{DS} = V _{(BR)DSS} , V _{GS} = 0 V			250 μA
			V _{DS} = 0.8 × V _{(BR)DSS} , V _{GS} = 0 V, T _J = 125°C			
On-State Drain Current ¹		I _{D(on)}	V _{DS} = 2 V, V _{GS} = 10 V		1.2	A
Drain-Source On-State Resistance ¹		r _{DS(on)}	V _{GS} = 10 V, I _D = 1.0 A	0.3		0.35 Ω
			V _{GS} = 10 V, I _D = 1.0 A, T _J = 125°C	0.55		0.64
Forward Transconductance ¹		g _{fs}	V _{DS} = 15 V, I _D = 1.0 A	1.5	1.2	S
DYNAMIC						
Input Capacitance		C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	220		300 pF
Output Capacitance		C _{oss}		120		200
Reverse Transfer Capacitance		C _{rss}		30		100
Total Gate Charge ²		Q _g	V _{DS} = 0.8 × V _{(BR)DSS} , V _{GS} = 10 V, I _D = 15 A	4.8		6.0 nC
Gate-Source Charge ²		Q _{gs}		1		
Gate-Drain Charge ²		Q _{gd}		2		
Turn-On Delay Time ²		t _{d(on)}	V _{DD} = 30 V, R _L = 25 Ω I _D ≈ 1.2 A, V _{GEN} = 10 V, R _G = 25 Ω	7		20 ns
Rise Time ²		t _r		13		30
Turn-Off Delay Time ²		t _{d(off)}		18		30
Fall Time ²		t _f		13		25
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_A = 25°C)						
Continuous Current		I _S				1.2 A
Pulsed Current ³		I _{SM}				10
Forward Voltage ¹		V _{SD}	I _F = I _S , V _{GS} = 0 V			1.6 V
Reverse Recovery Time		t _{rr}	I _F = I _S , di _F /dt = 100 A/μs	45		ns
Reverse Recovery Charge		Q _{rr}		0.6		μC

¹Pulse test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

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Figure 1. Output Characteristics

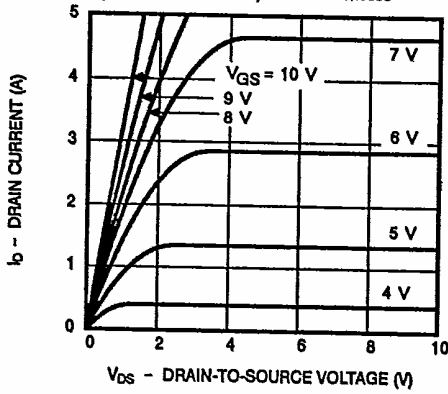


Figure 2. Transfer Characteristics

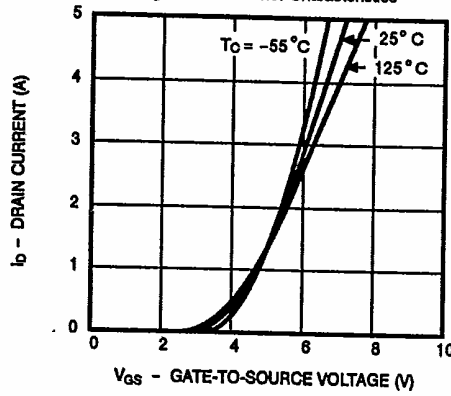


Figure 3. Transconductance

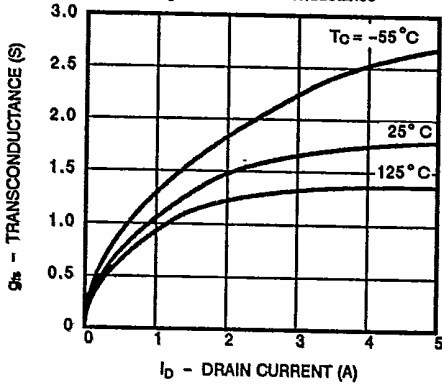
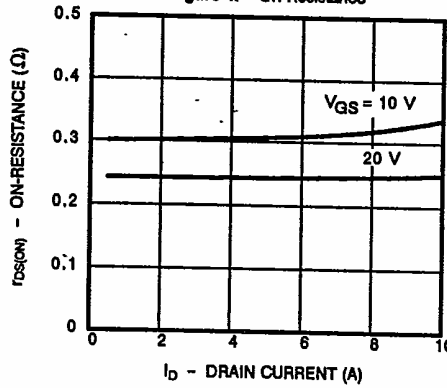


Figure 4. On-Resistance



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Figure 5. Capacitance

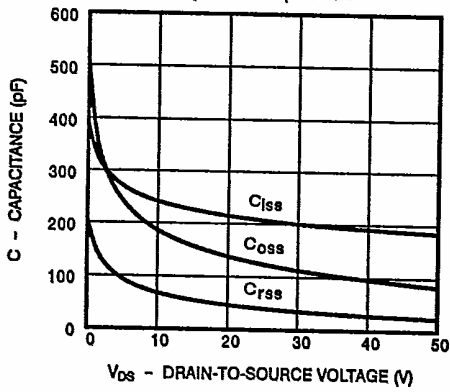
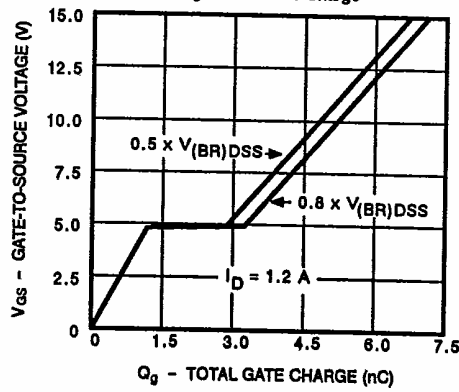


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

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Figure 7. On-Resistance vs. Junction Temperature

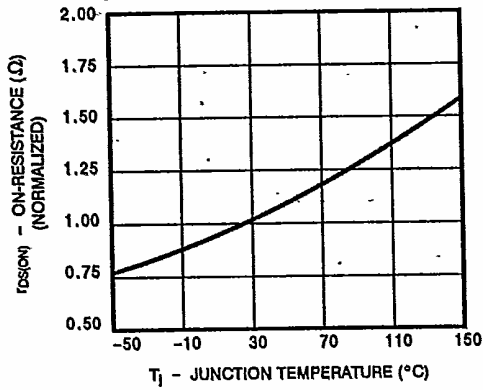
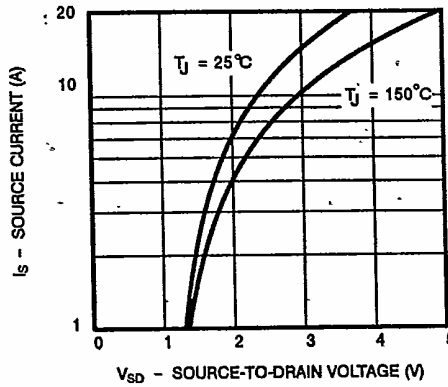


Figure 8: Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Ambient Temperature

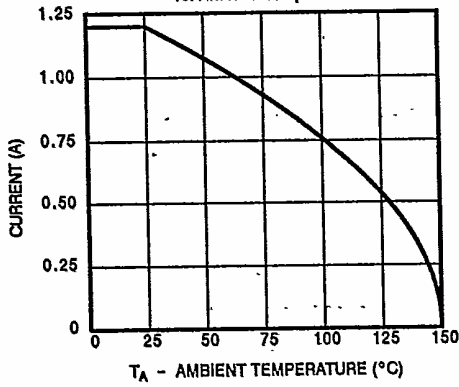


Figure 10. Safe Operating Area

