

# 2SJ518

Silicon P Channel MOS FET  
High Speed Power Switching

# HITACHI

ADE-208-580B (Z)

3rd. Edition

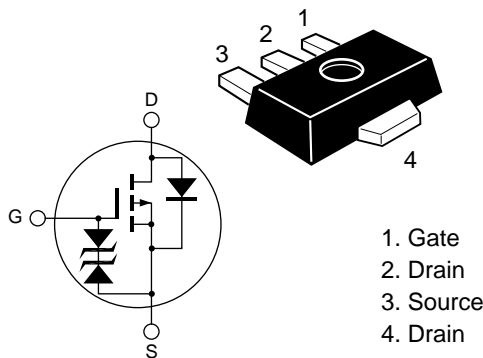
Jun 1998

## Features

- Low on-resistance  
 $R_{DS(on)} = 0.35 \Omega$  typ. at ( $V_{GS} = -10V, I_D = -1A$ )
- Low drive current
- 4 V gate drive devices
- High speed switching

## Outline

UPAK



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-60	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	-2	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	-4	A
Body-drain diode reverse drain current	$I_{DR}$	-2	A
Avalanche current	$I_{AP}$ <sup>Note2</sup>	-2	A
Avalanche energy	$E_{AR}$	0.34	mJ
Channel dissipation	$P_{ch}$ <sup>Note3</sup>	1	W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

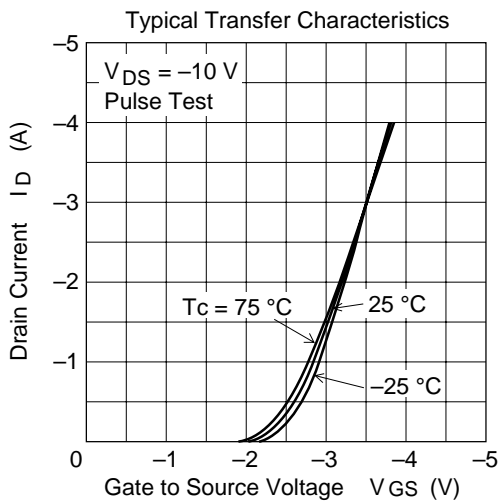
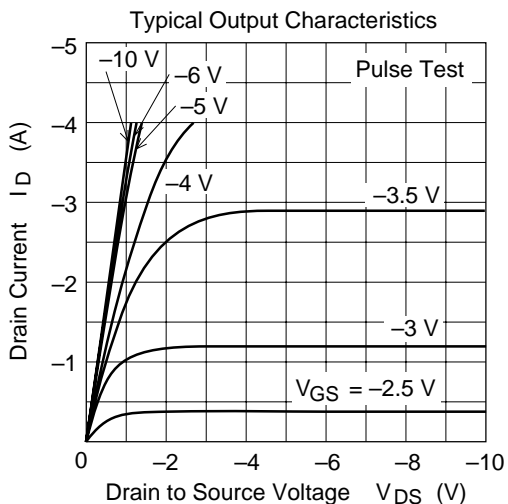
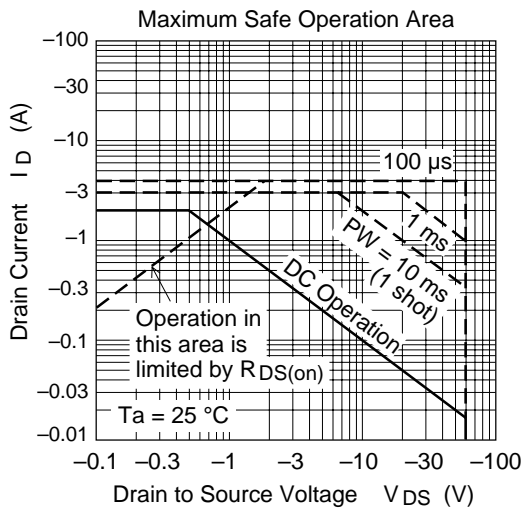
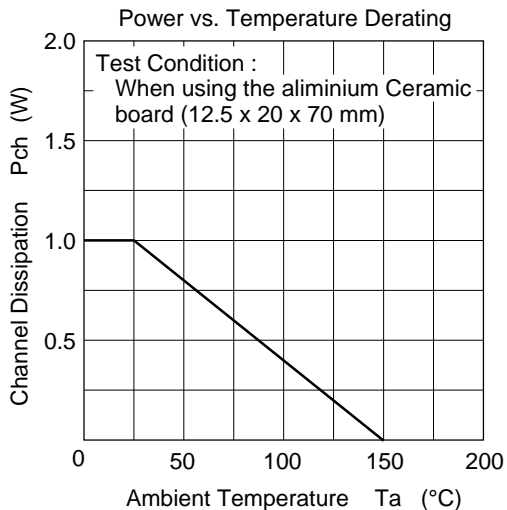
Note: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$   
 2. value at  $T_{ch} = 25^\circ C$ ,  $R_g \geq 50 \Omega$   
 3. Value at when using the aluminaceramic board (12.5x20x0.7mm)

## Electrical Characteristics (Ta = 25°C)

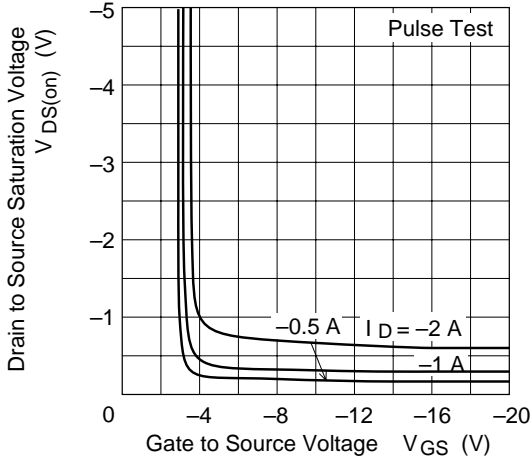
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10mA$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100\mu A$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-10	μA	$V_{DS} = -60V$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = \pm 16V$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1mA$ , $V_{DS} = -10V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.35	0.46	Ω	$I_D = -1A$ , $V_{GS} = -10V$ <sup>Note4</sup>
	$R_{DS(on)}$	—	0.45	0.63	Ω	$I_D = -1A$ , $V_{GS} = -4V$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	1.2	2.0	—	S	$I_D = -1A$ , $V_{DS} = -10V$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	220	—	pF	$V_{DS} = -10V$
Output capacitance	$C_{oss}$	—	110	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	35	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$V_{GS} = -10V$ , $I_D = -1A$
Rise time	$t_r$	—	11	—	ns	$R_L = 30\Omega$
Turn-off delay time	$t_{d(off)}$	—	45	—	ns	
Fall time	$t_f$	—	30	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	-1.05	—	V	$I_D = -2A$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	50	—	ns	$I_F = -2A$ , $V_{GS} = 0$ $diF/dt = 50A/\mu s$

Note: 4. Pulse test  
 5. Marking is "AZ"

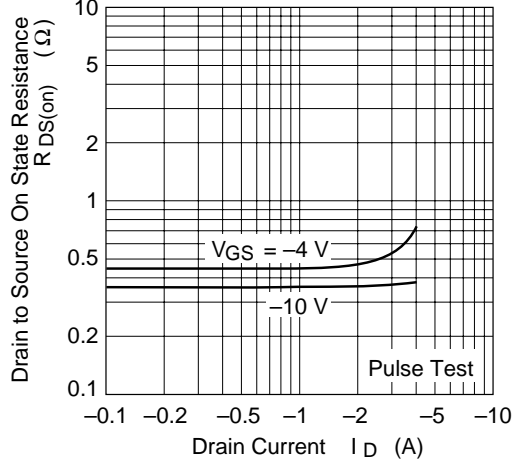
Main Characteristics



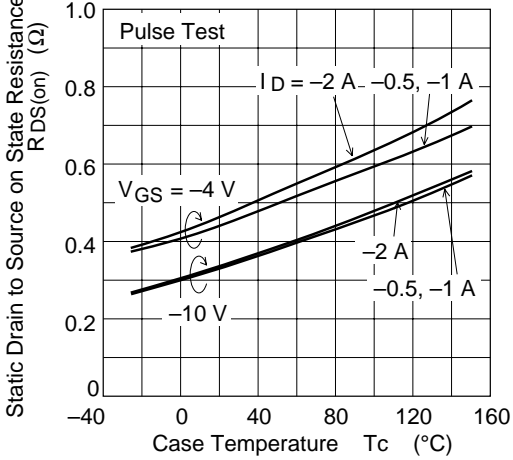
Drain to Source Saturation Voltage vs. Gate to Source Voltage



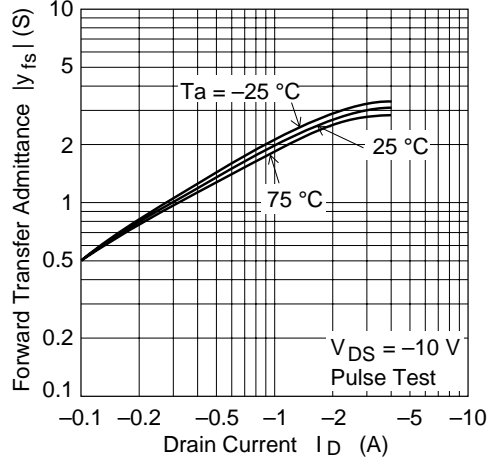
Static Drain to Source on State Resistance vs. Drain Current



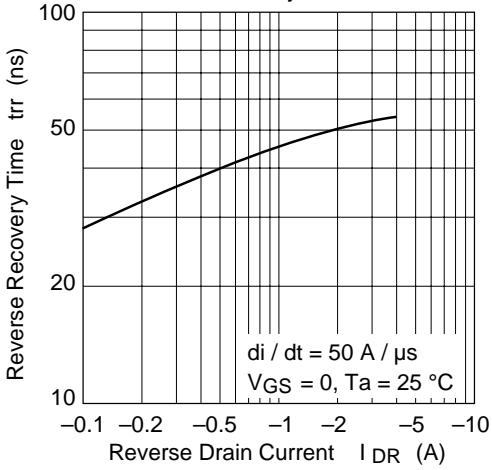
Static Drain to Source on State Resistance vs. Temperature



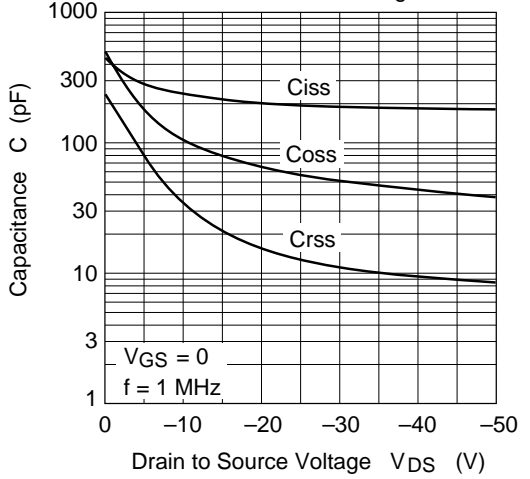
Forward Transfer Admittance vs. Drain Current



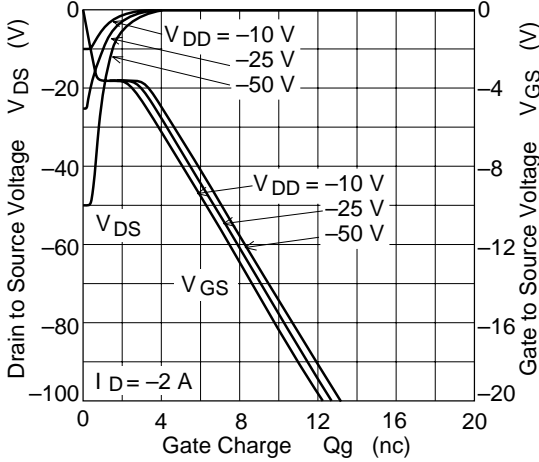
Body-Drain Diode Reverse Recovery Time



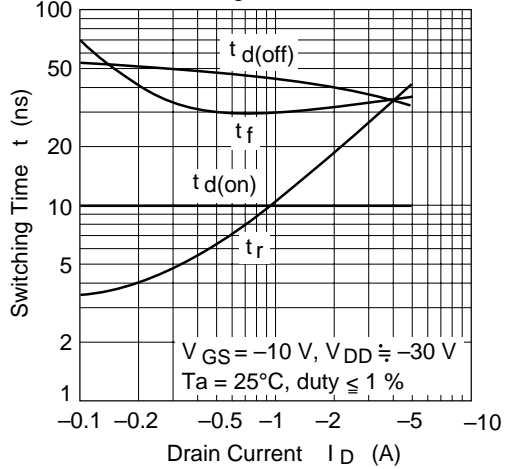
Typical Capacitance vs. Drain to Source Voltage

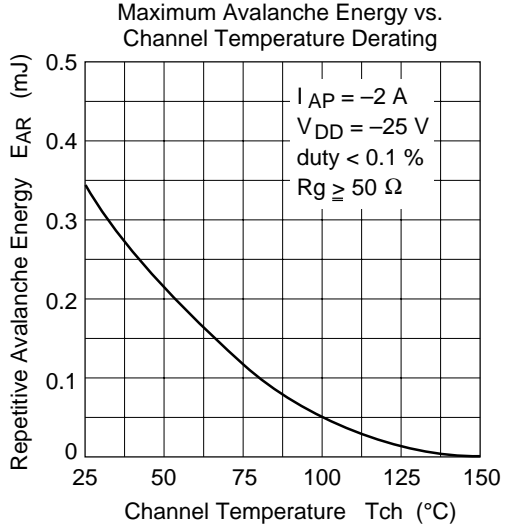
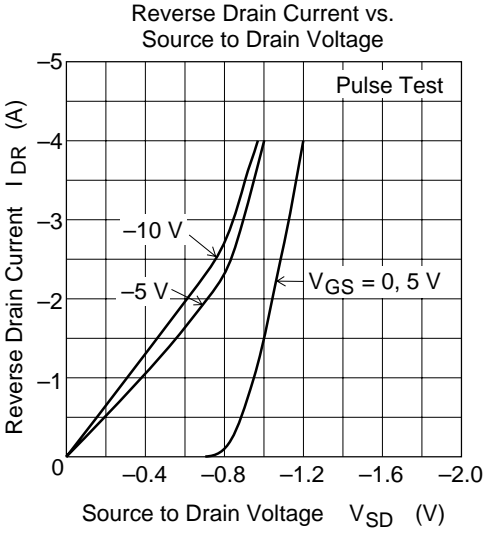


Dynamic Input Characteristics

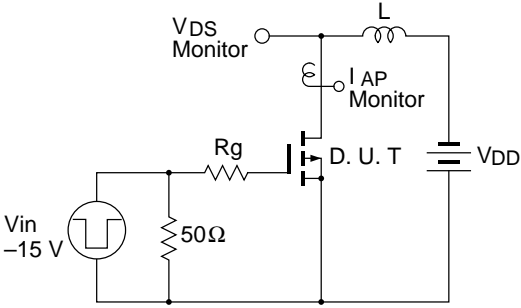


Switching Characteristics



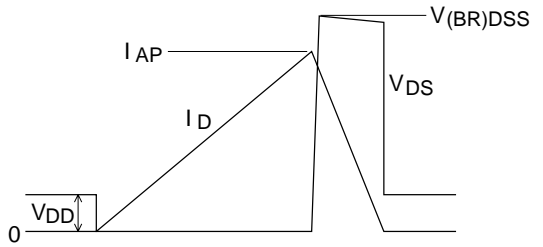


Avalanche Test Circuit

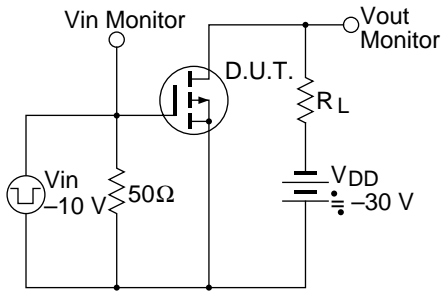


Avalanche Waveform

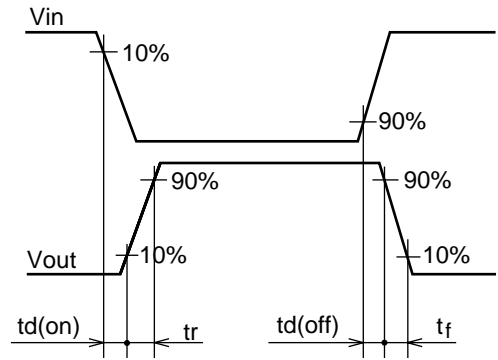
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

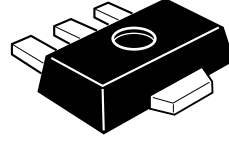
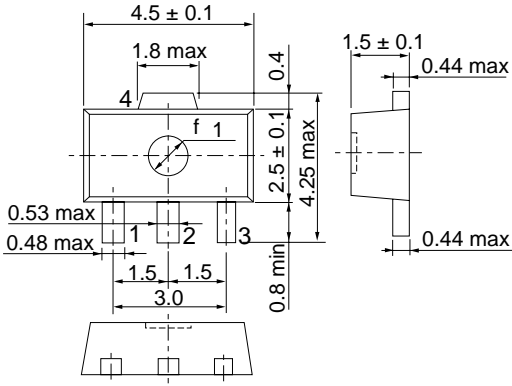


Waveform



## Package Dimensions

Unit: mm



Hitachi Code	UPAK
EIAJ	SC-62
JEDEC	UPAK



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