

2SK2203

Silicon N-Channel MOS FET

HITACHI

ADE-208-139
1st. Edition

Application

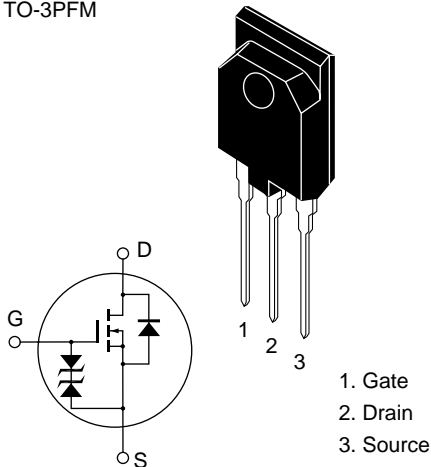
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC-DC converter

Outline

TO-3PFM



Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

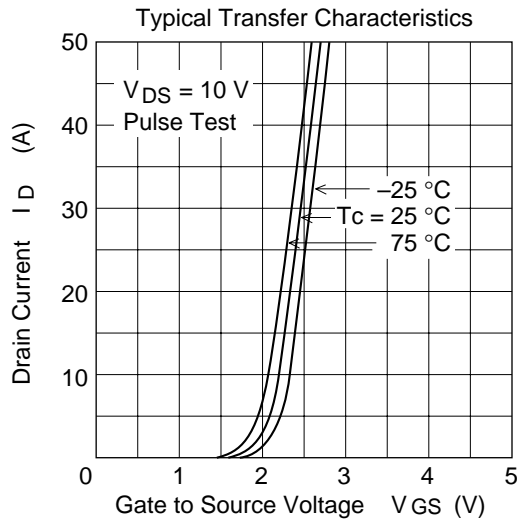
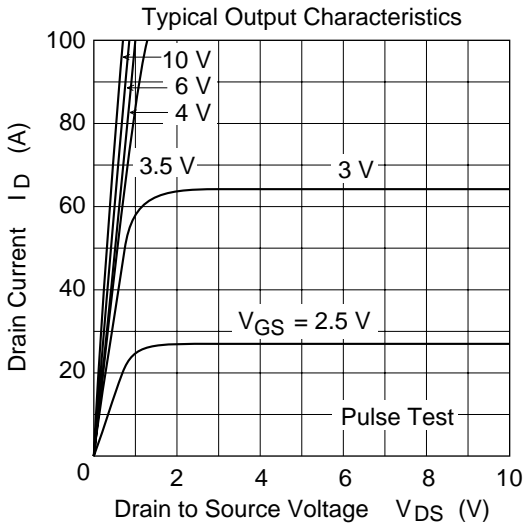
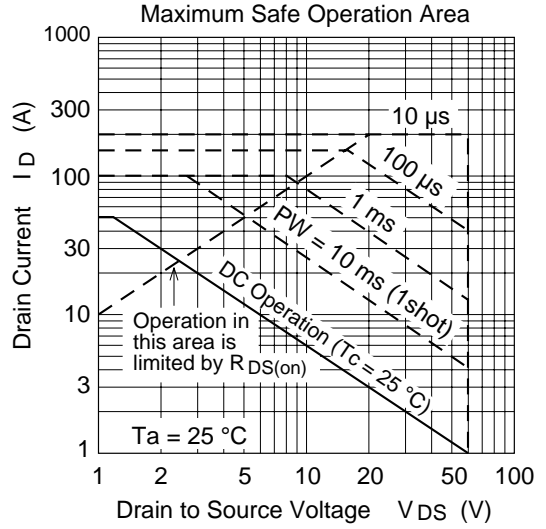
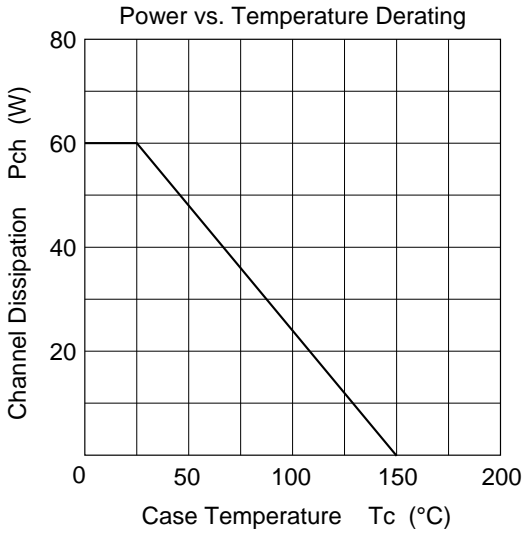
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}^{*1}$	200	A
Body to drain diode reverse drain current	I_{DR}	50	A
Avalanche current	I_{AP}^{*3}	50	A
Avalanche energy	E_{AR}^{*3}	214	mJ
Channel dissipation	P_{ch}^{*2}	60	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes
1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1 \%$
 2. Value at $T_c = 25^\circ\text{C}$
 3. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

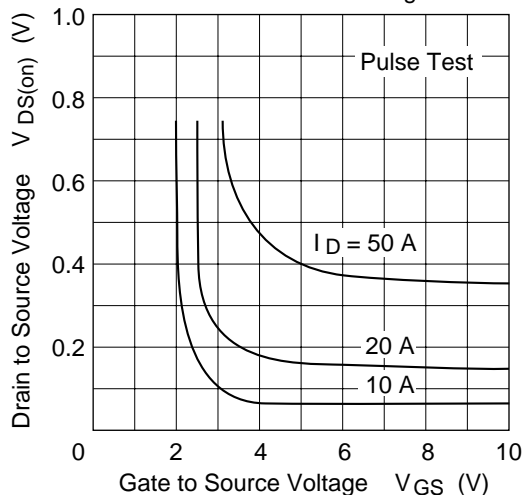
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.007	0.01	Ω	$I_D = 25 \text{ A}$ $V_{GS} = 10 \text{ V}^{*1}$
		—	0.009	0.013	Ω	$I_D = 25 \text{ A}$ $V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	40	65	—	S	$I_D = 25 \text{ A}$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	8330	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	3500	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	550	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	50	—	ns	$I_D = 25 \text{ A}$
Rise time	t_r	—	270	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	1400	—	ns	$R_L = 1.2 \text{ }\Omega$
Fall time	t_f	—	560	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.95	—	V	$I_F = 50 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	150	—	ns	$I_F = 50 \text{ A}$, $V_{GS} = 0$, $di_F / dt = 50 \text{ A} / \mu\text{s}$

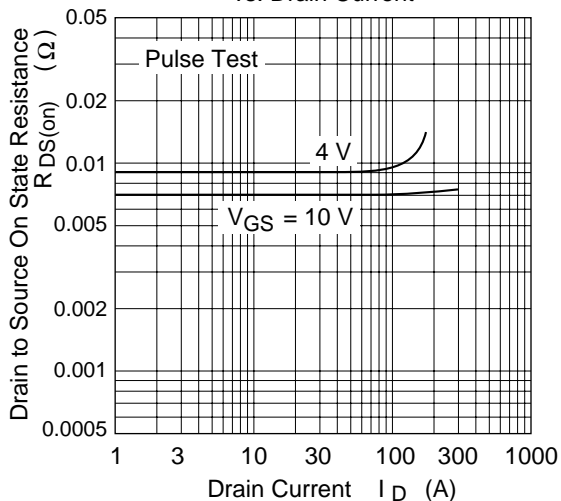
Note 1. Pulse Test



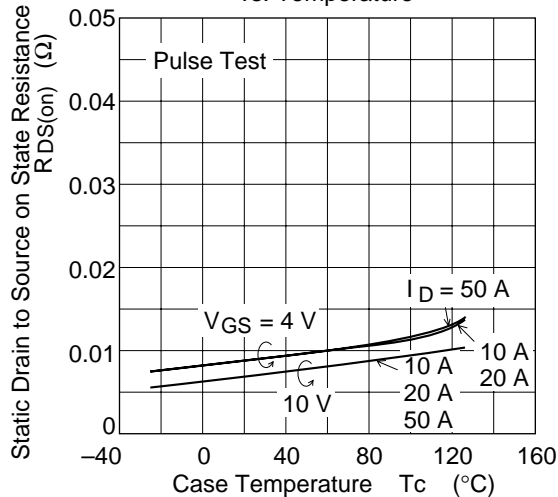
Drain to Source Saturation Voltage vs. Gate to Source Voltage



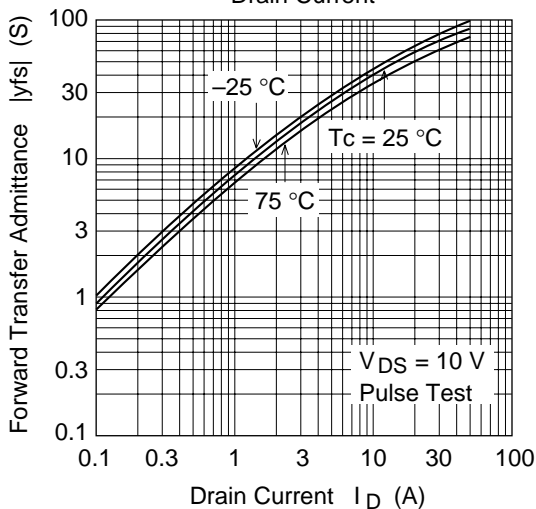
Static Drain to Source State Resistance vs. Drain Current

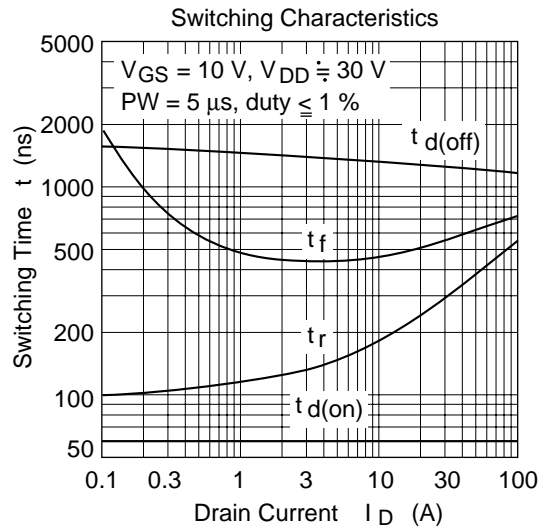
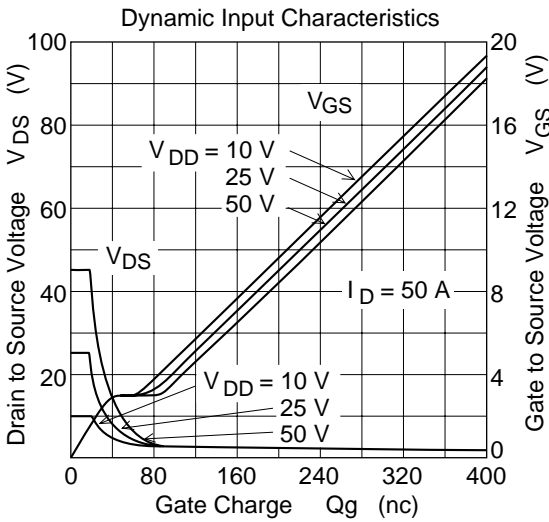
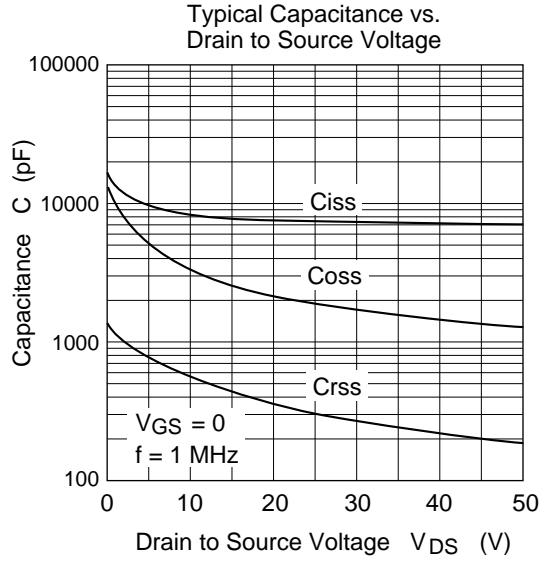
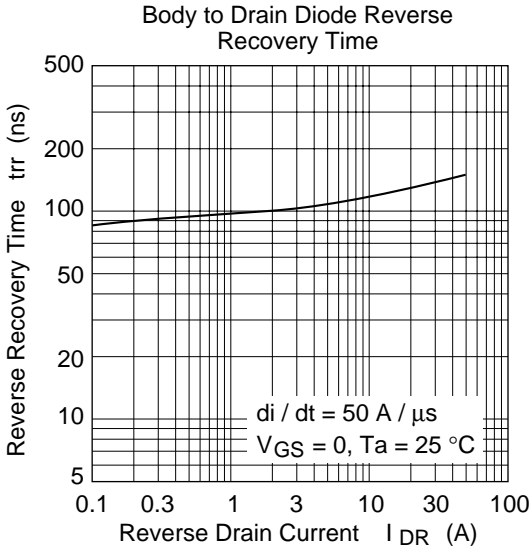


Static Drain to Source on State Resistance vs. Temperature

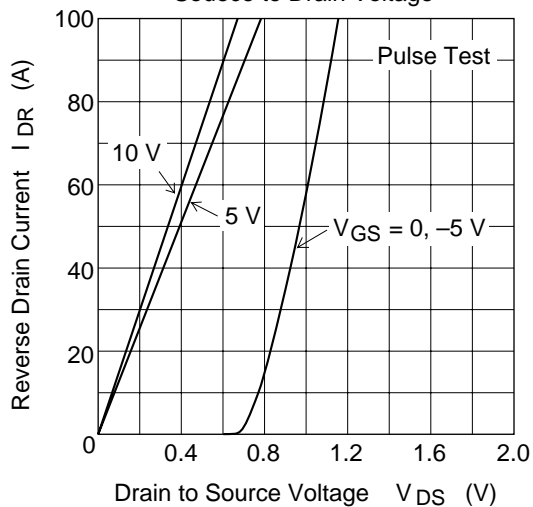


Forward Transfer Admittance vs. Drain Current

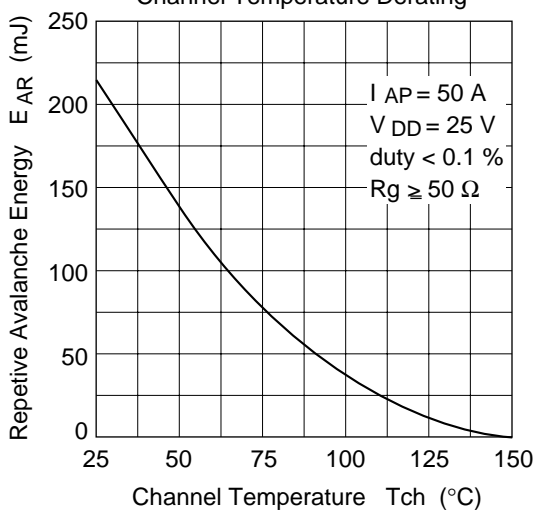




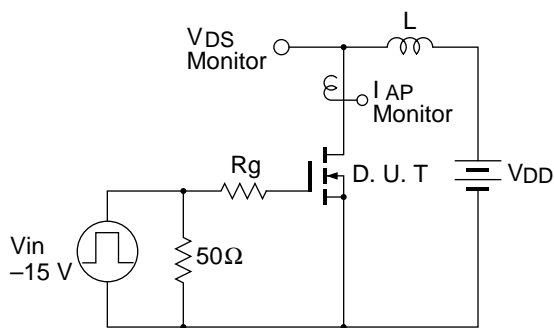
Reverse Drain Current vs. Source to Drain Voltage



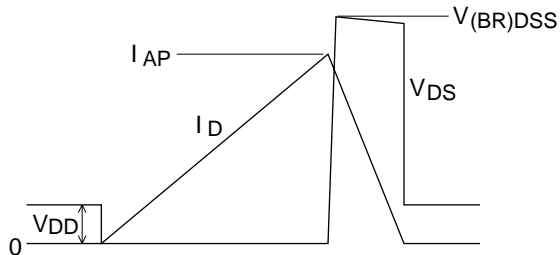
Maximum Avalanche Energy vs. Channel Temperature Derating

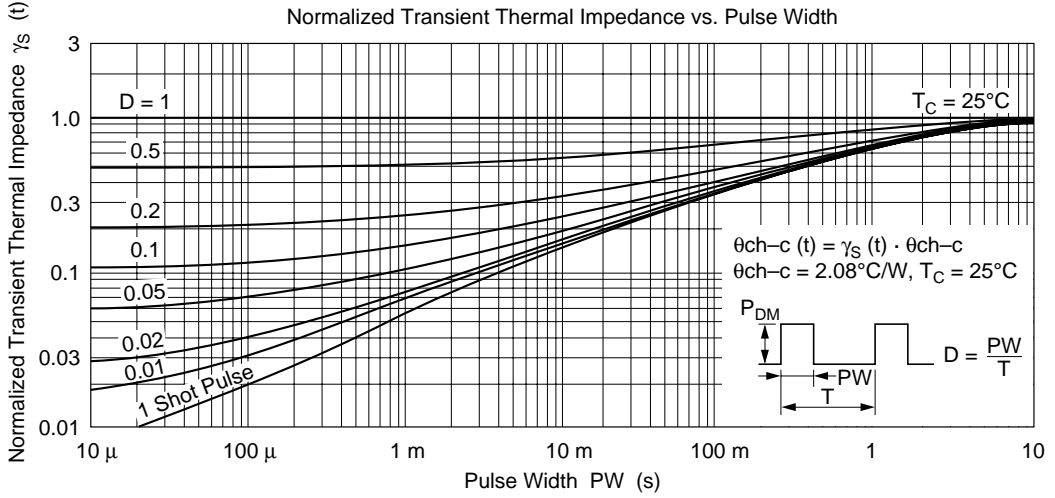


Avalanche Test Circuit and Waveform

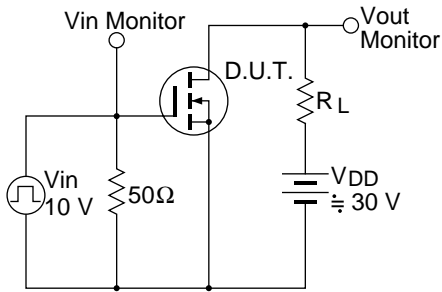


$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

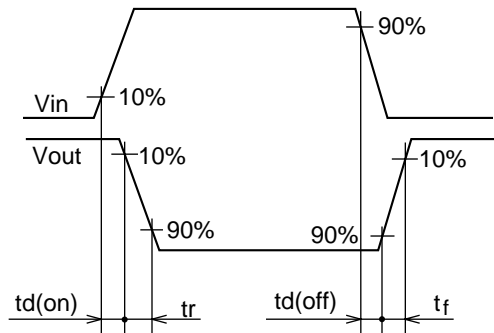


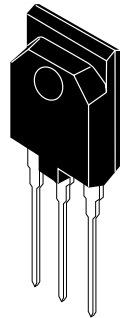
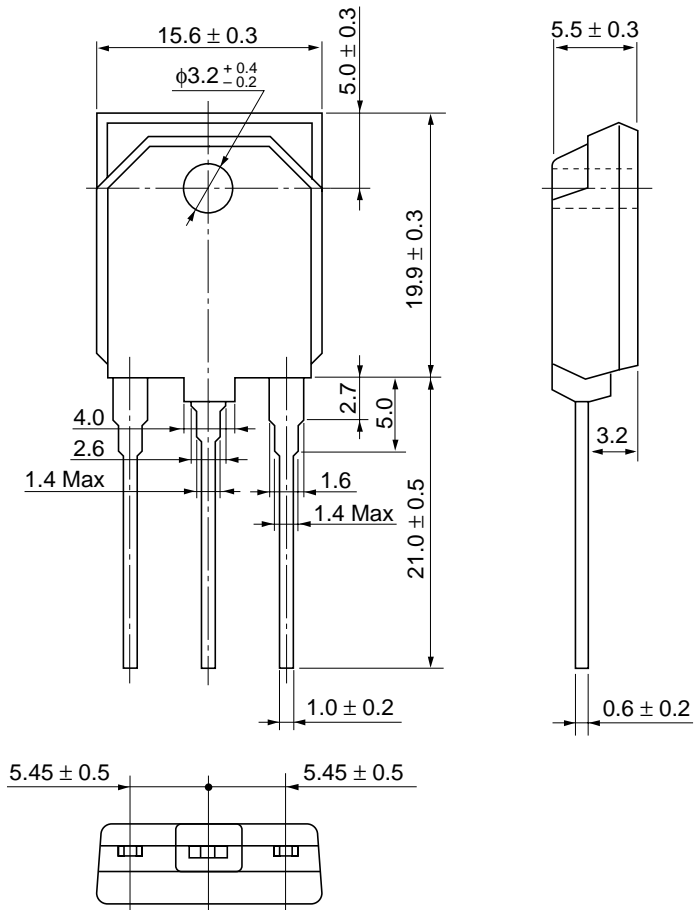


Switching Time Test Circuit



Waveform





Hitachi Code	TO-3PFM
JEDEC	—
EIAJ	—
Weight (reference value)	5.6 g

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