2SK3494

N-channel enhancement mode MOSFET

■ Features

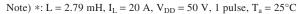
- Low on-resistance, low Q_g
- High avalanche resistance

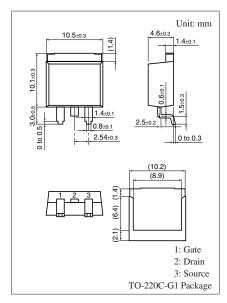
Applications

- For PDP
- For high-speed switching

■ Absolute Maximum Ratings $T_C = 25$ °C

Parameter		Symbol	Rating	Unit	
Drain-source surrender voltage		$V_{\rm DSS}$	250	V	
Gate-source surrender voltage		V _{GSS}	±30	V	
Drain current		I_{D}	20	A	
Peak drain current		I_{DP}	80	A	
Avalanche energy capability *		EAS	657	mJ	
Power dissipation		P_{D}	50	W	
	$T_a = 25$ °C		1.4		
Channel temperature		T _{ch}	150	°C	
Storage temperature		T_{stg}	-55 to +150	°C	





Marking Symbol: K3494

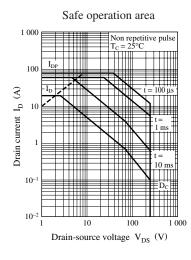
■ Electrical Characteristics $T_C = 25^{\circ}C \pm 3^{\circ}C$

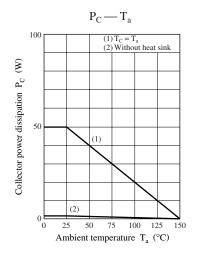
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source surrender voltage	$V_{\rm DSS}$	$I_D = 1 \text{ mA}, V_{GS} = 0$	250			V
Gate threshold voltage	V _{th}	$V_{DS} = 10 \text{ V}, I_{D} = 1 \text{ mA}$	2.0		4.0	V
Drain-source cutoff current	I_{DSS}	$V_{DS} = 200 \text{ V}, V_{GS} = 0$			10	μΑ
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0$			±1	μΑ
Drain-source ON resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		82	105	mΩ
Forward transfer admittance	Y _{fs}	$V_{DS} = 10 \text{ V}, I_{D} = 10 \text{ A}$	7	14		S
Short-circuit forward transfer capacitance (Common-source)	C _{iss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		2450		pF
Short-circuit output capacitance (Common-source)	C _{oss}			356		pF
Reverse transfer capacitance (Common-source)	C _{rss}			40		pF
Turn-on delay time	t _{d(on)}	$V_{DD} \approx 100 \text{ V}, I_D = 10 \text{ A}$		36		ns
Rise time	T _r	$R_{L} = 10 \Omega, V_{GS} = 10 V$		20		ns
Turn-off delay time	t _{d(off)}			184		ns
Fall time	t_{f}			29		ns

\blacksquare Electrical Characteristics (continued) $T_C = 25^{\circ}C \pm 3^{\circ}C$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Diode foward voltage	V _{DSF}	$I_{DR} = 20 \text{ A}, V_{GS} = 0$			-1.5	V
Reverse recovery time	t _{rr}	$L = 230 \mu H, V_{DD} = 100 V$		142		ns
Reverse recovery charge	Q _{rr}	$I_{DR} = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		668		nC
Gate charge load	Qg	$V_{DD} = 100 \text{ V}, I_D = 10 \text{ A}$		41		nC
Gate-source charge	Q_{gs}	$V_{GS} = 10 \text{ V}$		8.4		nC
Gate-drain charge	Q_{gd}			14		nC
Thermal resistance (ch-c)	R _{th(ch-c)}				2.5	°C/W
Thermal resistance (ch-a)	R _{th(ch-a)}				89.2	°C/W

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.





2 SJG00037AED

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