

FEATURES

- ◆ Two Independent Four-Bit Latches
- ◆ 3-State Outputs
- ◆ Direct Reset
- ◆ All Inputs Buffered

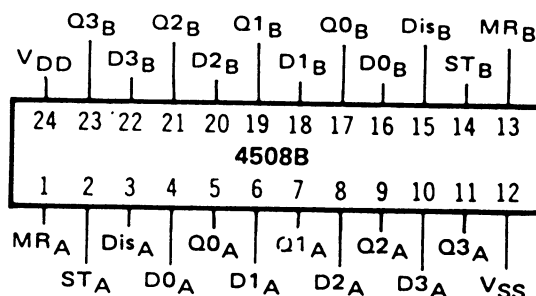
DESCRIPTION

The 4508B consists of two identical independent 4-Bit Latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high-impedance state for bus line applications.

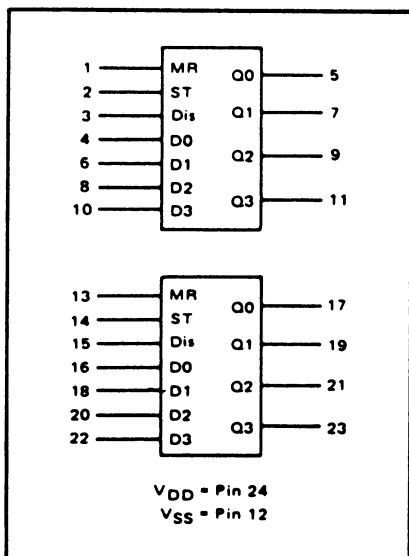
These devices find primary use in buffer storage, holding register, and display circuits, and other general digital logic applications.

CMOS DUAL 4-BIT LATCH

CONNECTION DIAGRAM (all packages)



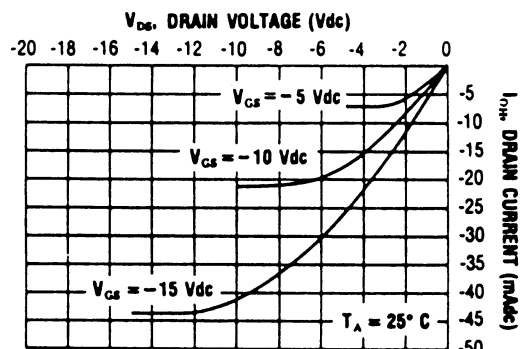
BLOCK DIAGRAM



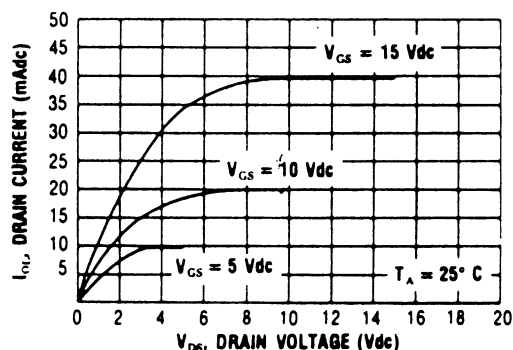
TRUTH TABLE

MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

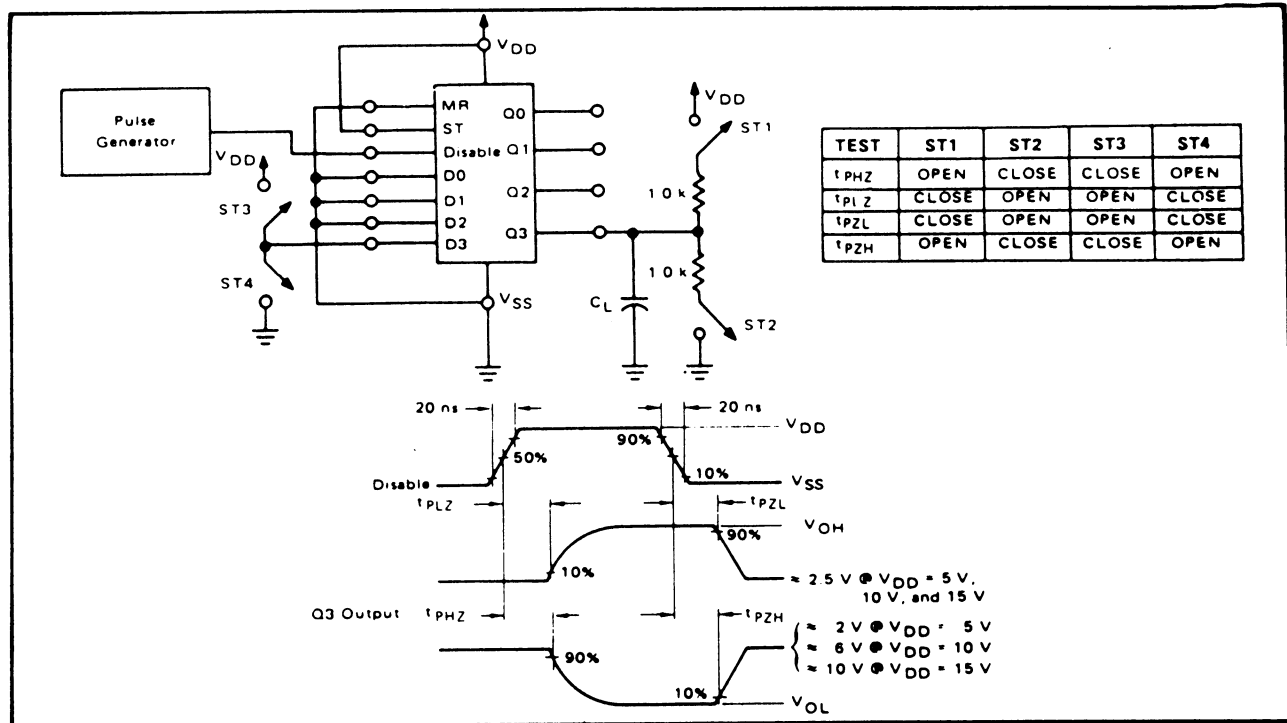
PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW}		+25°C			T _{HIGH}		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	
			—	20	—	0.2	20	—	600	
3-STATE OUTPUT LEAKAGE CURRENT	I _{ZL}		—	±0.1	—	±10 ⁻⁴	±0.1	—	±1.0	μAdc

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

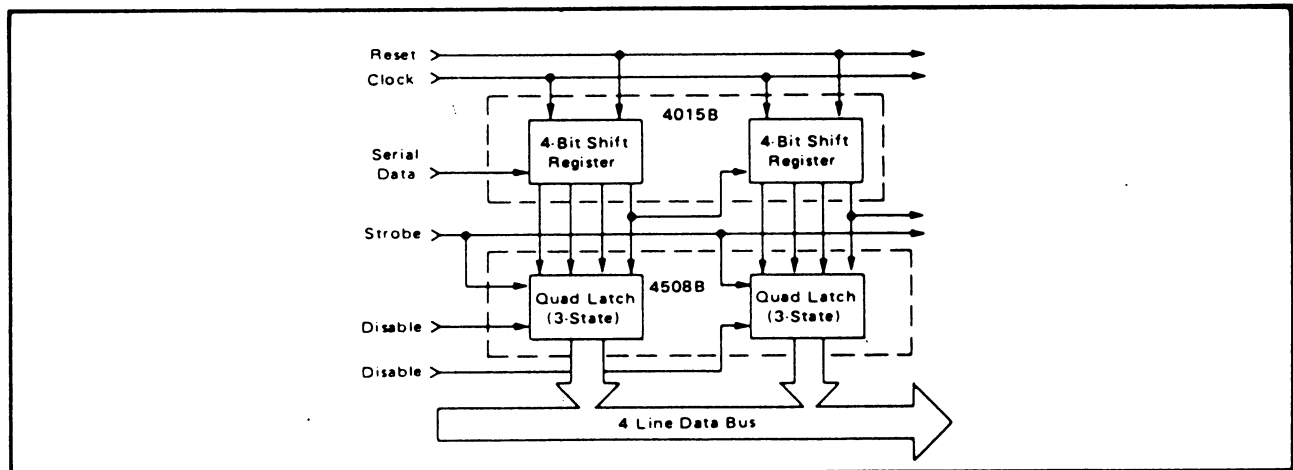
PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t _{PLH} , t _{PHL}	5	—	220	440	ns
		10	—	90	180	
		15	—	60	120	
	From Disable Input t _{PHZ} , t _{PLZ} t _{PZH} , t _{PZL}	5	—	85	170	ns
		10	—	45	90	
		15	—	30	60	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM MASTER RESET PULSE WIDTH	PW _{MR}	5	—	100	200	ns
		10	—	50	100	
		15	—	35	70	
MINIMUM STROBE PULSE WIDTH	PW _{ST}	5	—	70	140	ns
		10	—	35	70	
		15	—	20	40	
MINIMUM SETUP TIME Data Inputs	t _{setup}	5	—	25	50	ns
		10	—	10	20	
		15	—	5	10	
MINIMUM HOLD TIME Data Inputs	t _{hold}	5	—	0	0	ns
		10	—	0	0	
		15	—	0	0	

3-STATE AC TEST CIRCUIT AND WAVEFORMS

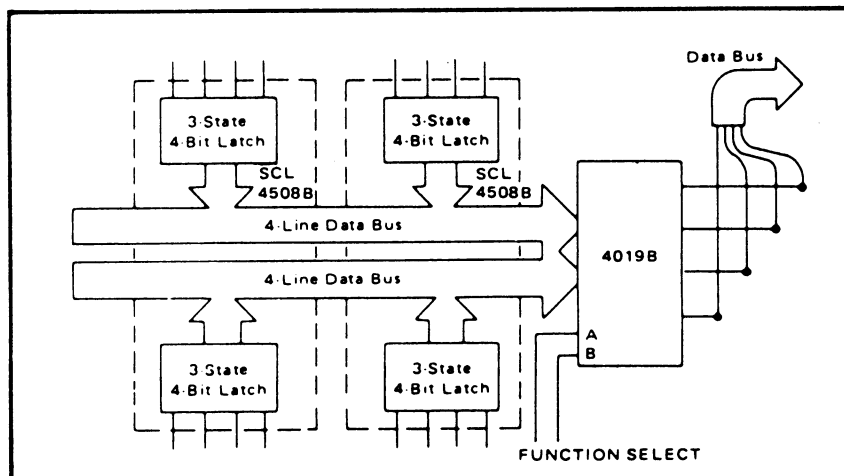


APPLICATIONS INFORMATION

BUS REGISTER



DUAL MULTIPLEXED BUS REGISTER WITH FUNCTION SELECT



FUNCTION SELECT

A	B	Function
0	0	Inhibit (all 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	A _i + B _i