

4532B

8-INPUT PRIORITY ENCODER

OBSOLETE

DESCRIPTION — The 4532B is an 8-Input Priority Encoder with eight active HIGH Priority Inputs (I₀-I₇), three active HIGH Address Outputs (A₀-A₂), an active HIGH Enable Input (E_{1n}), an active HIGH Enable Output (E_{Out}) and an active HIGH Group Select Output (GS).

Data is accepted on the eight Priority Inputs (I₀-I₇). The binary code corresponding to the highest Priority Input (I₀-I₇) which is HIGH is generated on the Address Outputs (A₀-A₂) if the Enable Input (E_{1n}) is HIGH. Priority Input I₇ is assigned the highest priority. The Group Select output (GS) is HIGH when one or more Priority Inputs (I₀-I₇) and the Enable Input (E_{1n}) are HIGH. The Enable Output (E_{Out}) is HIGH when all the Priority Inputs (I₀-I₇) are LOW and the Enable Input (E_{1n}) is HIGH. The Enable Input (E_{1n}) when LOW, forces all Outputs (A₀-A₂, GS, E_{Out}) LOW.

- ACTIVE HIGH PRIORITY INPUTS
- CASCADABLE

PIN NAMES

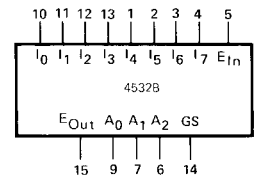
| | |
|--------------------------------|---------------------|
| I ₀ -I ₇ | Priority Inputs |
| E _{1n} | Enable Input |
| E _{Out} | Enable Output |
| GS | Group Select Output |
| A ₀ -A ₂ | Address Outputs |

TRUTH TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | | |
|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---------|----------------|----------------|----------------|------------------|
| E _{1n} | I ₇ | I ₆ | I ₅ | I ₄ | I ₃ | I ₂ | I ₁ | I ₀ | GS | A ₂ | A ₁ | A ₀ | E _{Out} |
| L | X | X | X | X | X | X | X | X | L | L | L | L | L |
| H | L | L | L | L | L | L | L | L | L | L | L | L | H |
| H | H | X | X | X | X | X | X | X | H | H | H | H | L |
| H | L | H | X | X | X | X | X | X | H | H | H | L | L |
| H | L | L | H | X | X | X | X | X | H | H | L | H | L |
| H | L | L | L | H | X | X | X | X | H | H | L | L | L |
| H | L | L | L | L | H | X | X | X | H | L | H | H | L |
| H | L | L | L | L | L | H | X | X | H | L | H | L | L |
| H | L | L | L | L | L | L | H | X | H | L | L | H | L |
| H | L | L | L | L | L | L | L | H | H | L | L | L | L |

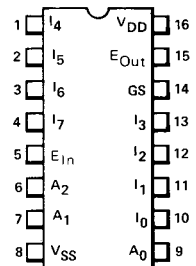
X = Don't Care (Either HIGH or LOW)
 L = LOW Level
 H = HIGH Level

LOGIC SYMBOL



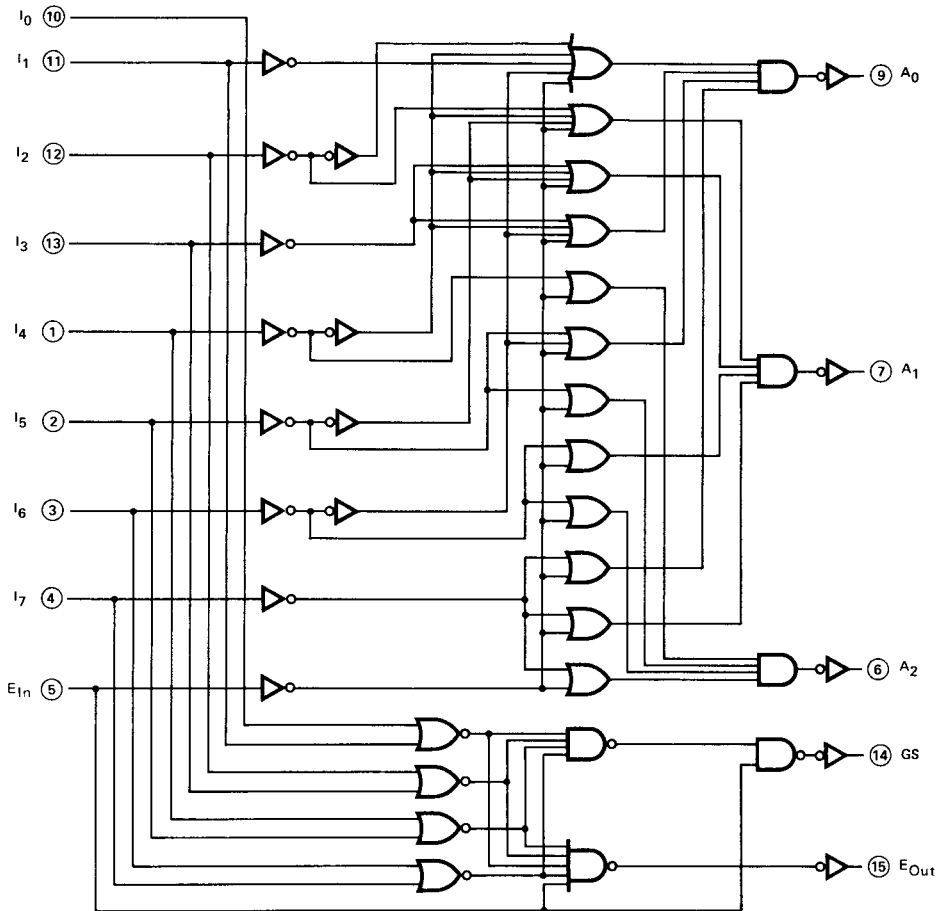
V_{DD} = Pin 16
 V_{SS} = Pin 8

**CONNECTION DIAGRAM
 DIP (TOP VIEW)**



NOTE:
 The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
 V_{SS} = Pin 8
 ○ = Pin Number

FAIRCHILD CMOS • 4532B

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

| SYMBOL | PARAMETER | | LIMITS | | | | | | | | | UNITS | TEMP | TEST CONDITIONS |
|----------|-----------------|----|----------------|-----|-----|-----------------|-----|-----|-----------------|-----|-----|---------|-----------|------------------------------|
| | | | $V_{DD} = 5$ V | | | $V_{DD} = 10$ V | | | $V_{DD} = 15$ V | | | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | | |
| I_{DD} | Quiescent Power | XC | | | 20 | | | 40 | | | 80 | μ A | MIN, 25°C | All inputs at 0V or V_{DD} |
| | | | | | 150 | | | 300 | | | 600 | | MAX | |
| | Supply Current | XM | | | 5 | | | 10 | | | 20 | μ A | MIN, 25°C | |
| | | | | | 150 | | | 300 | | | 600 | | MAX | |

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25^\circ$ C (See Note 2)

| SYMBOL | PARAMETER | LIMIT | | | | | | | | | UNITS | TEST CONDITIONS |
|-----------|--|----------------|-----|-----|-----------------|-----|-----|-----------------|-----|-----|-------|--|
| | | $V_{DD} = 5$ V | | | $V_{DD} = 10$ V | | | $V_{DD} = 15$ V | | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| t_{PLH} | Propagation Delay, E_{In} to E_{Out} | | 85 | 200 | | 45 | 90 | | 35 | 70 | ns | $C_L = 50$ pF, $R_L = 200$ k Ω Input Transition Times ≤ 20 ns |
| t_{PHL} | | | 85 | 200 | | 45 | 90 | | 35 | 70 | | |
| t_{PLH} | Propagation Delay, E_{In} to GS | | 65 | 150 | | 35 | 70 | | 25 | 56 | ns | |
| t_{PHL} | | | 65 | 150 | | 35 | 70 | | 25 | 56 | | |
| t_{PLH} | Propagation Delay, E_{In} to A_n | | 70 | 200 | | 35 | 90 | | 30 | 70 | ns | |
| t_{PHL} | | | 70 | 200 | | 35 | 90 | | 30 | 70 | | |
| t_{PLH} | Propagation Delay, I_n to A_n | | 70 | 200 | | 35 | 90 | | 30 | 70 | ns | |
| t_{PHL} | | | 70 | 200 | | 35 | 90 | | 30 | 70 | | |
| t_{PLH} | Propagation Delay, I_n to GS | | 75 | 200 | | 40 | 90 | | 31 | 70 | ns | |
| t_{PHL} | | | 70 | 200 | | 35 | 90 | | 28 | 70 | | |
| t_{TLH} | Output Transition Time | | 65 | 135 | | 35 | 75 | | 15 | 45 | ns | |
| t_{THL} | | | 65 | 135 | | 35 | 75 | | 15 | 45 | | |

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.