Wideband Dual-Channel Linear Multiplier/Divider

AD539

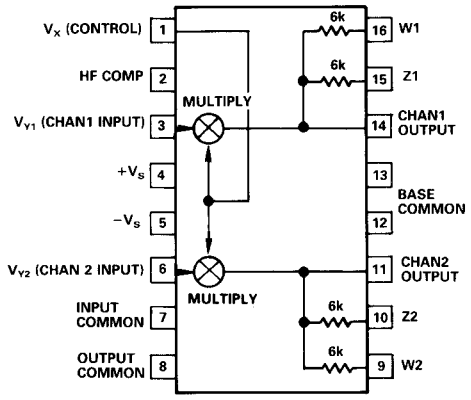
FEATURES

Two Quadrant Multiplication/Division
Two Independent Signal Channels
Signal Bandwidth of 60MHz (I_{OUT})
Linear Control Channel Bandwidth of 5MHz
Low Distortion (to 0.01%)
Fully-Calibrated, Monolithic Circuit

APPLICATIONS

Precise High Bandwidth AGC and VCA Systems
Voltage-Controlled Filters
Video-Signal Processing
High-Speed Analog Division
Automatic Signal-Leveling
Square-Law Gain/Loss Control

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD539 is a low-distortion analog multiplier having two identical signal channels (Y1 and Y2), with a common X-input providing linear control of gain. Excellent ac characteristics up to video frequencies and a 3dB bandwidth of over 60MHz are provided. Although intended primarily for applications where speed is important the circuit exhibits good static accuracy in "computational" applications. Scaling is accurately determined by a band-gap voltage reference and all critical parameters are laser-trimmed during manufacture.

The full bandwidth can be realized over most of the gain range using the AD539 with simple resistive loads of up to 100Ω. Output voltage is restricted to a few hundred millivolts under these conditions. Using external op amps such as the AD5539 in conjunction with the on-chip scaling resistors, accurate multiplication can be achieved, with bandwidths typically as high as 50MHz.

The two channels provide flexibility. In single-channel applications they may be used in parallel, to double the output current, or in series, to achieve a square-law gain function with a control range of over 100dB, or differentially, to reduce distortion. Alternatively, they may be used independently, as in audio stereo applications, with low crosstalk between channels. Voltage-controlled filters and oscillators using the "state-variable" approach are easily designed, taking advantage of the dual channels and common control. The AD539 can also be configured as a divider with signal bandwidths up to 15MHz.

Power consumption is only 135mW using the recommended ±5V supplies. The AD539 is available in three versions: the "J" and "K" grades are specified for 0 to +70°C operation and "S" grade is guaranteed over the extended range of −55°C to +125°C. The J and K grades are available in either a hermetic ceramic DIP (D) or a low cost plastic DIP (N), while the S grade is available in ceramic DIP (D) or LCC (E). J-grade chips are also available. The S grade is now available in MIL-STD-883 and Standard Military Drawing (DESC) Number 5962–8980901EA versions.

DUAL SIGNAL CHANNELS

The signal voltage inputs, V_{Y1} and V_{Y2}, have nominal full-scale (FS) values of ±2V with a peak range to ±4.2V (using a negative supply of 7.5V or greater). For video applications where differential phase is critical a reduced input range of ±1 volt is recommended, resulting in a phase variation of typically ±0.2° at 3.579MHz for full gain. The input impedance is typically 400kΩ shunted by 3pF. Signal channel distortion is typically well under 0.1% at 10kHz and can be reduced to 0.01% by using the channels differentially.

COMMON CONTROL CHANNEL

The control channel accepts positive inputs, V_X, from 0 to +3V FS, ±3.3V peak. The input resistance is 500Ω. An external, grounded capacitor determines the small-signal bandwidth and recovery time of the control amplifier; the minimum value of 3nF allows a bandwidth at mid-gain of about 5MHz. Larger compensation capacitors slow the control channel but improve the high-frequency performance of the signal channels.

FLEXIBLE SCALING

Using either one or two external op amps in conjunction with the on-chip 6kΩ scaling resistors, the output currents (nominally ±1mA FS, ±2.25mA peak) can be converted to voltages with accurate transfer functions of $V_W = -V_X V_Y/2$, $V_W = -V_X V_Y$ or $V_W = -2V_X V_Y$ (where inputs V_X and V_Y and output V_W are expressed in volts), with corresponding full-scale outputs of ±3V, ±6V and ±12V. Alternatively, low-impedance grounded loads can be used to achieve the full signal bandwidth of 60MHz, in which mode the scaling is less accurate.

REV. A

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AD539—SPECIFICATIONS (@ T_A = 25°C, V_S = ±5V, unless otherwise specified)

Parameter	Conditions	AD539J Min	AD539J Typ	AD539J Max	AD539K Min	AD539K Typ	AD539K Max	AD539S Min	AD539S Typ	AD539S Max	Units
SIGNAL-CHANNEL DYNAMICS											
Minimal Configuration	Reference Figure 6a										
Bandwidth, −3dB	R_L = 50Ω, C_C = 0.01μF	30	60		30	60		30	60		MHz
Maximum Output	+0.1V<V_X<+3V, $V_Y$ac = 1V rms		−10			−10			−10		dBm
Feedthrough, f<1MHz	V_X = 0, $V_Y$ac = 1.5V rms		−75			−75			−75		dBm
f = 20MHz			−55			−55			−55		dBm
Differential Phase Linearity											
−1V<$V_Y$dc<+1V	f = 3.58MHz, V_X = +3V,		±0.2			±0.2			±0.2		Degrees
−2V<$V_Y$dc<+2V	$V_Y$ac = 100mV		±0.5			±0.5			±0.5		Degrees
Group Delay	V_X = +3V, $V_y$ac = 1V rms, f = 1MHz		4			4			4		ns
Standard Dual-Channel Multiplier	Reference Figure 2										
Maximum Output	V_X = +3V, $V_Y$ac = 1.5V rms		4.5			4.5			4.5		V
Feedthrough, f<100kHz	V_X = 0, $V_Y$ac = 1.5V rms		1			1			1		mV rms
Crosstalk (CH1 to CH2)	V_{Y1} = 1V rms, V_{Y2} = 0										
	V_X = +3V, f<100kHz		−40			−40			−40		dB
RTO Noise, 10Hz to 1MHz	V_X = +1.5V, V_Y = 0, Figure 2		200			200			200		nV/√Hz
THD + Noise, V_X = +1V,	f = 10kHz, $V_Y$ac = 1V rms		0.02			0.02			0.02		%
V_Y = +3V	f = 10kHz, $V_Y$ac = 1V rms		0.04			0.04			0.04		%
Wide Band Two-Channel Multiplier	Figure 2										
Bandwidth, −3dB (LH0032)	+0.1V<V_X<+3V, $V_Y$ac = 1V rms		25			25			25		MHz
Maximum Output V_X = +3V	$V_Y$ac = 1.5V rms, f = 3MHz		4.5			4.5			4.5		V rms
Feedthrough V_X = 0V	$V_Y$ac = 1.0V rms, f = 3MHz		14			14			14		mV rms
Wide Band Single Channel VCA											
(AD5539)	Reference Figure 8										
Bandwidth, −3dB	+0.1V<V_X<+3V, $V_Y$ac = 1V rms		50			50			50		MHz
Maximum Output	75Ω Load		±1			±1			±1		V
Feedthrough	V_X = −0.01V, f = 5MHz		−54			−54			−54		dB
CONTROL CHANNEL DYNAMICS											
Bandwidth, −3dB	C_C = 3000pF, $V_X$dc = +1.5V,										
	$V_X$ac = 100mV rms		5			5			5		MHz
SIGNAL INPUTS, V_{Y1} & V_{Y2}											
Nominal Full-Scale Input			±2			±2			±2		V
Operational Range, Degraded Performance	$-V_S \leq 7V$	**±4.2**			**±4.2**			**±4.2**			V
Input Resistance			400			400			400		kΩ
Bias Current			10	**30**		10	**20**		10	**30**	μA
Offset Voltage	V_X = +3V, V_Y = 0		5	**20**		5	**10**		5	**20**	mV
(T_{min} to T_{max})			10			5			15	**35**	mV
Power Supply Sensitivity	V_X = +3V, V_Y = 0		2			2			2		mV/V
CONTROL INPUT, V_X											
Nominal Full-Scale Input			+3.0			+3.0			+3.0		V
Operational Range, Degraded Performance		**+3.2**			**+3.2**			**+3.2**			V
Input Resistance[1]			500			500			500		Ω
Offset Voltage			1	**4**		1	**2**		1	**4**	mV
(T_{min} to T_{max})			3			2			2	**5**	mV
Power Supply Sensitivity			30			30			30		μV/V
Gain	(Figure 2)										
Absolute Gain Error	V_X = +0.1V to +3.0V and		0.2	**0.4**		0.1	**0.2**		0.2	**0.4**	dB
(T_{min} to T_{max})	V_y = ±2V		0.3			0.15			0.25	**0.5**	dB
CURRENT OUTPUT[1]											
Full-Scale Output Current	V_X = +3V, V_Y = ±2V		±1			±1			±1		mA
Peak Output Current	V_X = +3.3V, V_Y = ±5V, V_S = ±7.5V	±2	±2.8		±2	±2.8		±2	±2.8		mA
Output Offset Current	V_X = 0, V_Y = 0		0.2	**1.5**		0.2	**1.5**		0.2	**1.5**	μA
Output Offset Voltage[2]	Figure 2, V_X = 0, V_Y = 0		3	**10**		3	**10**		3	**10**	mV
Output Resistance[1]			1.2			1.2			1.2		kΩ
Scaling Resistors											
CH1	Z1, W1 to CH1		6			6			6		kΩ
CH2	Z2, W2 to CH2		6			6			6		kΩ
VOLTAGE OUTPUTS, V_{W1} & V_{W2}[2]	(Figure 2)										
Multiplier Transfer Function,											
Either Channel			$V_W = -V_X \cdot V_Y / V_U$			$V_W = -V_X \cdot V_Y / V_U$			$V_W = -V_X \cdot V_Y / V_U$		
Multiplier Scaling Voltage, V_U		**0.98**	1.0	**1.02**	**0.99**	1.0	**1.01**	**0.98**	1.0	**1.02**	V
Accuracy			0.5	2		0.5	1		0.5	2	%
(T_{min} to T_{max})			1			0.5			1.0	3	%
Power Supply Sensitivity			0.04			0.04			0.04		%/V
Total Multiplication Error[3]	V_X<=+3V, −2V<V_Y<2V		1	**2.5**		0.6	**1.5**		1	**2.5**	% FSR
T_{min} to T_{max}			2			1			2	**4**	%
Control Feedthrough	V_X = 0 to +3V, V_Y = 0		25	**60**		15	**30**		15	**60**	mV
T_{min} to T_{max}			30			15			60	**120**	mV
TEMPERATURE RANGE											
Rated Performance		0		+70	0		+70	−55		+125	°C
POWER SUPPLIES											
Operational Range		±4.5		±15	±4.5		±15	±4.5		±15	V
Current Consumption											
$+V_S$			8.5	**10.2**		8.5	**10.2**		8.5	**10.2**	mA
$-V_S$			18.5	**22.2**		18.5	**22.2**		18.5	**22.2**	mA

NOTES

[1]Resistance value and absolute current outputs subject to 20% tolerance.

[2]Spec assumes the external op amp is trimmed for negligible input offset.

[3]Includes all errors.

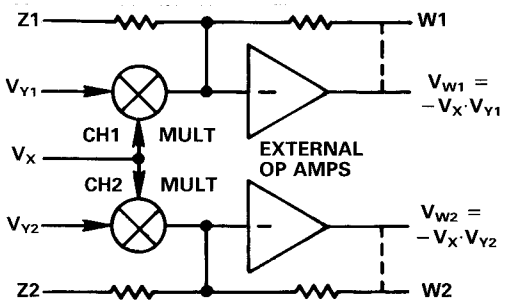
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD539JN	0°C to +70°C	Plastic DIP	N-16
AD539KN	0°C to +70°C	Plastic DIP	N-16
AD539JD	0°C to +70°C	Side Brazed DIP	D-16
AD539KD	0°C to +70°C	Side Brazed DIP	D-16
AD539J Chip	0°C to +70°C	Chip	
AD539SD	−55°C to +125°C	Side Brazed DIP	D-16
AD539SD/883B	−55°C to +125°C	Side Brazed DIP	D-16
5962–8980901EA[1]	−55°C to +125°C	Side Brazed DIP	D-16
AD539SE/883B	−55°C to +125°C	LCC	E-20A

NOTE
[1]The standard military drawing version of the AD539 (5962–8980901EA) is now available.



AD539 Functional Block Diagram

CIRCUIT DESCRIPTION

Figure 1 is a simplified schematic of the AD539. Q1-Q6 are large-geometry transistors designed for low distortion and low noise. Emitter-area scaling further reduces distortion: Q1 is 3 times larger than Q2; Q4, Q5 are each 3 times larger than Q3, Q6, and these transistors are twice as large as Q1, Q2. A stable reference current I_{REF} = 1.375mA is produced by a band-gap reference circuit and applied to the common emitter node of a *controlled-cascode* formed by Q1 and Q2. When V_X = 0, all of I_{REF} flows in Q1, due to the action of the high-gain control amplifier which lowers the voltage on the base of Q2. As V_X is raised the fraction of I_{REF} flowing in Q2 is forced to balance the control current, V_X/2.5k. At the full-scale value of V_X (+3V) this fraction is 0.873. Since the bases of Q1, Q4 and Q5 are at ground potential and the bases of Q2, Q3 and Q6 are commoned, all three controlled-cascodes divide the current applied to their emitter nodes in the same proportion. The control loop is stabilized by the external capacitor, C_C.

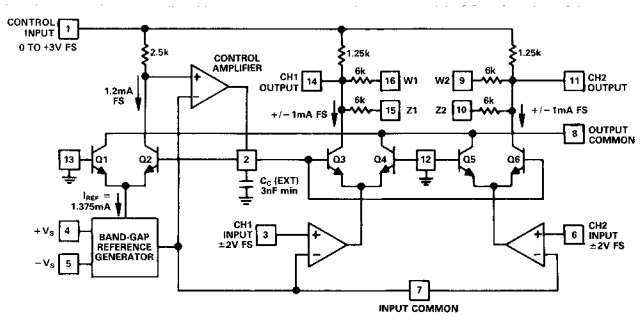


Figure 1. Simplified Schematic of AD539 Multiplier

The signal voltages V_{Y1} and V_{Y2} (generically referred to as V_Y) are first converted to currents by voltage-to-current converters with a g_m of 575μmhos; thus, the full-scale input of ±2V becomes a current of ±1.15mA, which is superimposed on a bias of 2.75mA, and applied to the common emitter node of controlled cascode Q3-Q4 or Q5-Q6. As just explained, the proportion of this current steered to the output node is linearly dependent on V_X. Thus for full-scale V_X and V_Y inputs, a signal of ±1mA (0.873 × ±1.15mA) and a bias component of 2.4mA (0.873 × 2.75mA) appear at the output. The bias component absorbed by the 1.25k resistors also connected to V_X, and the resulting signal current can be applied to an external load resistor (in which case scaling is not accurate) or can be forced into either or both of the 6kΩ feedback resistors (to the Z and W nodes) by an external op amp. In the latter case, scaling accuracy is guaranteed.

GENERAL RECOMMENDATIONS

The AD539 is a high speed circuit and requires considerable care to achieve its full performance potential. A high-quality ground plane should be used with the device either soldered directly into the board or mounted in a low-profile socket. In the figures used here an open triangle denotes a *direct, short* connection to this ground plane; pins 12 and 13 are especially prone to unwanted signal pick-up. Power supply decoupling capacitors of 0.1μF to 1μF should be connected from pins 4 and 5 to the ground plane. In applications using external high-speed op amps, separate supply decoupling should be used. It is good practice to insert small (10Ω) resistors between the primary supply and the decoupling capacitor.

The control amplifier compensation capacitor, C_C, should likewise have short leads to ground and a minimum value of 3nF. Unless maximum control bandwidth is esssential it is advisable to use a larger value of 0.01μF to 0.1μF to improve the signal channel phase response, high-frequency crosstalk and high-frequency distortion. The control bandwidth is inversely proportional to this capacitance, typically 2MHz for C_C = 0.01μF, V_X = 1.7V. The bandwidth and pulse response of the control channel can be improved by using a feedforward capacitor of 5% to 20% the value of C_C between pins 1 and 2. Optimum transient response will result when the rise/fall time of V_X are commensurate with the control-channel response time.

V_X should not exceed the specified range of 0 to +3V. The ac gain is zero for V_x<0 but there remains a feedforward path (see Figure 1) causing control feedthrough. Recovery time from negative values of V_X can be improved by adding a small-signal Schottky diode with its cathode connected to pin 2 and its anode grounded. This constrains the voltage swing on C_C. Above V_X = +3.2V, the ac gain limits at its maximum value, but any overdrive appears as control feedthrough at the output.

The power supplies to the AD539 can be as low as ±4.5V and as high as ±16.5V. The maximum allowable range of the signal inputs, V_Y, is approximately 0.5V above +V_S; the minimum value is 2.5V above −V_S. To accommodate the peak specified inputs of ±4.2V the supplies should be nominally +5V and −7.5V. While there is no performance advantage in raising supplies above these values, it may often be convenient to use the same supplies as for the op amps. The AD539 can tolerate the excess voltage with only a slight effect on dc accuracy but dissipation at ±16.5V can be as high as 535mW and some form of heat-sink is essential in the interests of reliability.

TRANSFER FUNCTION

In using any analog multiplier or divider careful attention must be paid to the matter of *scaling*, particularly in computational applications. To be *dimensionally consistent* a scaling voltage must appear in the transfer function, which, for each channel of the AD539 in the standard multiplier configuration (Figure 2) is

$$V_W = -V_X V_Y / V_U$$

where the inputs V_X and V_Y, the output V_W and the scaling voltage V_U are expressed in a consistent unit, usually volts. In this case, V_U is fixed by the design to be 1V and it is often acceptable in the interest of simplification to use the less rigorous expression

$$V_W = -V_X V_Y$$

where it is understood that *all signals must be expressed in volts*, that is, they are rendered dimensionless by division by (1V).

The accuracy specifications for V_U allow the use of either of the two feedback resistors supplied with each channel, since these are very closely matched, or they may be used in parallel to halve the gain (double the effective scaling voltage), when

$$V_W = -V_X V_Y / 2.$$

When an external load resistor, R_L, is used the scaling is no longer exact since the internal thin-film resistors, while trimmed to high *ratiometric* accuracy, have an absolute tolerance of 20%. However, the nominal transfer function is

$$V_W = -V_X V_Y / V_U'$$

where the effective scaling voltage, V_U' can be calculated for each channel using the formula $V_U' = V_U (5R_L + 6.25)/R_L$, where R_L is expressed in kilohms. For example, when R_L = 100Ω, V_U' = 67.5V. Table II provides more detailed data for the case where both channels are used in parallel. The AD539 can also be used with no external load (output pin 11 or 14 open-circuit), when V_U' is quite accurately 5V.

BASIC MULTIPLIER CONNECTIONS

Figure 2 shows the connections for the standard two-channel multiplier, using op amps to provide useful output power and the AD539 feedback resistors to achieve accurate scaling. The transfer function for each channel is

$$V_W = -V_X V_Y$$

where inputs and outputs are expressed in volts (see TRANSFER FUNCTION). At the nominal full-scale inputs of V_X = +3V, V_Y = ±2V the full-scale outputs are ±6V. Depending on the choice of op amp, their supply voltages usually need to be about 2V more than the peak output. Thus, supplies of at least ±8V are required; the AD539 can share these supplies. Higher outputs are possible if V_X and V_Y are driven to their peak values of

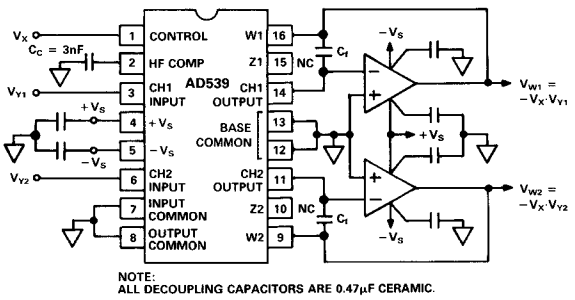


Figure 2. Standard Dual-Channel Multiplier

+3.2V and ±4.2V respectively, when the peak output is ±13.4V. This requires operating the op amps at supplies of ±15V. Under these conditions it is advisable to reduce the supplies to the AD539 to ±7.5V to limit its power dissipation; however, with some form of heat sinking it is permissible to operate the AD539 directly from ±15V supplies.

Viewed as a voltage-controlled amplifier, the decibel gain is simply

$$G = 20 \log V_X$$

where V_X is expressed in volts. This results in a gain of 10dB at V_X = +3.162V, 0dB at V_X = +1V, −20dB at V_X = +0.1V, and so on. In many ac applications the output offset voltage (for V_X = 0 or V_Y = 0) will not be of major concern; however, it can be eliminated using the offset nulling method recommended for the particular op amp, with $V_X = V_Y = 0$.

At small values of V_X the offset voltage of the control channel will degrade the gain/loss accuracy. For example, a ±1mV offset uncertainty will cause the nominal 40dB attenuation at V_X = +0.01V to range from 39.2dB to 40.9dB. Figure 3a shows the maximum gain error boundaries based on the guaranteed control-channel offset voltages of ±2mV for the AD539K and ±4mV for the AD539J. These curves include all scaling errors and apply to all configurations using the internal feedback resistors (W1 and W2; alternatively, Z1 and Z2).

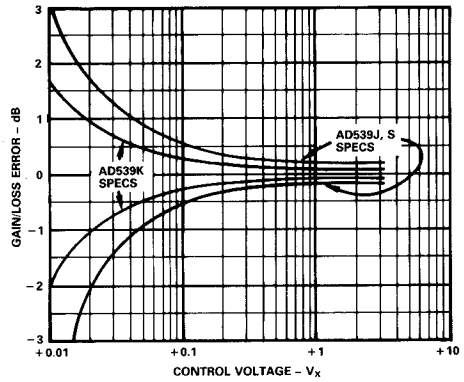


Figure 3a. Maximum AC Gain Error Boundaries

Distortion is a function of the signal input level (V_Y) and the control input (V_X). It is also a function of frequency, although in practice the op amp will generate most of the distortion at frequencies above 100kHz. Figure 3b shows typical results at f = 10kHz as a function of V_X with V_Y = 0.5 and 1.5V rms.

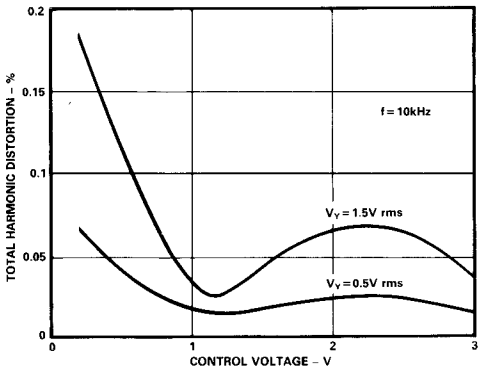


Figure 3b. Total Harmonic Distortion vs. Control Voltage

In some cases it may be desirable to alter the scaling. This can be achieved in several ways. One option is to use both the Z and W feedback resistors (see Figure 1) in parallel, in which case $V_W = -V_X V_Y/2$. This may be preferable where the output swing must be held at ±3V FS (±6.75V pk), for example, to allow the use of reduced supply voltages for the op amps. Alternatively, the gain can be doubled by connecting both channels in parallel and using only a single feedback resistor, in which case $V_W = -2V_X Y_Y$ and the full-scale output is ±12V. Another option is to insert a resistor in series with the control-channel input, permitting the use of a large (for example, 0 to +10V) control voltage. A disadvantage of this scheme is the need to adjust this resistor to accommodate the tolerance of the nominal 500Ω input resistance at pin 1. The signal channel inputs can also be resistively attenuated to permit operation at higher values of V_Y, in which case it may often be possible to partially compensate for the response roll-off of the op amp by adding a capacitor across the upper arm of this attenuator.

Signal-Channel ac and Transient Response

The HF response is dependent almost entirely on the op amp. Note that the "noise gain" for the op amp in Figure 2 is determined by the value of the feedback resistor (6kΩ) and the 1.25kΩ control-bias resistors (Figure 1). Op amps with provision for external frequency compensation (such as the AD301 and AD518) should be compensated for a closed-loop gain of 6.

The layout of the circuit components is very important if low feedthrough and flat response at low values of V_X is to be maintained (see GENERAL RECOMMENDATIONS).

For wide-bandwidth applications requiring an output voltage swing greater than ±1V, the LH0032 hybrid op-amp is recommended. Figure 4a shows the HF response of the circuit of Figure 2 using this amplifier with V_Y = 1V rms and other conditions as shown in Table I. C_F was adjusted for 1dB peaking at V_X = +1V; the −3dB bandwidth exceeds 25MHz. The effect of signal feedthrough on the response becomes apparent at V_X = +0.01V. The minimum feedthrough results when V_X is taken slightly negative to ensure that the residual control-channel offset is exceeded and the dc gain is reliably zero. Measurements show that the feedthrough can be held to −90dB relative to full output at low frequencies and to −60dB up to 20MHz with careful board layout. The corresponding pulse response is shown in Figure 4b for a signal input of V_Y of ±1V and two values of V_X (+3V and +0.1V).

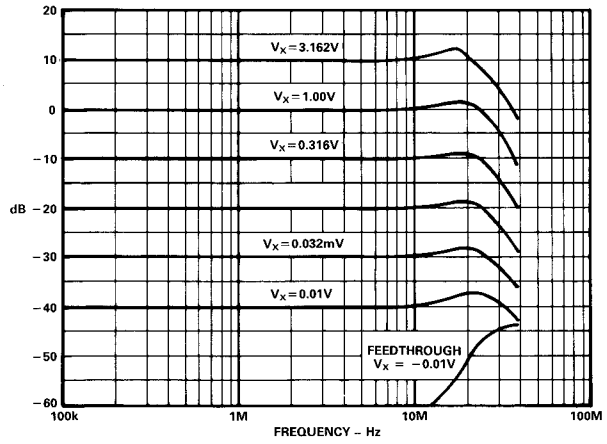
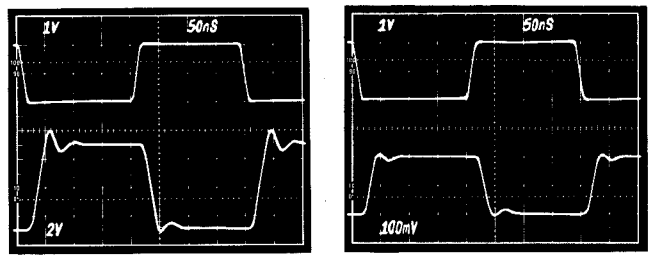


Figure 4a. Multiplier HF Response Using LH0032 Op Amps



V_X = +3V V_X = +0.1V

Figure 4b. Multiplier Pulse Response Using LH0032 Op Amps

	AD711[1]	AD5539[2]	LH0032[1]
Op Amp Supply Voltages	±15V	±9V	±10V
Op Amp Compensation Capacitor	None	None	1-5pF
Feedback Capacitor, C_F	None	0.25-1.5pF	1-4pF
−3dB Bandwidth, V_X = +1V	900kHz	50MHz	25MHz
Load Capacitance	<1nF	<10pF	<100pF
HF Feedthrough, V_X = −0.01V, f = 5MHz	N/A	−54dB	−70dB
rms Output Noise, V_X = +1V, BW 10Hz-10kHz	50μV	40μV	30μV
rms Output Noise, V_X = +1V, BW 10Hz-5MHz	120μV	620μV	500μV

In all cases, 0.47μF ceramic supply-decoupling capacitors were used at each IC pin, the AD539 supplies were ±5V and the control-compensation capacitor C_C was 3nF.

NOTES
[1]For the circuit of Figure 2.
[2]For the circuit of Figure 8.

Table I. Summary of Operating Conditions and Performance for the AD539 When Used with Various External Op-Amp Output Amplifiers

Minimal Wide-Band Configurations

The maximum bandwidth can be achieved using the AD539 with simple resistive loads to convert the output currents to voltages. These currents (nominally ±1mA FS, ±2.25mA pk,

Table II. Summary of Performance for Minimal Configuration

Load Resistance	50Ω	75Ω	100Ω	150Ω	600Ω	O/C
FS Output Voltage	±92.6mV 65.5mV rms	±134mV 94.7mV rms	±172mV 122mV rms	±242mV 171mV rms	±612mV 433mV rms	±1V *
FS Output-Power in Load	0.086mW −10.5dBm	0.12mW −9.2dBm	0.15mW −8.3dBm	0.195mW −7.1dBm	0.312mW −5.05dBm	– –
Pk Output Voltage	±210mV 148mV rms	±300mV 212mV rms	±388mV 274mV rms	±544mV 385mV rms	±1V *	±1V *
Pk Output-Power in Load	0.44mW −7dBm	0.6mW −4.4dBm	0.75mW −2.5dBm	1mW 0dBm	±1V *	±1V *
Effective Scaling Voltage, V_U'	67.5V	46.7V	36.3V	25.8V	10.2V	5V

*Peak negative voltage swing limited by output compliance.

into short-circuit loads) are shunted by their source resistance of 1.25kΩ (each channel). Calculations of load power and effective scaling-voltage must allow for this shunting effect when using resistive loads. The output power is quite low in this mode, and the device behaves more like a voltage-controlled attenuator than a classical multiplier. The matching of gain and phase between the two channels is excellent. From dc to 10MHz the gains are typically within ±0.025dB (measured using precision 50Ω load resistors) and the phase difference within ±0.1°.

For a given load resistance the output power can be quadrupled by using both channels in parallel, as shown in Figure 5a. The small-signal silicon diode D connected between ground and pins 12 and 13 provides extra voltage compliance at the output nodes in the negative direction (to −1V at 25°C); it is not required if the output swing does not exceed −300mV. Table II compares performance for various load resistances, using this configuration.

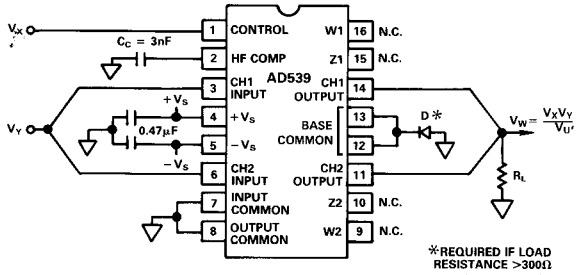


Figure 5a. Minimal Single-Channel Multiplier

Figure 5b shows the HF response for Figure 5a with the AD539 in a carefully-shielded 50Ω test-environment; the test system response was first characterized and this background removed by digital signal processing to show the inherent circuit response.

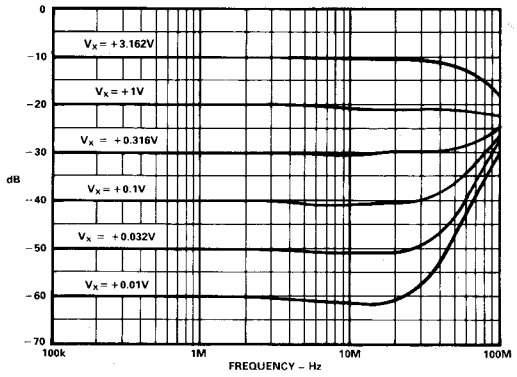


Figure 5b. HF Response in Minimal Configuration

In many applications *phase linearity* over frequency is important. Figure 5c shows the deviation from an ideal linear-phase response for a typical AD539 over the frequency range dc to 10MHz, for V_X = +3V; the peak deviation is slightly more than 1°. *Differential phase linearity* (the stability of phase over the signal window at a fixed frequency) is shown in Figure 5d for f = 3.579MHz and various values of V_X. The most rapid variation occurs for V_Y above +1V; in applications where this characteristic is critical, it is recommended that a ground-referenced, negative-going signal be used.

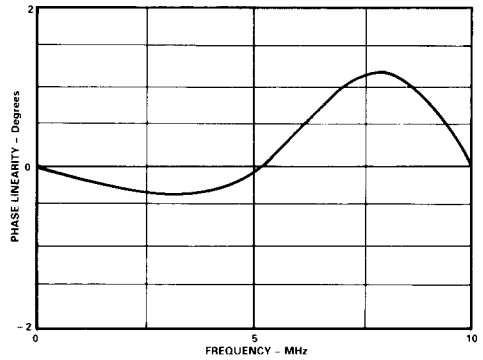


Figure 5c. Phase Linearity Error in Minimal Configuration

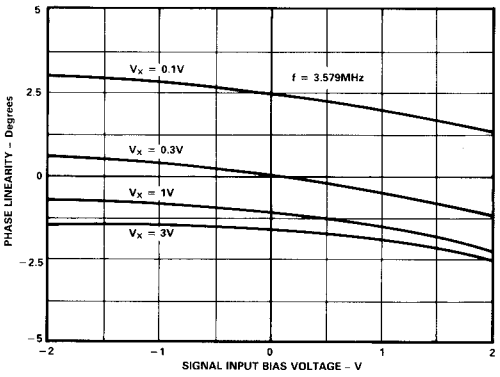


Figure 5d. Differential Phase Linearity in Minimal Configuration for a Typical Device

Differential Configurations

When only one signal channel must be handled it is often advantageous to use the channels differentially. By subtracting the CH1 and CH2 outputs any residual transient control feedthrough is virtually eliminated. Figure 6a shows a minimal configuration where it is assumed that the host system uses differential signals and a 50Ω environment throughout. This figure also shows a recommended control-feedforward network to improve large-signal

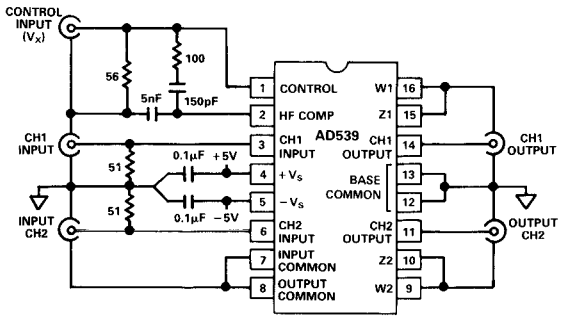


Figure 6a. High-Speed Differential Configuration

response time. The control feedthrough glitch is shown in Figure 6b, where the input was applied to CH1 and only the output of CH1 was displayed on the oscilloscope. The improvement obtained when CH1 and CH2 outputs are viewed differentially is clear in Figure 6c. The envelope rise-time is of the order of 40ns.

Lower distortion results when CH1 and CH2 are driven by *complementary* inputs and the outputs are utilized differentially, using a circuit such as Figure 7a. Resistors R1 and R2 should have a value in the range 100 to 1000Ω.

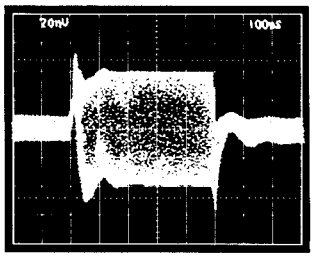


Figure 6b. Control Feedthrough One Channel of Figure 6a

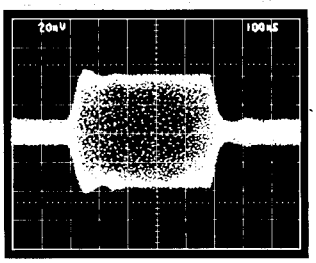


Figure 6c. Control Feedthrough Differential Mode, Figure 6a

They minimize a secondary distortion mechanism caused by a collector-modulation effect in the controlled cascodes (see CIRCUIT DESCRIPTION) by keeping the voltage-swing at the outputs to an acceptable level. Figure 7b shows the improvement in distortion over the standard configuration (compare Figure 3b). Note that the Z nodes (pins 10 and 15) are returned to the control input; this prevents the early onset of output-transistor saturation.

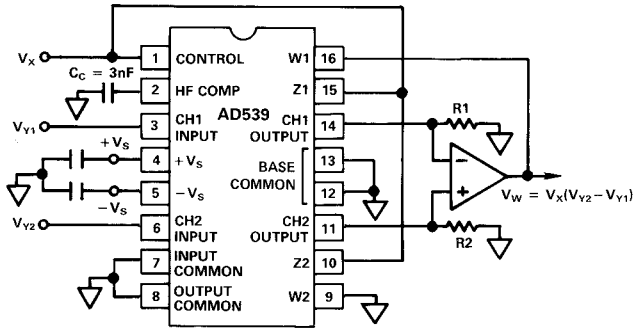


Figure 7a. Low-Distortion Differential Configuration

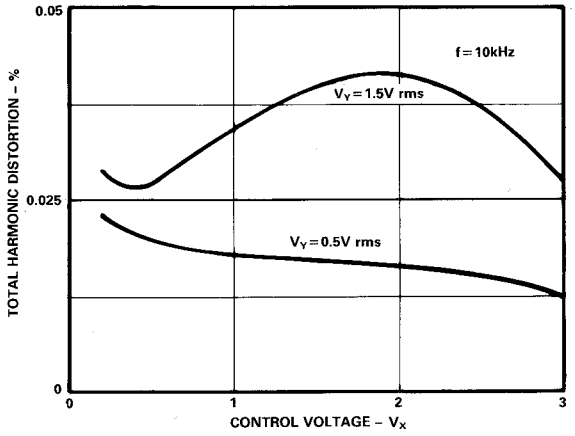


Figure 7b. Distortion in Differential Mode Using LH0032 Op Amp

Even lower distortion (0.01%, or −80dB) has been measured using two output op amps in a configuration similar to Figure 2 connected as virtual-ground current-summers (to prevent the modulation effect). Note that to generate the difference output it is merely necessary to connect the output of the CH1 op amp to the Z node of CH2. In this way, the net input to the CH2 op amp is the difference signal, and the low-distortion resultant appears as its output.

A 50MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 8 is a circuit for a 50MHz voltage-controlled amplifier (VCA) suitable for use in high-quality-video-speed applications. The outputs from the two-signal channels of the AD539 are applied to the op-amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven (V_X<0 or V_X>3.3V). Secondly, it provides a choice of either non-inverting or inverting responses, using either inputs V_{Y1} or V_{Y2} respectively. In this circuit, the output of the op-amp will equal:

$$V_{OUT} = \frac{V_X\,(V_{Y1} - V_{Y2})}{2V} \text{ for } V_X > 0$$

Hence, the gain is unity at $V_X = +2V$. Since V_X can over-range to +3.3V, the maximum gain in this configuration is about 4.3dB. (Note: If pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10dB.)

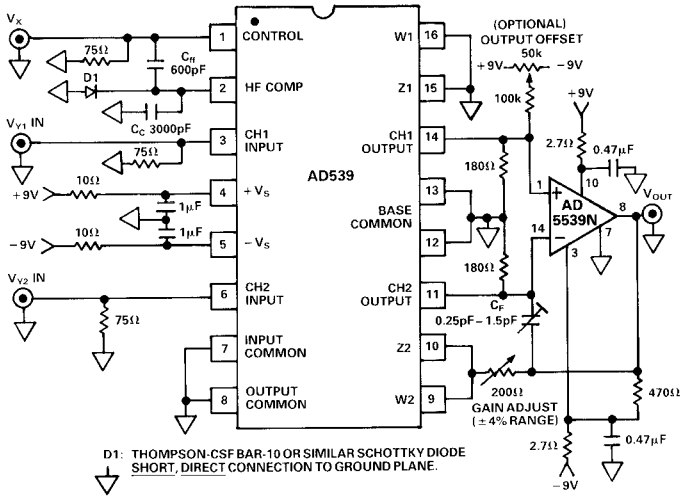


Figure 8. A Wide Bandwidth Voltage-Controlled Amplifier

The −3dB bandwidth of this circuit is over 50MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, *extreme* care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 9a shows the ac response from the noninverting

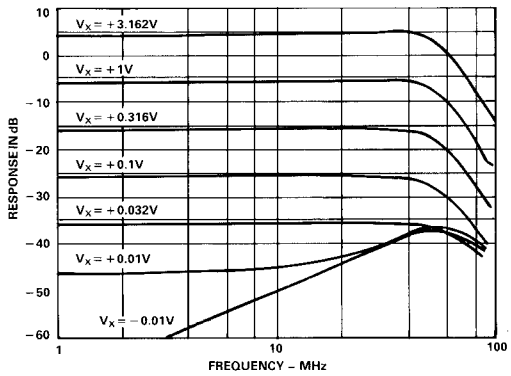


Figure 9a. AC Response of the VCA at Different Gains V_Y = 0.5V RMS

input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: $V_{Y1} = 0.5V$ rms for values of V_X from +10mV to +3.16V; this is with a 75Ω load on the output. The feedthrough at $V_X = -10mV$ is also shown.

The transient response of the signal channel at $V_X = +2V$, $V_Y = V_{OUT} = \pm 1V$ is shown in Figure 9b; with the VCA driving a 75Ω load. The rise and fall times are approximately 7ns.

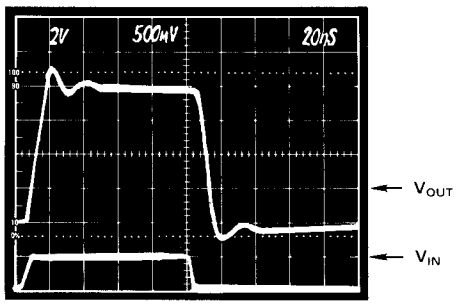


Figure 9b. Transient Response of the Voltage-Controlled Amplifier $V_X = +2$ Volts $V_Y = \pm 1$ Volt

A more detailed description of this circuit, including differential gain and phase characteristics, is given in the application note "Low Cost, Two Chip Voltage-Controlled Amplifier and Video Switch" available from Analog Devices.

BASIC DIVIDER CONNECTIONS

Standard Scaling

The AD539 provides excellent operation as a two-quadrant analog divider in wide-band wide gain-range applications, with the advantage of dual-channel operation. Figure 10a shows the simplest connections for division with a transfer function of

$$V_Y = -V_U V_W / V_X$$

Recalling that the nominal value of V_U is 1V, this can be simplified to

$$V_Y = -V_W / V_X$$

where all signals are expressed in volts. The circuit thus exhibits unity gain for $V_X = +1V$ and a gain of 40dB when $V_X = +0.01V$.

The output swing is limited to ±2V nominal full-scale and ±4.2V peak (using a $-V_S$ supply of at least 7.5V for the AD539). Since the maximum *loss* is 10dB (at $V_X = 3.162V$), it follows that the maximum input to V_W should be ±6.3V (4.4V rms)

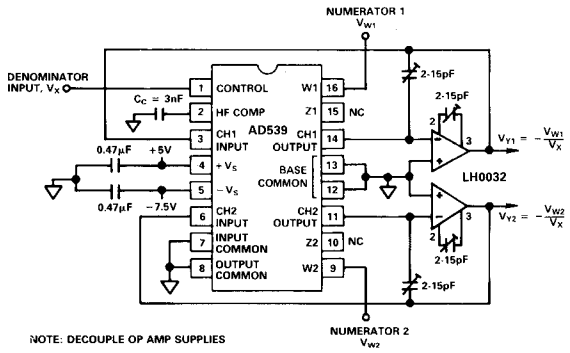


Figure 10a. Two-Channel Divider with 1V Scaling

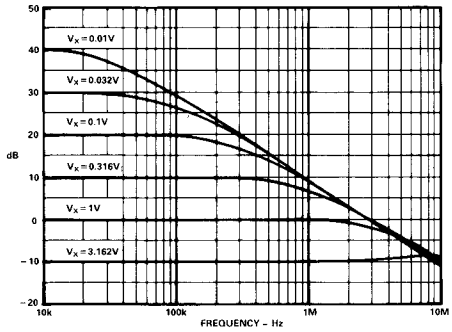


Figure 10b. HF Response of Figure 10a Divider

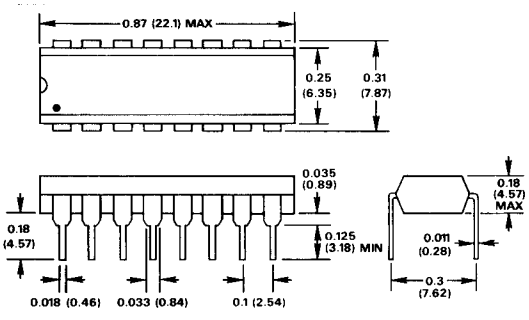
for low distortion applications, and no more than ±13.4V (9.5V rms) to avoid clipping. Note that offset adjustment will be needed for the op amps to maintain accurate dc levels at the output in high gain applications: the "noise gain" is $6V/V_X$, or 600 at $V_X = +0.01V$.

The gain-magnitude response for this configuration using the LH0032 op amps with nominally 12pF compensation (pins 2 to 3) and $C_F = 7pF$ is shown in Figure 10b; of course, other amplifiers may also be used. Since there is some manufacturing variation in the HF response of the op amps, and load conditions will also affect the response, these capacitors should be adjustable: 5-15pF is recommended for both positions. The bandwidth in this configuration is nominally 17MHz at $V_X = +3.162V$, 4.5MHz at $V_X = +1V$, 350kHz at $V_X = +0.1V$ and 35kHz at $V_X = +0.01V$. The general recommendations regarding the use of a good ground plane and power-supply decoupling should be carefully observed. Other suitable high speed op amps include: AD844, AD827 and AD811. Consult these data sheets for suitable applications circuits.

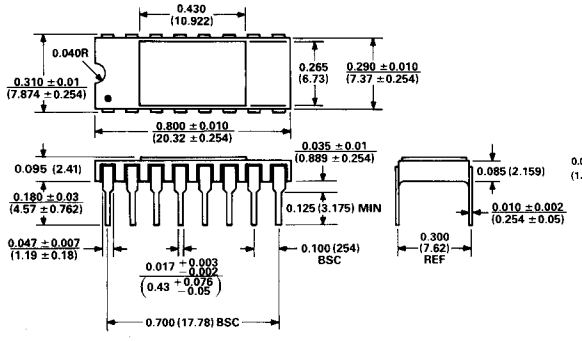
PACKAGE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Plastic (N) Package



TO-116 Ceramic (D) Package



20-Pin LCC (E) Package