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AD829—SPECIFICATIONS (@ $T_A = 25^\circ\text{C}$ and $V_S = \pm 15\text{ V}$ dc, unless otherwise noted.)

Model	Conditions	V_S	AD829JR			AD829AR			AD829AQ/S			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE	T_{MIN} to T_{MAX}	$\pm 5\text{ V}, \pm 15\text{ V}$		0.2	1		0.2	1		0.1	0.5	mV
Offset Voltage Drift		$\pm 5\text{ V}, \pm 15\text{ V}$			1			1			0.5	mV/ $^\circ\text{C}$
INPUT BIAS CURRENT	T_{MIN} to T_{MAX}	$\pm 5\text{ V}, \pm 15\text{ V}$		3.3	7		3.3	7		3.3	7	μA
					8.2			9.5			9.5	μA
INPUT OFFSET CURRENT	T_{MIN} to T_{MAX}	$\pm 5\text{ V}, \pm 15\text{ V}$		50	500		50	500		50	500	nA
Offset Current Drift		$\pm 5\text{ V}, \pm 15\text{ V}$			500			500			500	nA/ $^\circ\text{C}$
OPEN-LOOP GAIN	$V_O = \pm 2.5\text{ V}$ $R_{\text{LOAD}} = 500\ \Omega$ T_{MIN} to T_{MAX} $R_{\text{LOAD}} = 150\ \Omega$ $V_{\text{OUT}} = \pm 10\text{ V}$ $R_{\text{LOAD}} = 1\text{ k}\Omega$ T_{MIN} to T_{MAX} $R_{\text{LOAD}} = 500\ \Omega$	$\pm 5\text{ V}$	30	65		30	65		30	65		V/mV
			20			20			20			V/mV
		$\pm 15\text{ V}$		40			40			40		V/mV
			50	100		50	100		50	100		V/mV
			20			20			20			V/mV
				85			85			85		V/mV
DYNAMIC PERFORMANCE	$V_O = 2\text{ V p-p}$ $R_{\text{LOAD}} = 500\ \Omega$ $V_O = 20\text{ V p-p}$ $R_{\text{LOAD}} = 1\text{ k}\Omega$ $R_{\text{LOAD}} = 500\ \Omega$ $R_{\text{LOAD}} = 1\text{ k}\Omega$ $A_V = -19$ -2.5 V to $+2.5\text{ V}$ 10 V Step $C_{\text{LOAD}} = 10\text{ pF}$ $R_{\text{LOAD}} = 1\text{ k}\Omega$	$\pm 5\text{ V}$		600			600			600		MHz
Gain Bandwidth Product		$\pm 15\text{ V}$		750			750			750		MHz
Full Power Bandwidth ^{1, 2}		$\pm 5\text{ V}$		25			25			25		MHz
		$\pm 15\text{ V}$		3.6			3.6			3.6		MHz
Slew Rate ²		$\pm 5\text{ V}$		150			150			150		V/ μs
		$\pm 15\text{ V}$		230			230			230		V/ μs
Settling Time to 0.1%		$\pm 5\text{ V}$		65			65			65		ns
		$\pm 15\text{ V}$		90			90			90		ns
Phase Margin ²		$\pm 15\text{ V}$		60			60			60		Degrees
DIFFERENTIAL GAIN ERROR ³	$R_{\text{LOAD}} = 100\ \Omega$ $C_{\text{COMP}} = 30\text{ pF}$	$\pm 15\text{ V}$		0.02			0.02			0.02		%
DIFFERENTIAL PHASE ERROR ³	$R_{\text{LOAD}} = 100\ \Omega$ $C_{\text{COMP}} = 30\text{ pF}$	$\pm 15\text{ V}$		0.04			0.04			0.04		Degrees
COMMON-MODE REJECTION	$V_{\text{CM}} = \pm 2.5\text{ V}$ $V_{\text{CM}} = \pm 12\text{ V}$ T_{MIN} to T_{MAX}	$\pm 5\text{ V}$	100	120		100	120		100	120		dB
		$\pm 15\text{ V}$	100	120		100	120		100	120		dB
			96			96			96			dB
POWER SUPPLY REJECTION	$V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$ T_{MIN} to T_{MAX}		98	120		98	120		98	120		dB
			94			94			94			dB
INPUT VOLTAGE NOISE	$f = 1\text{ kHz}$	$\pm 15\text{ V}$		1.7	2		1.7	2		1.7	2	nV/ $\sqrt{\text{Hz}}$
INPUT CURRENT NOISE	$f = 1\text{ kHz}$	$\pm 15\text{ V}$		1.5			1.5			1.5		pA/ $\sqrt{\text{Hz}}$
INPUT COMMON-MODE VOLTAGE RANGE		$\pm 5\text{ V}$		+4.3			+4.3			+4.3		V
				-3.8			-3.8			-3.8		V
		$\pm 15\text{ V}$		+14.3			+14.3			+14.3		V
				-13.8			-13.8			-13.8		V
OUTPUT VOLTAGE SWING	$R_{\text{LOAD}} = 500\ \Omega$ $R_{\text{LOAD}} = 150\ \Omega$ $R_{\text{LOAD}} = 50\ \Omega$ $R_{\text{LOAD}} = 1\text{ k}\Omega$ $R_{\text{LOAD}} = 500\ \Omega$	$\pm 5\text{ V}$	± 3.0	± 3.6		± 3.0	± 3.6		± 3.0	± 3.6		V
		$\pm 5\text{ V}$	± 2.5	± 3.0		± 2.5	± 3.0		± 2.5	± 3.0		V
		$\pm 5\text{ V}$		± 1.4			± 1.4			± 1.4		V
		$\pm 15\text{ V}$	± 12	± 13.3		± 12	± 13.3		± 12	± 13.3		V
		$\pm 15\text{ V}$	± 10	± 12.2		± 10	± 12.2		± 10	± 12.2		V
Short Circuit Current		$\pm 5\text{ V}, \pm 15\text{ V}$		32			32			32		mA
INPUT CHARACTERISTICS												
Input Resistance (Differential)				13			13			13		k Ω
Input Capacitance (Differential) ⁴				5			5			5		pF
Input Capacitance (Common Mode)				1.5			1.5			1.5		pF
CLOSED-LOOP OUTPUT RESISTANCE	$A_V = +1, f = 1\text{ kHz}$			2			2			2		m Ω

Model	Conditions	V _S	AD829JR			AD829AR			AD829AQ/S			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY Operating Range Quiescent Current	T _{MIN} to T _{MAX}	±15 V	±4.5		±18	±4.5		±18	±4.5		±18	V
				5	6.5		5	6.5		5	6.5	mA
		±15 V			8.0			8.0			8.2/8.7	mA
				5.3	6.8		5.3	6.8		5.3	6.8	mA
	T _{MIN} to T _{MAX}				8.3			9.0			8.5/9.0	mA
TRANSISTOR COUNT	Number of Transistors		46			46			46			

NOTES

¹Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.²Tested at Gain = +20, C_{COMP} = 0 pF.³3.58 MHz (NTSC) and 4.43 MHz (PAL and SECAM).⁴Differential input capacitance consists of 1.5 pF package capacitance plus 3.5 pF from the input differential pair.

Specifications subject to change without notice.

AD829

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	±18 V
Internal Power Dissipation ²	
PDIP (N)	1.3 W
SOIC (R)	0.9 W
CERDIP (Q)	1.3 W
LCC (E)	0.8 W
Input Voltage	±V
Differential Input Voltage ³	±6 V
Output Short Circuit Duration	Indefinite
Storage Temperature Range (Q, E)	−65°C to +150°C
Storage Temperature Range (N, R)	−65°C to +125°C
Operating Temperature Range	
AD829J	0°C to 70°C
AD829A	−40°C to +125°C
AD829S	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

² Maximum internal power dissipation is specified so that T_J does not exceed 150°C at an ambient temperature of 25°C.

Thermal characteristics:

8-lead PDIP package: $\theta_{JA} = 100^\circ\text{C/W}$ (derate at 8.7 mW/°C)

8-lead CERDIP package: $\theta_{JA} = 110^\circ\text{C/W}$ (derate at 8.7 mW/°C)

20-lead LCC package: $\theta_{JA} = 77^\circ\text{C/W}$

8-lead SOIC package: $\theta_{JA} = 125^\circ\text{C/W}$ (derate at 6 mW/°C).

³ If the differential voltage exceeds 6 V, external series protection resistors should be added to limit the input current.

METALLIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).

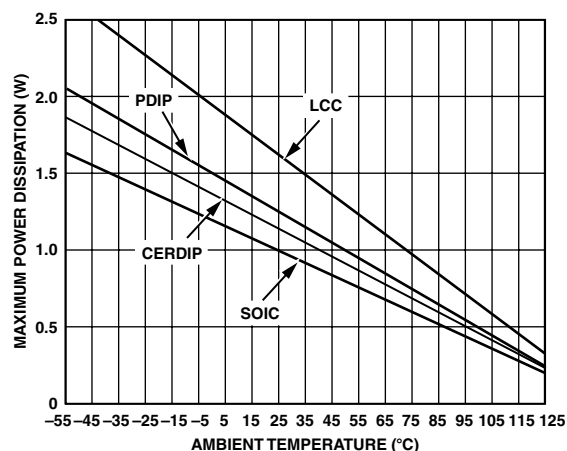
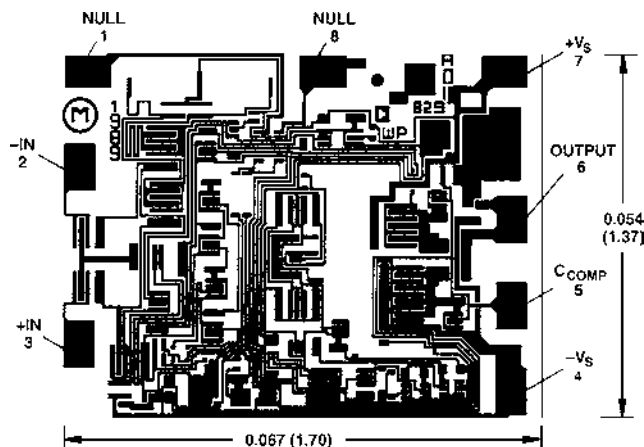


Figure 1. Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD829 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

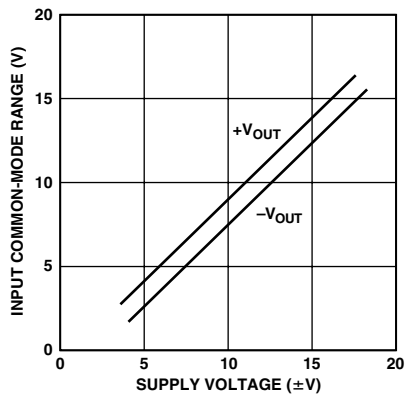


ORDERING GUIDE

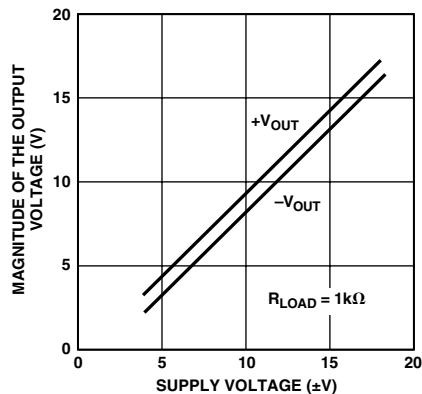
Model	Temperature Range	Package Description	Package Option
AD829AR	−40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829AR-REEL	−40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829AR-REEL7	−40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829ARZ*	−40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829ARZ-REEL*	−40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829ARZ-REEL7*	−40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829JN	0°C to 70°C	8-Lead Plastic PDIP	N-8
AD829JR	0°C to 70°C	8-Lead Plastic SOIC	R-8
AD829JR-REEL	0°C to 70°C	8-Lead Plastic SOIC	R-8
AD829JR-REEL7	0°C to 70°C	8-Lead Plastic SOIC	R-8
AD829AQ	−40°C to +125°C	8-Lead Cerdip	Q-8
AD829SQ	−55°C to +125°C	8-Lead Cerdip	Q-8
AD829SQ/883B	−55°C to +125°C	8-Lead Cerdip	Q-8
5962-9312901MPA	−55°C to +125°C	8-Lead Cerdip	Q-8
AD829SE/883B	−55°C to +125°C	20-Lead LCC	E-20A
5962-9312901M2A	−55°C to +125°C	20-Lead LCC	E-20A
AD829JCHIPS		Die	
AD829SCHIPS		Die	

*Z = Pb-free part.

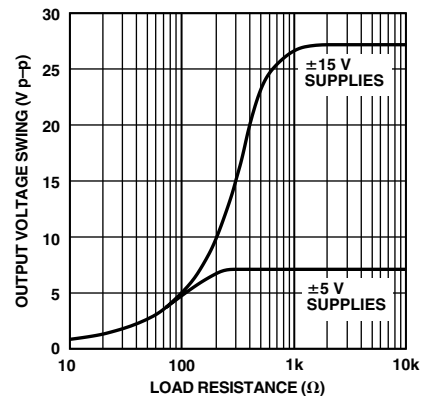
AD829—Typical Performance Characteristics



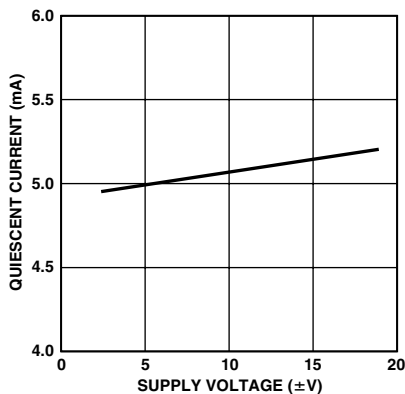
TPC 1. Input Common-Mode Range vs. Supply Voltage



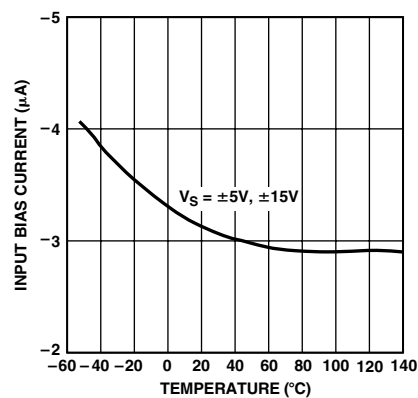
TPC 2. Output Voltage Swing vs. Supply Voltage



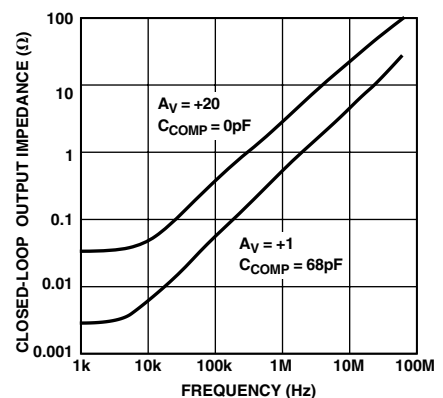
TPC 3. Output Voltage Swing vs. Resistive Load



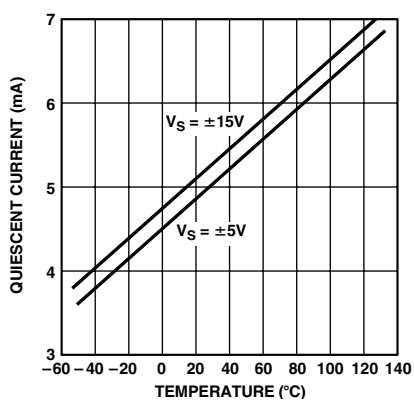
TPC 4. Quiescent Current vs. Supply Voltage



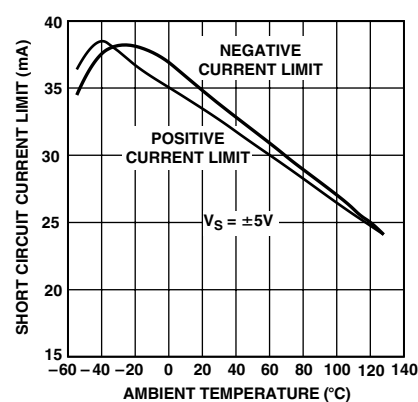
TPC 5. Input Bias Current vs. Temperature



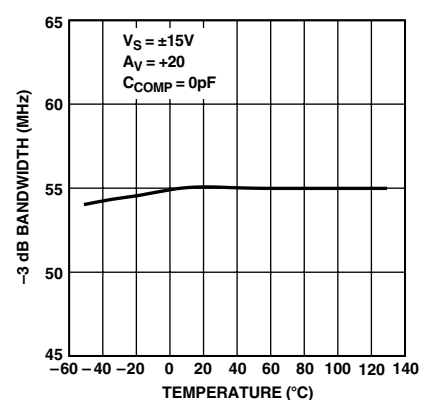
TPC 6. Closed-Loop Output Impedance vs. Frequency



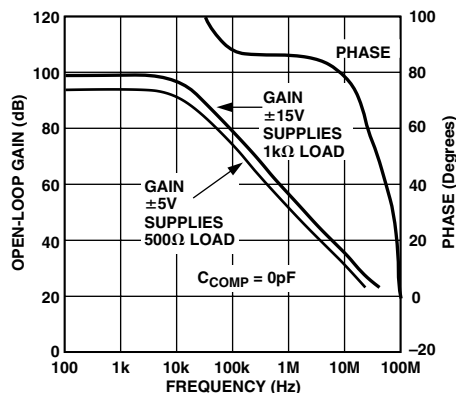
TPC 7. Quiescent Current vs. Temperature



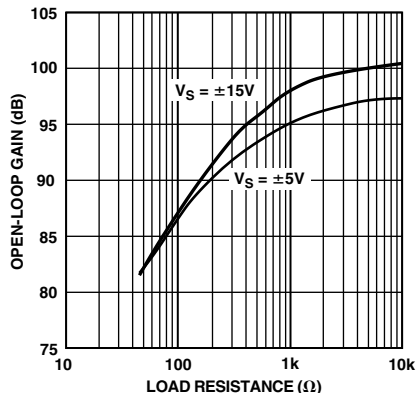
TPC 8. Short-Circuit Current Limit vs. Temperature



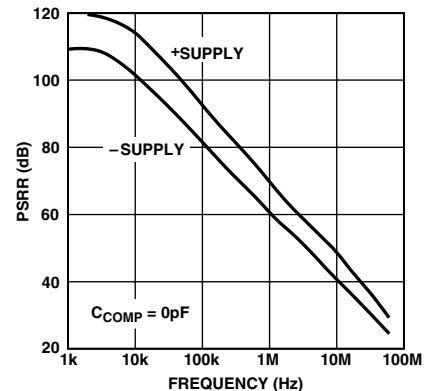
TPC 9. -3 dB Bandwidth vs. Temperature



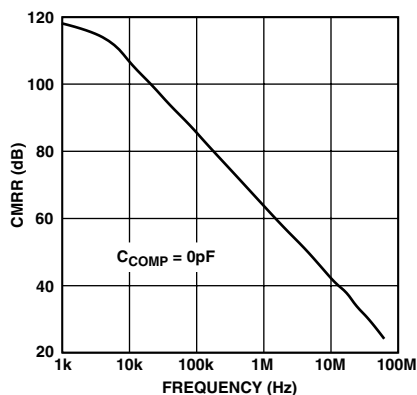
TPC 10. Open-Loop Gain and Phase Margin vs. Frequency



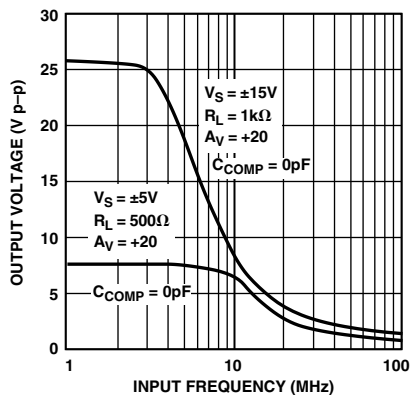
TPC 11. Open-Loop Gain vs. Resistive Load



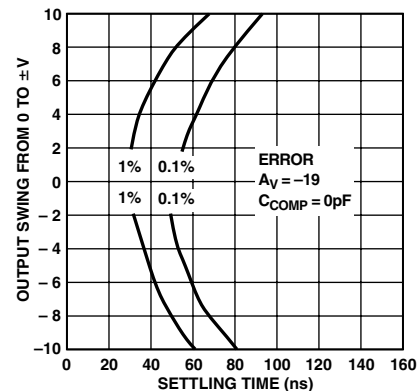
TPC 12. Power Supply Rejection Ratio (PSRR) vs. Frequency



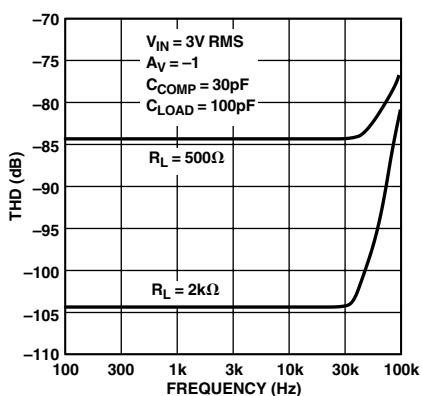
TPC 13. Common-Mode Rejection Ratio vs. Frequency



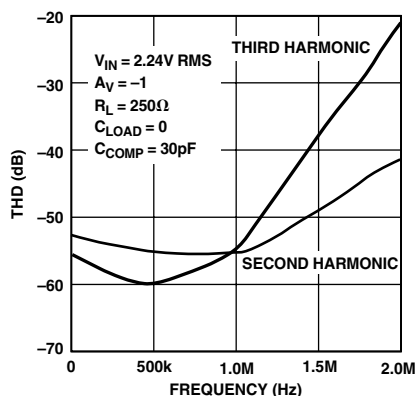
TPC 14. Large Signal Frequency Response



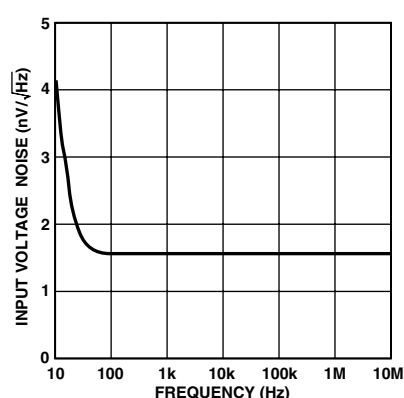
TPC 15. Output Swing and Error vs. Settling Time



TPC 16. Total Harmonic Distortion (THD) vs. Frequency

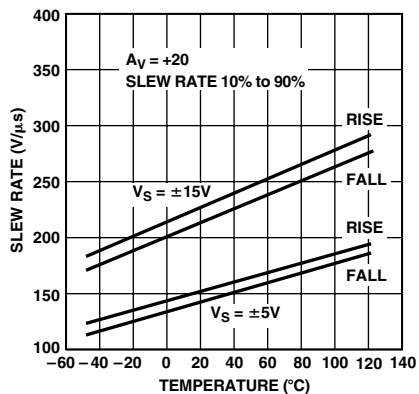


TPC 17. Second and Third Harmonic Distortion vs. Frequency

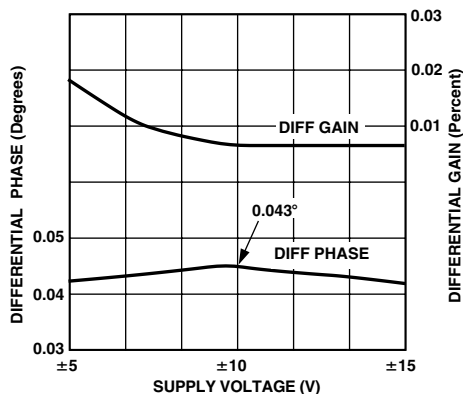


TPC 18. Input Voltage Noise Spectral Density

AD829



TPC 19. Slew Rate vs. Temperature



TPC 20. Differential Gain and Phase vs. Supply

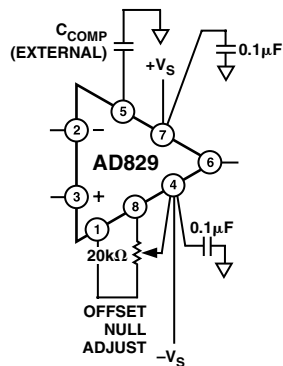


Figure 2. Offset Null and External Shunt Compensation Connections

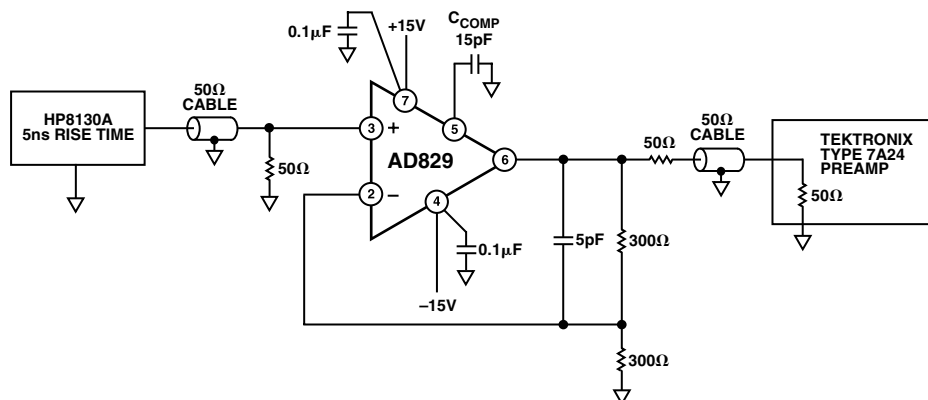


Figure 3a. Follower Connection. Gain = +2

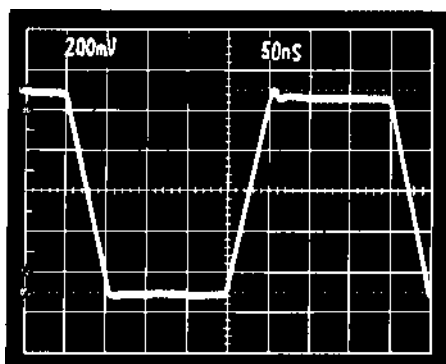


Figure 3b. Gain-of-2 Follower Large Signal Pulse Response

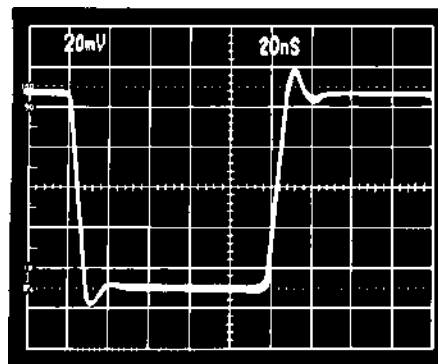


Figure 3c. Gain-of-2 Follower Small Signal Pulse Response

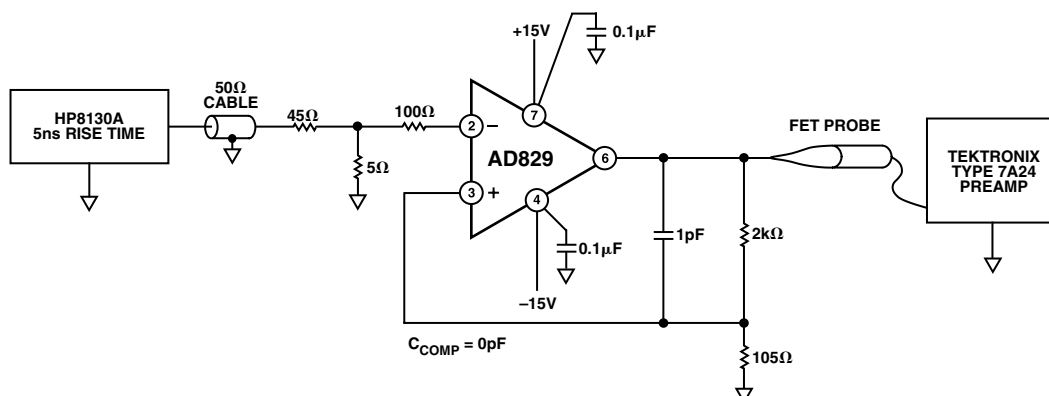


Figure 4a. Follower Connection. Gain = +20

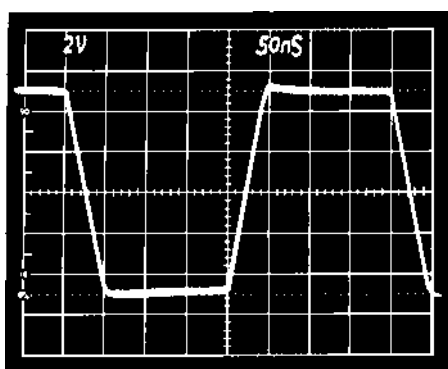
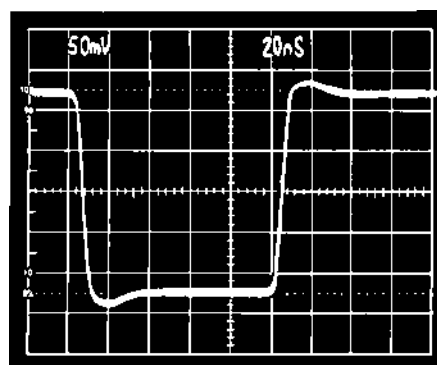
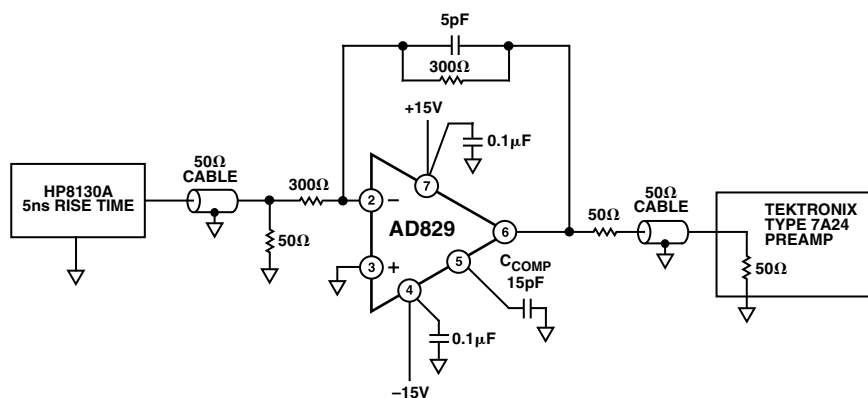
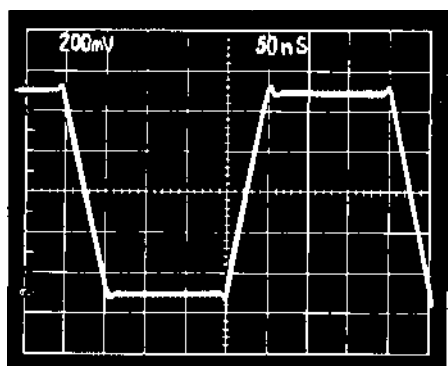
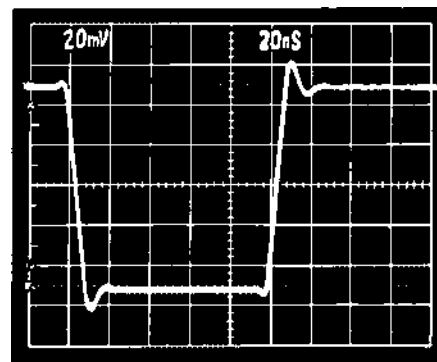
Figure 4b. Gain-of-20 Follower
Large Signal Pulse ResponseFigure 4c. Gain-of-20 Follower
Small Signal Pulse Response

Figure 5a. Unity Gain Inverter Connection

Figure 5b. Unity Gain Inverter
Large Signal Pulse ResponseFigure 5c. Unity Gain Inverter
Small Signal Pulse Response

AD829

THEORY OF OPERATION

The AD829 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process, which provides PNP and NPN transistors with similar f_T s of 600 MHz. As shown in Figure 6, the AD829 input stage consists of an NPN differential pair in which each transistor operates at 600 μ A collector current. This gives the input devices a high transconductance, which in turn gives the AD829 a low noise figure of 2 $\text{nV}/\sqrt{\text{Hz}}$ @ 1 kHz.

The input stage drives a folded cascode that consists of a fast pair of PNP transistors. These PNPs drive a current mirror that provides a differential-input-to-single-ended-output conversion. The high speed PNPs are also used in the current-amplifying output stage, which provides high current gain of 40,000. Even under conditions of heavy loading, the high f_T s of the NPN and PNPs, produced using the CB process, permits cascading two stages of emitter followers while maintaining 60° phase margin at closed-loop bandwidths greater than 50 MHz.

Two stages of complementary emitter followers also effectively buffer the high impedance compensation node (at the C_{COMP} pin) from the output so the AD829 can maintain a high dc open-loop gain, even into low load impedances: 92 dB into a 150 Ω load and 100 dB into a 1 k Ω load. Laser trimming and PTAT biasing ensure low offset voltage and low offset voltage drift, enabling the user to eliminate ac coupling in many applications.

For added flexibility, the AD829 provides access to the internal frequency compensation node. This allows the user to customize frequency response characteristics for a particular application.

Unity gain stability requires a compensation capacitance of 68 pF (Pin 5 to ground), which will yield a small signal bandwidth of 66 MHz and slew rate of 16 V/ μ s. The slew rate and gain bandwidth product will vary inversely with compensation capacitance. Table I and Figure 8 show the optimum compensation capacitance and the resulting slew rate for a desired noise gain. For gains between 1 and 20, C_{COMP} can be chosen to keep the small signal bandwidth relatively constant. The minimum gain that will still provide stability depends on the value of external compensation capacitance.

An RC network in the output stage (Figure 6) completely removes the effect of capacitive loading when the amplifier is compensated for closed-loop gains of 10 or higher. At low frequencies, and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C is bootstrapped and does not contribute to the compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage this reduces the gain, and subsequently, C is incompletely bootstrapped. Therefore, some fraction of C contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is further increased, the bandwidth continues to fall and the amplifier remains stable.

Externally Compensating the AD829

The AD829 is stable with no external compensation for noise gains greater than 20. For lower gains, two different methods of frequency compensating the amplifier can be used to achieve closed-loop stability: shunt and current feedback compensation.

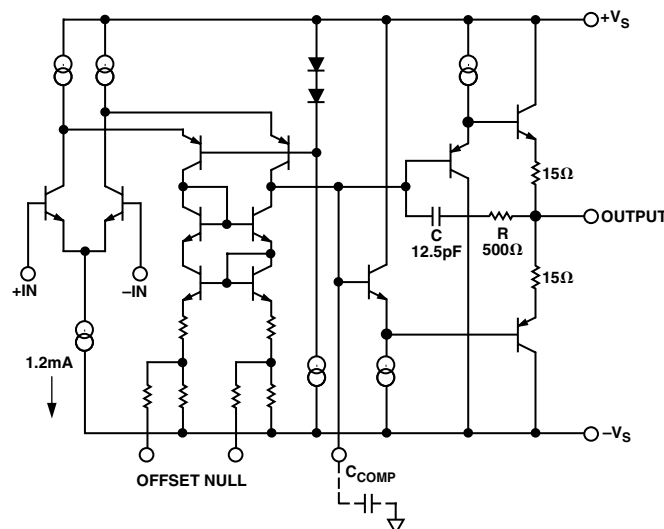


Figure 6. Simplified Schematic

Shunt Compensation

Figures 7 and 8 show that shunt compensation has an external compensation capacitor, C_{COMP} , connected between the compensation pin and ground. This external capacitor is tied in parallel with approximately 3 pF of internal capacitance at the compensation node. In addition, a small capacitance, C_{LEAD} , in parallel with resistor R2, compensates for the capacitance at the amplifier's inverting input.

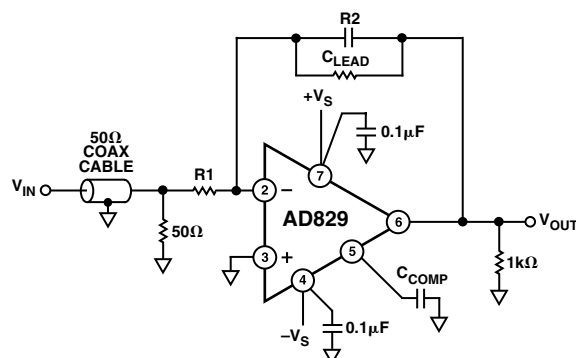


Figure 7. Inverting Amplifier Connection Using External Shunt Compensation

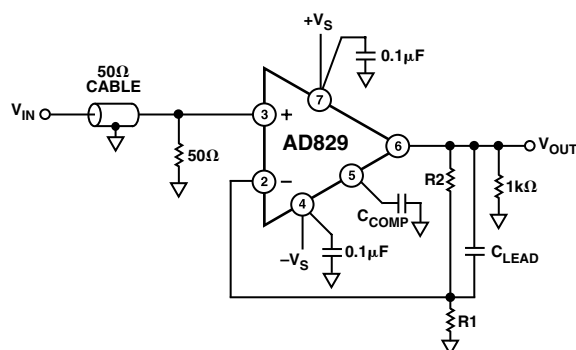
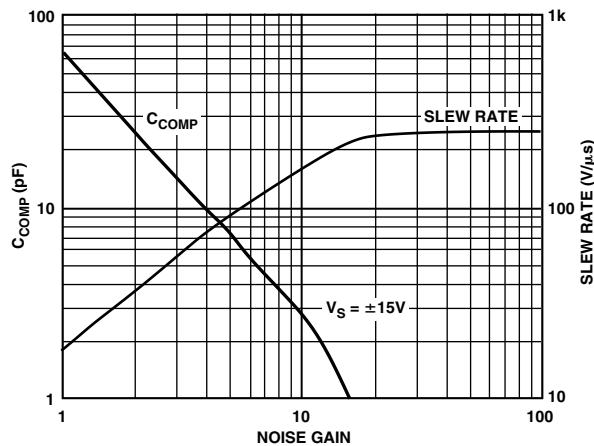


Figure 8. Noninverting Amplifier Connection Using External Shunt Compensation

Table I. Component Selection for Shunt Compensation

Follower Gain	Inverter Gain	R1 (Ω)	R2 (Ω)	C _L (pF)	C _{COMP} (pF)	Slew Rate (V/μs)	-3 dB Small Signal Bandwidth (MHz)
1		Open	100	0	68	16	66
2	-1	1 k	1 k	5	25	38	71
5	-4	511	2.0 k	1	7	90	76
10	-9	226	2.05 k	0	3	130	65
20	-19	105	2 k	0	0	230	55
25	-24	105	2.49 k	0	0	230	39
100	-99	20	2 k	0	0	230	7.5

Table I gives the recommended C_{COMP} and C_{LEAD} values, as well as the corresponding slew rates and bandwidth. The capacitor values were selected to provide a small signal frequency response with less than 1 dB of peaking and less than 10% overshoot. For this table, supply voltages of ± 15 V should be used. Figure 9 is a graphical extension of the table that shows the slew rate/gain trade-off for lower closed-loop gains, when using the shunt compensation scheme.

Figure 9. Value of C_{COMP} and Slew Rate vs. Noise Gain

Current Feedback Compensation

Bipolar, nondegenerated, single pole, and internally compensated amplifiers have their bandwidths defined as

$$f_T = \frac{1}{2\pi r_e C_{COMP}} = \frac{I}{2\pi \frac{kT}{q} C_{COMP}}$$

where

f_T is the unity gain bandwidth of the amplifier.

I is the collector current of the input transistor.

C_{COMP} is the compensation capacitance.

r_e is the inverse of the transconductance of the input transistors. kT/q approximately equals 26 mV @ 27°C.

Since both f_T and slew rate are functions of the same variables, the dynamic behavior of an amplifier is limited. Since

$$\text{Slew Rate} = \frac{2I}{C_{COMP}}$$

then

$$\frac{\text{Slew Rate}}{f_T} = 4\pi \frac{kT}{q}$$

This shows that the slew rate will be only 0.314 V/μs for every MHz of bandwidth. The only way to increase slew rate is to increase the f_T , and that is difficult because of process limitations. Unfortunately, an amplifier with a bandwidth of 10 MHz can only slew at 3.1 V/μs, which is barely enough to provide a full power bandwidth of 50 kHz.

The AD829 is especially suited to a new form of compensation that allows for the enhancement of both the full power bandwidth and slew rate of the amplifier. The voltage gain from the inverting input pin to the compensation pin is large; therefore, if a capacitance is inserted between these pins, the amplifier's bandwidth becomes a function of its feedback resistor and the capacitance. The slew rate of the amplifier is now a function of its internal bias (2I) and the compensation capacitance.

Since the closed-loop bandwidth is a function of R_F and C_{COMP} (Figure 10), it is independent of the amplifier closed-loop gain, as shown in Figure 12. To preserve stability, the time constant of R_F and C_{COMP} needs to provide a bandwidth of less than 65 MHz. For example, with $C_{COMP} = 15$ pF and $R_F = 1$ kΩ, the small signal bandwidth of the AD829 is 10 MHz. Figure 11 shows that the slew rate is in excess of 60 V/μs. As shown in Figure 12, the closed-loop bandwidth is constant for gains of -1 to -4; this is a property of current feedback amplifiers.

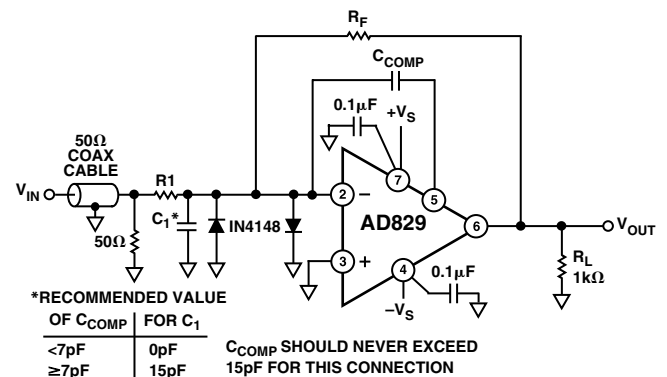


Figure 10. Inverting Amplifier Connection Using Current Feedback Compensation

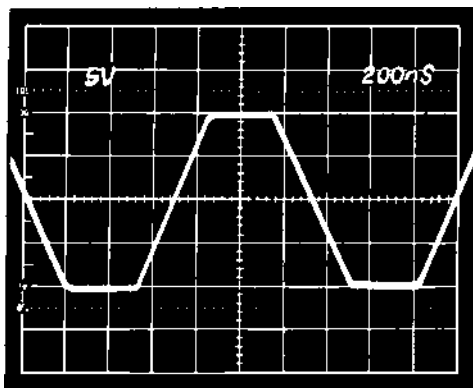


Figure 11. Large Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation, $C_{COMP} = 15 \text{ pF}$, $C_1 = 15 \text{ pF}$, $R_F = 1 \text{ k}\Omega$, $R_1 = 1 \text{ k}\Omega$

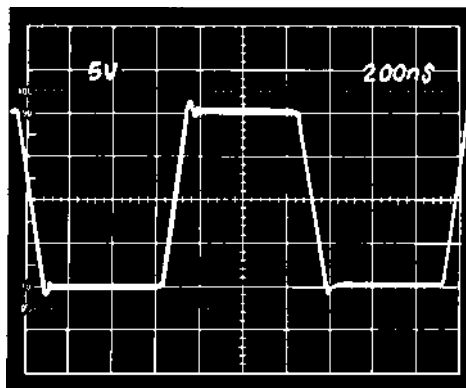


Figure 13. Large Signal Pulse Response of the Inverting Amplifier Using Current Feedback Compensation, $C_{COMP} = 1 \text{ pF}$, $R_F = 3 \text{ k}\Omega$, $R_1 = 3 \text{ k}\Omega$

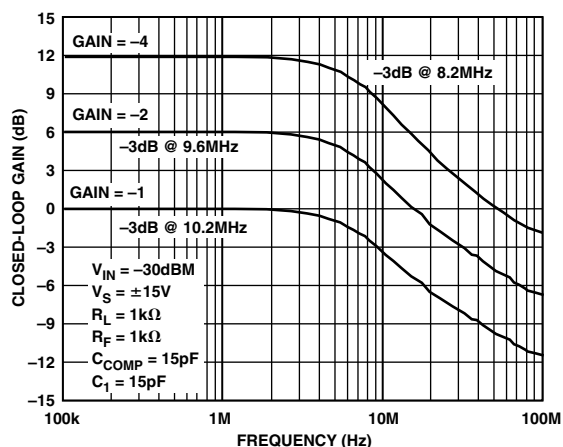


Figure 12. Closed-Loop Gain vs. Frequency for the Circuit of Figure 9

Figure 13 is an oscilloscope photo of the pulse response of a unity gain inverter that has been configured to provide a small signal bandwidth of 53 MHz and a subsequent slew rate of 180 V/ μ s; resistor $R_F = 3 \text{ k}\Omega$ and capacitor $C_{COMP} = 1 \text{ pF}$. Figure 14 shows the excellent pulse response as a unity gain inverter, this using component values of $R_F = 1 \text{ k}\Omega$ and $C_{COMP} = 4 \text{ pF}$.

Figures 15 and 16 show the closed-loop frequency response of the AD829 for different closed-loop gains and different supply voltages.

If a noninverting amplifier configuration using current feedback compensation is needed, the circuit of Figure 17 is recommended. This circuit provides a slew rate twice that of the shunt compensated noninverting amplifier of Figure 18 at the expense of gain flatness. Nonetheless, this circuit delivers 95 MHz bandwidth with $\pm 1 \text{ dB}$ flatness into a back terminated cable, with a differential gain error of only 0.01% and a differential phase error of only 0.015° at 4.43 MHz.

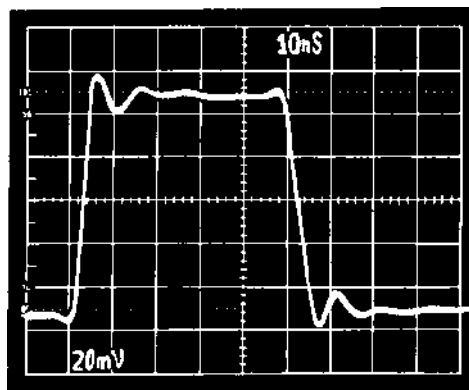


Figure 14. Small Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation, $C_{COMP} = 4 \text{ pF}$, $R_F = 1 \text{ k}\Omega$, $R_1 = 1 \text{ k}\Omega$

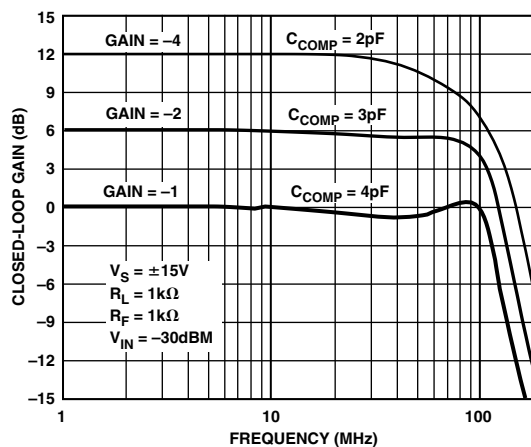


Figure 15. Closed-Loop Frequency Response for the Inverting Amplifier Using Current Feedback Compensation

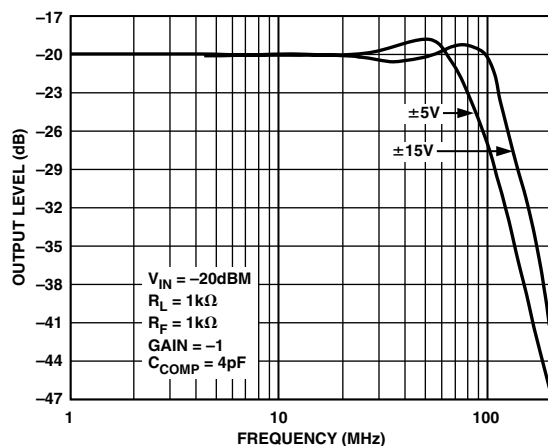


Figure 16. Closed-Loop Frequency Response vs. Supply for the Inverting Amplifier Using Current Feedback Compensation

A Low Error Video Line Driver

The buffer circuit shown in Figure 18 will drive a back-terminated 75 Ω video line to standard video levels (1 V p-p) with 0.1 dB gain flatness to 30 MHz with only 0.04° and 0.02% differential phase and gain at the 4.43 MHz PAL color subcarrier frequency. This level of performance, which meets the requirements for high definition video displays and test equipment, is achieved using only 5 mA quiescent current.

A High Gain, Video Bandwidth, Three Op Amp In Amp

Figure 19 shows a three op amp instrumentation amplifier circuit that provides a gain of 100 at video bandwidths. At a circuit gain of 100, the small signal bandwidth equals 18 MHz into a FET probe. Small signal bandwidth equals 6.6 MHz with a 50 Ω load. The 0.1% settling time is 300 ns.

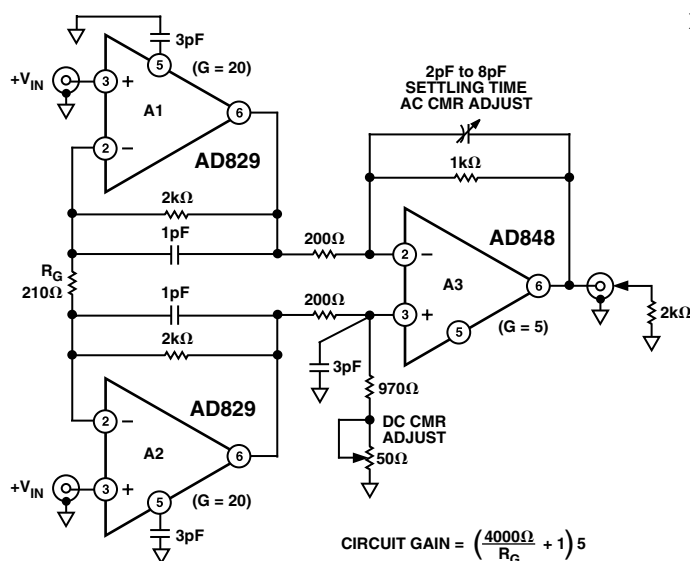


Figure 19. A High Gain, Video Bandwidth, Three Op Amp In Amp Circuit

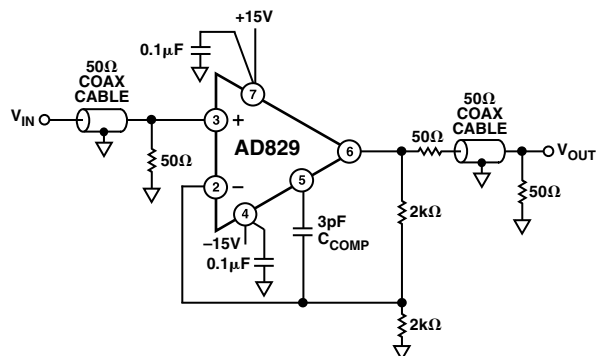


Figure 17. Noninverting Amplifier Connection Using Current Feedback Compensation

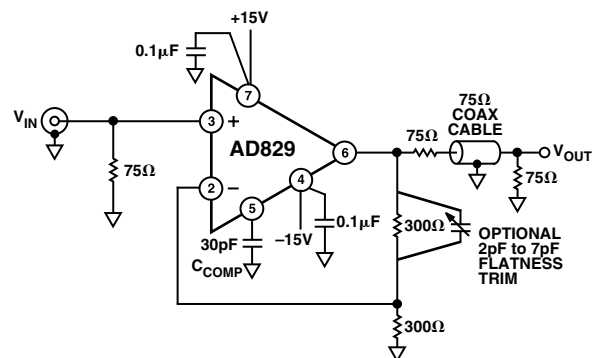
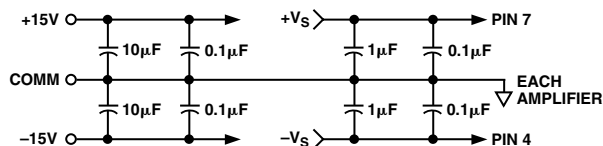


Figure 18. A Video Line Driver with a Flatness over Frequency Adjustment

The input amplifiers operate at a gain of 20, while the output op amp runs at a gain of 5. In this circuit, the main bandwidth limitation is the gain/bandwidth product of the output amplifier. Extra care should be taken while breadboarding this circuit, since even a couple of extra picofarads of stray capacitance at the compensation pins of A1 and A2 will degrade circuit bandwidth.

INPUT FREQUENCY	CMRR
100 Hz	64.6dB
1 MHz	44.7dB
10 MHz	23.9dB

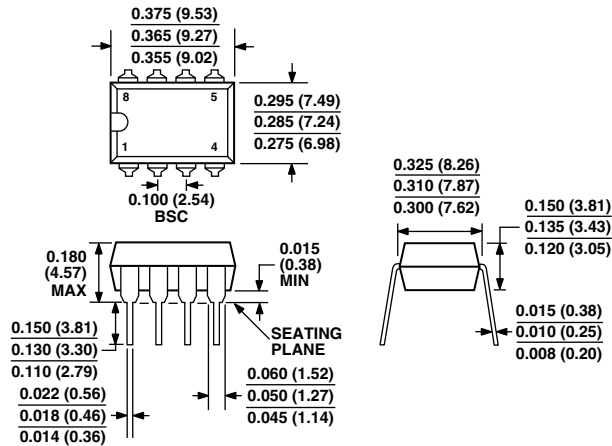


OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]

(N-8)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA

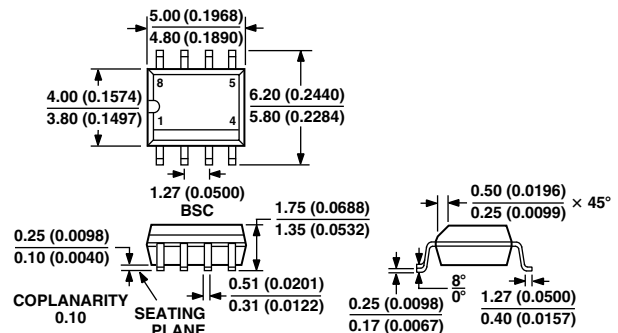
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC]

Narrow Body

(R-8)

Dimensions shown in millimeters and (inches)



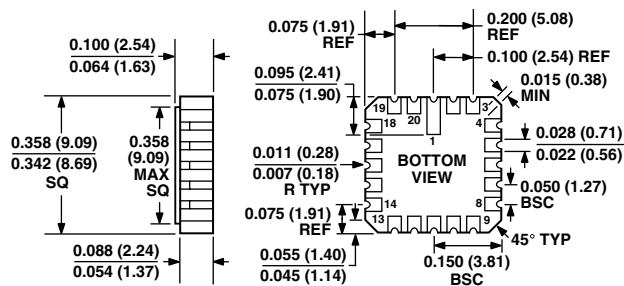
COMPLIANT TO JEDEC STANDARDS MS-012AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

20-Terminal Ceramic Leadless Chip Carrier [LCC]

(E-20A)

Dimensions shown in inches and (millimeters)

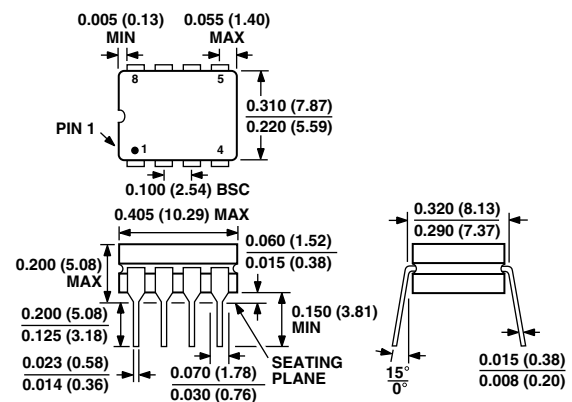


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8-Lead Ceramic Dual In-Line Package [CERDIP]

(Q-8)

Dimensions shown in inches and (millimeters)



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Revision History

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4/04—Data Sheet changed from REV. F to REV. G.	
Added new Figure 1 and renumbered all figures	4
Changes to ORDERING GUIDE	5
Updated Table I	11
Updated Figure 15	12
Updated Figure 16	13
Updated OUTLINE DIMENSIONS	14
2/03—Data Sheet changed from REV. E to REV. F.	
Renumbered Figures	Universal
Changes made to PRODUCT HIGHLIGHTS	1
Changes made to SPECIFICATIONS	2
Changes made to ABSOLUTE MAXIMUM RATINGS	4
Changes made to ORDERING GUIDE	4
Updated OUTLINE DIMENSIONS	13

