Data Sheet | July 1999 | File Number 4612.1

Radiation Hardened Octal Three-State Buffer/Line Driver

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil ACTS541T is a Radiation Hardened Octal Buffer/Line Driver, with three-state outputs. The output enable pins $\overline{OE1}$, $\overline{OE2}$ control the three-state outputs. If either enable is high the output will be in a high impedance state. For data output both enables must be low.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACTS541T are contained in SMD 5962-96726. A "hot-link" is provided from our website for downloading**.**
www.intersil.com/spacedefense/newsafclasst.asp

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.semi.intersil.com/quality/manuals.asp

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^oC)
5962R9672602TRC	ACTS541DTR-02	-55 to 125
5962R9672602TXC	ACTS541KTR-02	-55 to 125

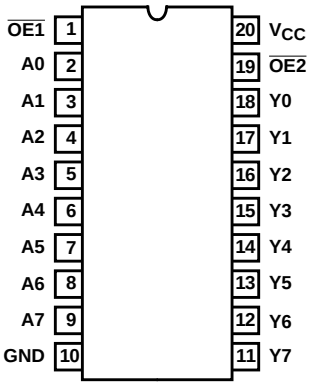
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct***.

Features

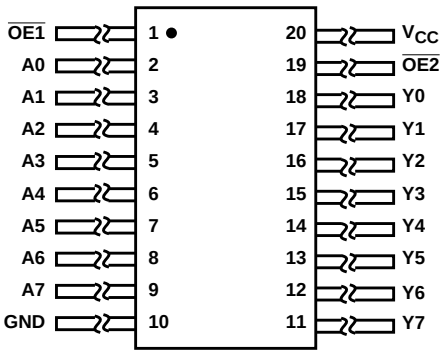
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - Latch-Up Free Under Any Conditions
  - Single Event Upset (SEU) Immunity: <1 x 10^{-10} Errors/Bit/Day (Typ)
  - SEU LET Threshold . . . . . .>100 MEV-cm^2/mg
- 1.25 Micron Radiation Hardened SOS CMOS
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range. . . . . 4.5V to 5.5V
- Input Logic Levels
  - V_{IL} = 0.8V Max
  - V_{IH} = VCC/2 Min
- Fast Propagation Delay . . . . . 21ns (Max), 14ns (Typ)

Pinouts

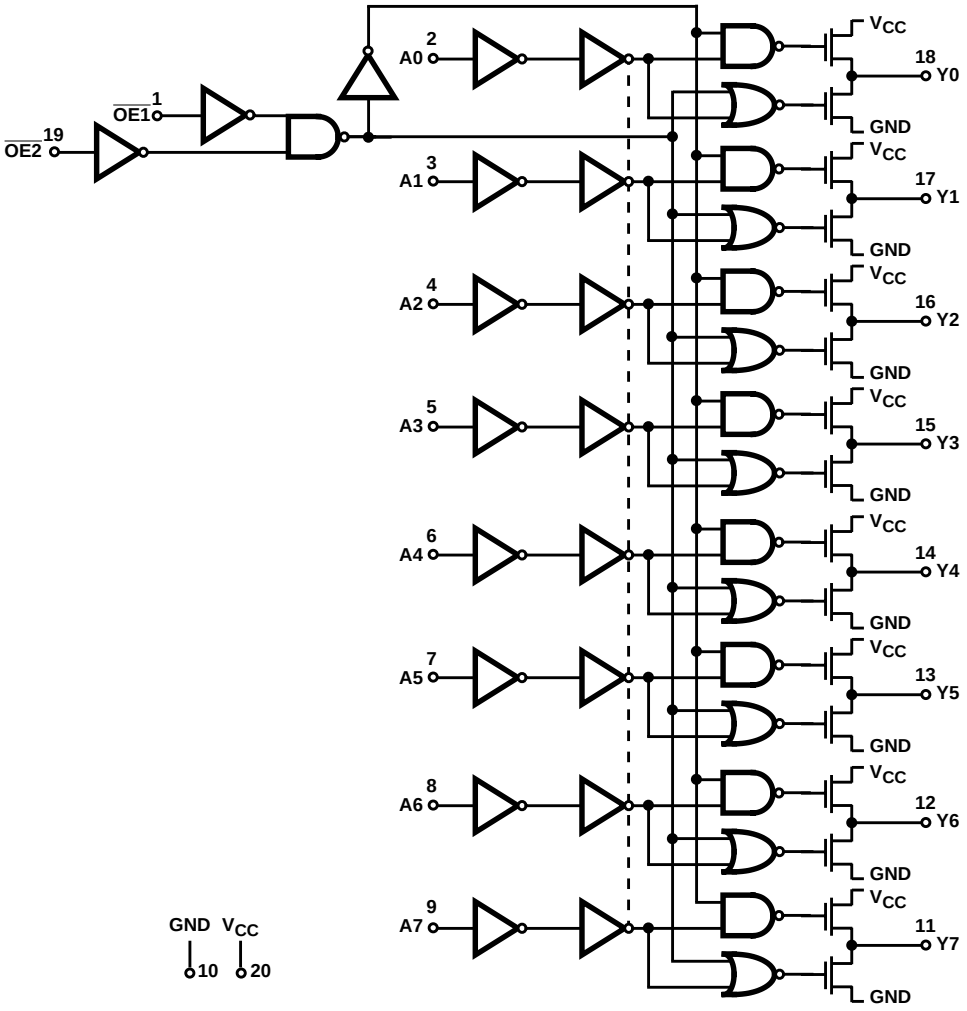
ACTS541T (SBDIP), CDIP2-T20
TOP VIEW



ACTS541T (FLATPACK), CDFP4-F20
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE1}$	$\overline{OE2}$	An	Yn
L	L	H	H
L	L	L	L
H	X	X	Z
X	H	X	Z

NOTE: L = Low Logic Level, H = High Logic Level, Z = High Impedance.

Die Characteristics

DIE DIMENSIONS:

(2600µm x 2600µm x 533µm ±51µm)

102 x 102 x 21mils ±2mil

METALLIZATION:

Type: Al Si Cu

Thickness: 10.0kÅ ±2kÅ

SUBSTRATE POTENTIAL:

Unbiased (Silicon on Sapphire)

Bond Pad #20 (V_{CC}) First

BACKSIDE FINISH:

Sapphire

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 8.0kÅ ±1.0kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

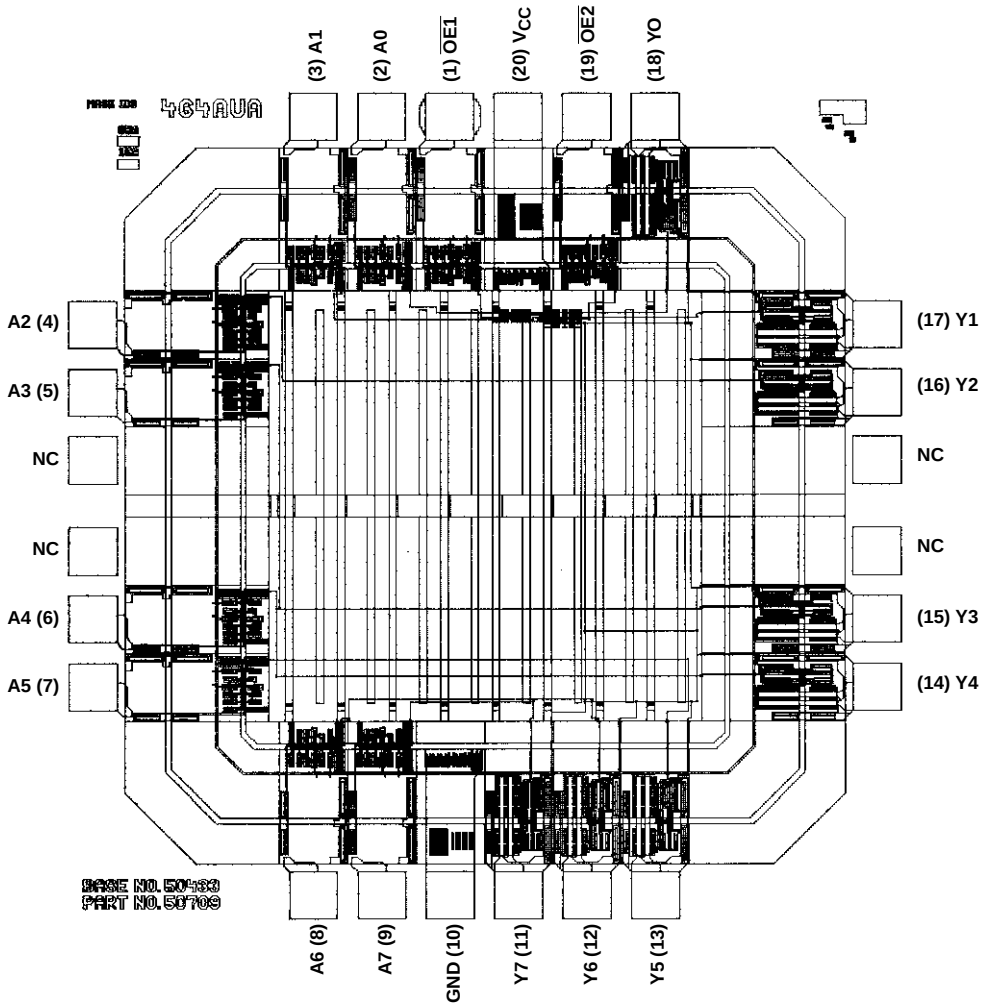
182

PROCESS:

CMOS SOS

Metallization Mask Layout

ACTS541T



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.