

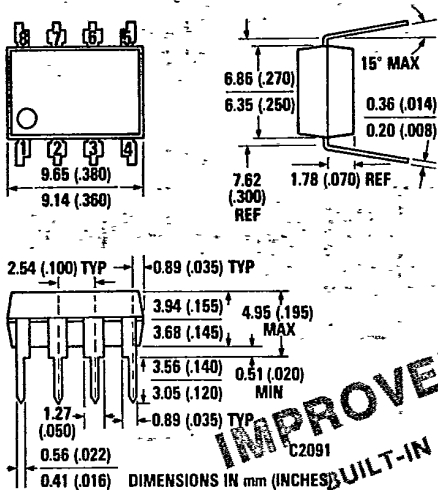
GENERAL INSTRUMENT

VERY HIGH-SPEED LOGIC GATE OPTOCOUPLED

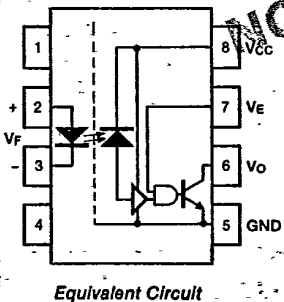
Optocouplers

6N137 10 Mbit/s LOGIC GATE MCL2601 (HCPL-2601)

PACKAGE DIMENSIONS



IMPROVED!
BUILT-IN NOISE SHIELD



TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

A 0.1µF bypass capacitor must be connected between pins 8 and 5. (See note 1)

DESCRIPTION

The 6N137 and MCL/HCPL-2601 single-channel optocouplers consists of a 700 nm GaAsP LED, optically coupled to a very high speed integrated photodetector logic gate with a strobable output. This output features an open collector, thereby permitting wired-OR outputs. The coupled parameters are guaranteed over the temperature range of 0-70°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan-out of 8).

An internal noise shield provides superior common mode rejection of typically 10 kV/µs. The MCL/HCPL-2601 has a minimum CMR of 1 kV/µs.

An improved package allows superior insulation, permitting a 480 V working voltage compared to industry standard 220 V.

FEATURES

- Very high speed — 10 MBit/s
- Superior CMR — 10 k V/µs
- Superior insulation — 2500 V RMS 1 min.
- Double working voltage — 480 V
- Fan-out of 8 over 0-70°C
- Logic gate output
- Stroable output
- Wired-OR — open collector
- U.L. recognized (File #E50151)

APPLICATIONS

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

ABSOLUTE MAXIMUM RATING

- Storage temperature -55°C to + 125°C
- Operating temperature 0°C to + 70°C
- Lead solder temperature 260°C for 10 s
- DC/average forward input current 20 mA
- Enable input voltage, (VE) (Not to exceed Vcc by more than 500 mV) ... 5.5 V

- Reverse input voltage 5.0 V
- Reverse supply voltage (-Vcc) -500 mV
- Supply voltage, (Vcc) 7.0 V/1 minute maximum
- Output current, (Io) 25 mA
- Output voltage, (Vo) 7.0 V
- Collector output power dissipation 40 mW

6N137 MCL2601 (HCPL-2601)

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RECOMMENDED OPERATING CONDITIONS

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	SYMBOL	MIN.	MAX.	UNITS
Input current, low level	I _{FL}	0	250	μA
Input current, high level	I _{FH}	*6.3	15	mA
Supply voltage, output	V _{CC}	4.5	5.5	V
Enable voltage low level	V _{EL}	0	0.8	V
Enable voltage high level	V _{EH}	2.0	V _{CC}	V
Operating temperature	T _A	0	70	°C
Fan out (TTL load)	N		8	

*6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

ELECTRICAL CHARACTERISTICS (T_A = 0° C to 70° C Unless Otherwise Specified)

PARAMETER	SYM.	TEST CONDITIONS	6N137			MCL(HCPL)-2601			UNITS
			MIN.	TYP.**	MAX.	MIN.	TYP.*	MAX.	
High level output current	I _{OH}	V _{CC} = 5.5 V, V _O = 5.5 V I _F = 250 μA, V _E = 2.0 V		.02	250*		.02	250	μA
Low level output voltage	V _{OL}	V _{CC} = 5.5 V, I _F = 5 mA V _E = 2.0 V, I _{OL} = 13 mA		.34	0.6*		.34	0.6	V
High level supply current	I _{CCH}	V _{CC} = 5.5 V, I _F = 0 mA V _E = 0.5 V		10	15*		10	15	mA
Low level supply current	I _{CCL}	V _{CC} = 5.5 V, I _F = 10 mA V _E = 0.5 V		15	18*		15	18	mA
Low level enable current	I _{EL}	V _{CC} = 5.5 V, V _E = 0.5 V		-1.5	-2.0*		-1.5	-2.0	mA
High level enable current	I _{EH}	V _{CC} = 5.5 V, V _E = 2.0 V		-1.0			-1.0		mA
High level enable voltage	V _{EH}	V _{CC} = 5.5 V, I _F = 10 mA	2.0			2.0			V
Low level enable voltage	V _{EL}	Note: 11			0.8			0.8	V
Input forward voltage	V _F	I _F = 10 mA, T _A = 25° C		1.55	1.75*		1.55	1.75	V
Input reverse breakdown voltage	B _{VR}	I _R = 10 μA, T _A = 25° C	5.0*			5.0			V
Input capacitance	C _{IN}	V _F = 0, f = 1 MHz		60			60		pF
Input diode temperature coefficient	ΔV _F /ΔT _A	I _F = 10 mA		-1.4			-1.4		mV/°C
Input-output insulation leakage current	I _{I-O}	Relative humidity = 45% T _A = 25° C, t = 5 s V _{I-O} = 3000 VDC Note: 10			1.0*			1.0	μA
Withstand insulation test voltage	V _{ISO}	RH < 50 % T _A = 25° C t = 1 min.	2500			2500			V _{RMS}
Resistance (input to output)	R _{I-O}	V _{I-O} = 500 V, Note: 10		10 ¹²			10 ¹²		Ω
Capacitance (input to output)	C _{I-O}	f = 1 MHz, Note: 10		0.6			0.6		pF

SWITCHING CHARACTERISTICS (TA = 25°C, VCC = 5.0 V)

PARAMETER	SYM.	TEST CONDITIONS	6N137			MCL(HCPL)-2601			UNITS
			MIN.	TYP.**	MAX.	MIN.	TYP.*	MAX.	
Propagation delay time (For output high level)	TPLH			48	75*		48	75	ns
Propagation delay time (For output low level)	TPHL	RL = 350 Ω CL = 15 pF		48	75*		48	75	ns
Output rise time (10-90%)	tr	IF = 7.5 mA		30			30		ns
Output fall time (90-10%)	tf	Notes 2, 3, 4 & 5, Figure 10		14			14		ns
Enable propagation delay time (For output high level)	TELH	IF = 7.5 mA VEH = 3.0 V VEL = 0 V		25			25		ns
Enable propagation delay time (For output low level)	TEHL	RL = 350 Ω, CL = 15 pF Notes 6 & 7, Figure 11		14			14		ns
Common mode transient immunity (At output high level)	CMH	VCM = 50 V (Peak) IF = 0 mA, VOH (Min.) = 2.0 V RL = 350 Ω, Note 9 Figure 16, 15		10,000		1000	10,000		V/μs
Common mode transient immunity (At output low level)	CML	VCM = 50 V (Peak) IF = 7.5 mA, VOL (Max.) = 0.8 V RL = 350 Ω Note 8, Figure 16, 15		-10,000		-1000	-10,000		V/μs

*JEDEC Registered Data

**All typical values are at VCC = 5 V, TA = 25°C.

TYPICAL CHARACTERISTIC CURVES (TA = 25°C Unless Otherwise Specified)

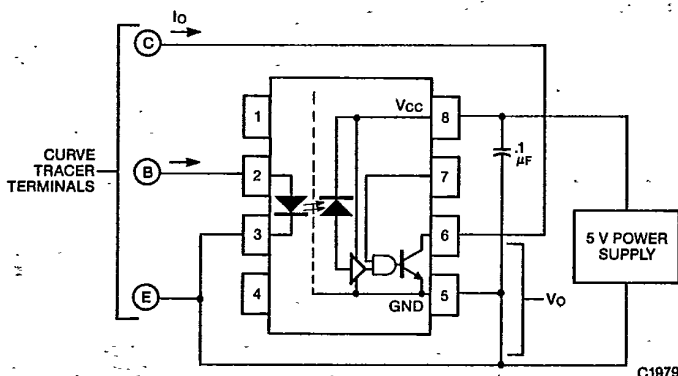


Fig. 1. Curve Tracer Connection to Obtain Collector Characteristics

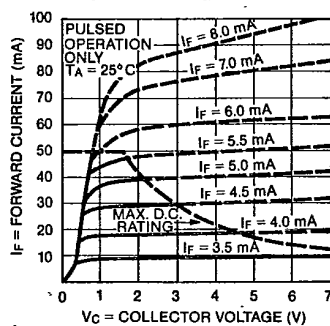


Fig. 2. Optocoupler Collector Characteristics

Optocouplers

6N137 MCL2601 (HCPL-2601)

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TYPICAL CHARACTERISTIC CURVES ($T_A = 25^\circ\text{C}$ Unless Otherwise Specified)

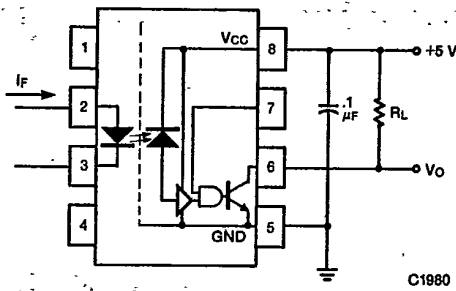


Fig. 3. Input-Output Schematic

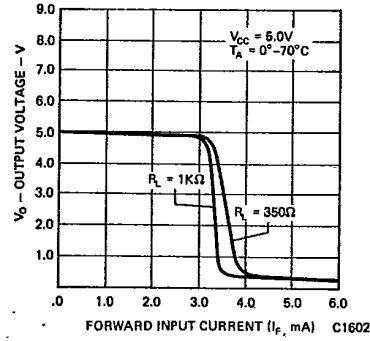


Fig. 4. Output Voltage vs. Forward Input Current

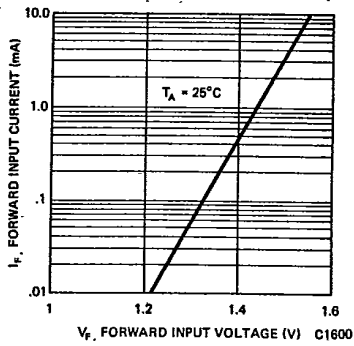


Fig. 5. Forward Input Current vs. Forward Input Voltage

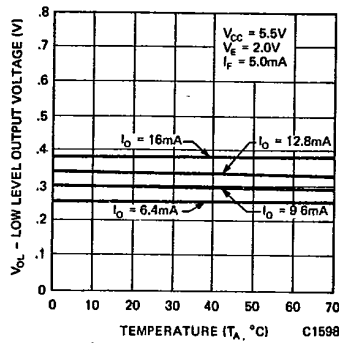


Fig. 6. Low Level Output Voltage vs. Temperature

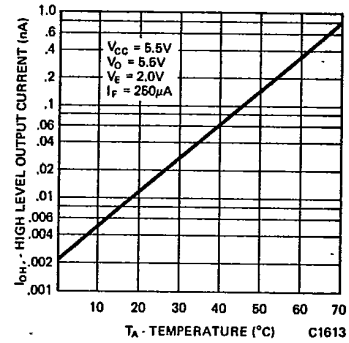


Fig. 7. High Level Output Current vs. Temperature

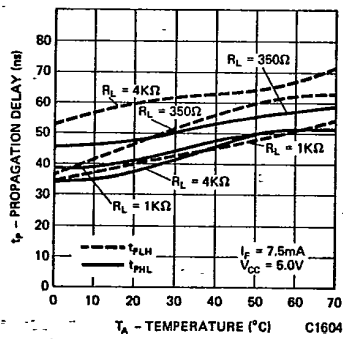


Fig. 8. Propagation Delay vs. Temperature

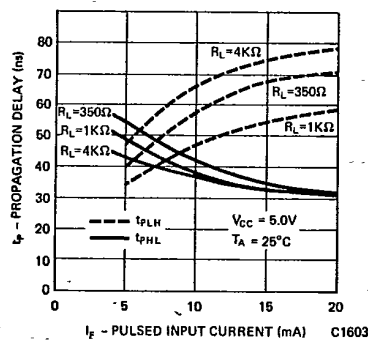


Fig. 9. Propagation Delay vs. Pulse Input Current

TYPICAL CHARACTERISTIC CURVES (T_A = 25°C Unless Otherwise Specified)

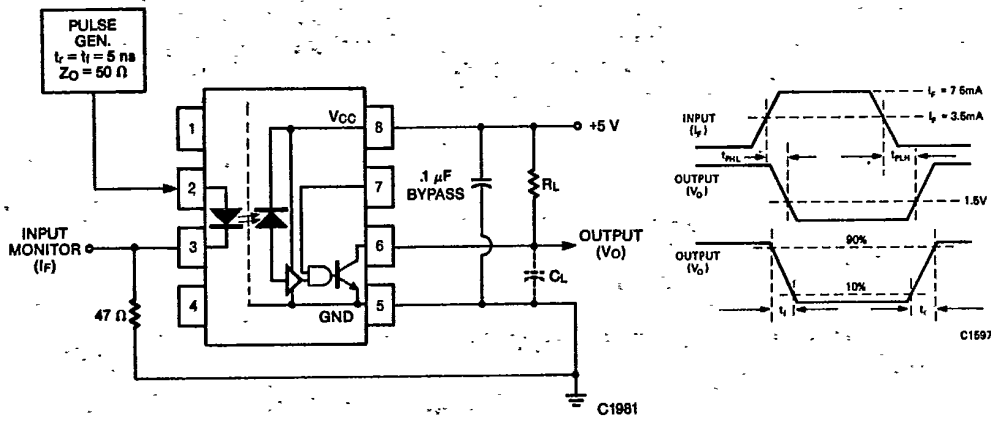


Fig. 10. Test Circuit and Waveforms for t_{PLH}, t_P, and t_F

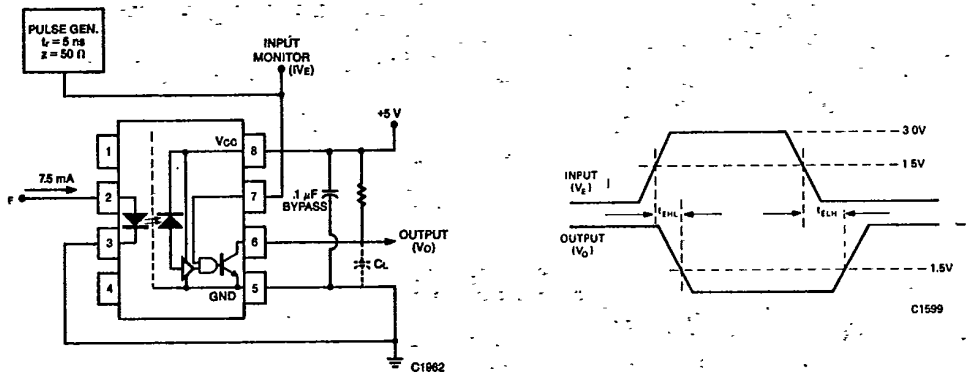


Fig. 11. Test Circuit t_{EHL} and t_{ELH}

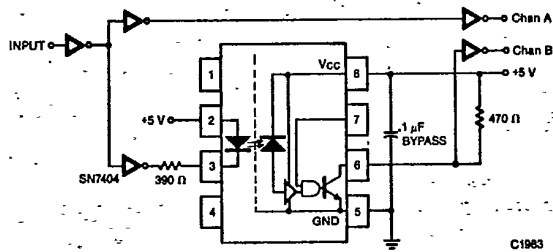


Fig. 12. Response Delay Between TTL Gates

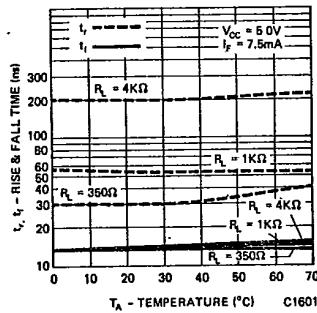


Fig. 13. Rise and Fall Time vs. Temperature

