CMOS
TIA IS-54 Baseband Receive Port

AD7013

FEATURES
Single +5 V Supply
Receive Channel
Differential or Single-Ended Analog Inputs
Auxiliary Set of Analog I & Q Inputs
Two Sigma-Delta A/D Converters
Choice of Two Digital FIR Filters
Root-Raised-Cosine Rx Filters, α = 0.35
Brick Wall FIR Rx Filters
On-Chip or User Rx Offset Calibration
ADC Sampling Vernier
Three Auxiliary DACs
On-Chip Voltage Reference
Low Active Power Dissipation, Typical 45 mW
Low Sleep Mode Power Dissipation, <50 μW
28-Pin SSOP

APPLICATIONS
American TIA Digital Cellular Telephony
American Analog Cellular Telephony
Digital Baseband Receivers

GENERAL DESCRIPTION

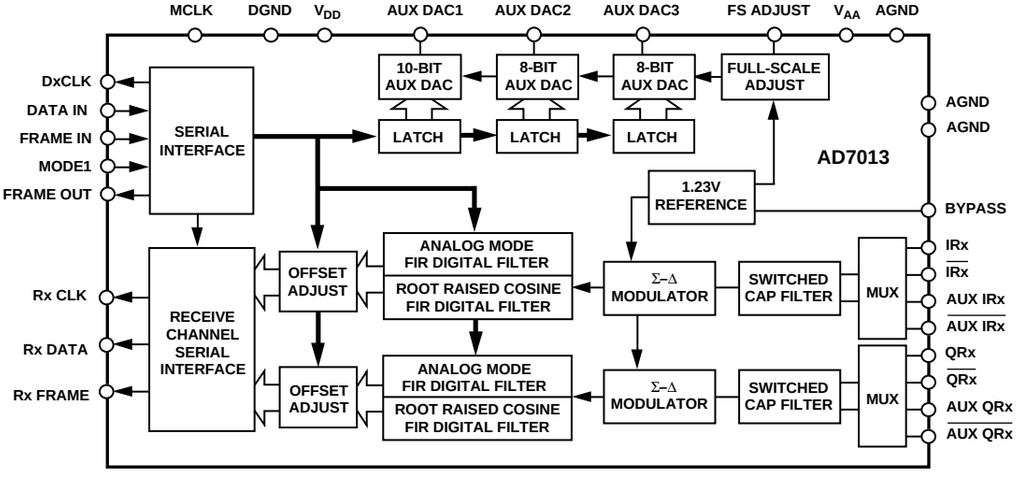
The AD7013 is a complete low power, CMOS, TIA IS-54 baseband receive port with single +5 V power supply. The part is designed to perform the baseband conversion of I and Q waveforms in accordance with the American (TIA IS-54) Digital Cellular Telephone system.

The receive path consists of two high performance sigma-delta ADCs, each followed by a FIR digital filter. A primary and auxiliary set of IQ differential analog inputs are provided, where either can be selected as inputs to the sigma-delta ADCs. Also, a choice of two frequency responses are available for the receive FIR filters; a Root-Raised-Cosine filter for digital mode or a brick wall response for analog mode. Differential analog inputs are provided for both I and Q channels. On-chip calibration logic is also provided to remove either on-chip offsets or remove system offsets. A 16-bit serial interface is provided, interfacing easily to most DSPs. The receive path also provides a means to vary the sampling instant, giving a resolution to 1/32 of a symbol interval.

The auxiliary section provides two 8-bit DACs and one 10-bit DAC for functions such as automatic gain control (AGC), automatic frequency control (AFC) and power amplifier control.

As it is a necessity for all digital mobile systems to use the lowest possible power, the device has receive and auxiliary power down options. The AD7013 is housed in a space efficient 28-pin SSOP (Shrink Small Outline Package).

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD7013—SPECIFICATIONS[1] ($V_{AA} = V_{DD} = +5$ V ± 10%; AGND = DGND = 0 V; f_{MCLK} = 6.2208 MHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	AD7013A	Units	Test Conditions/Comments
RECEIVE SECTION			
ADC SPECIFICATION			
Number of Input Channels	4		(IRx–$\overline{\text{IRx}}$) and (QRx–$\overline{\text{QRx}}$); CR12 = 0 (AUX IRx–$\overline{\text{AUX IRx}}$) and (AUX QRx–$\overline{\text{AUX QRx}}$); CR12 = 1
Number of ADC Channels	2		
Resolution	15	Bits	
ADC Signal Range	2.6	Volts p-p	Measured Using an Input Sine Wave of 3 kHz
Differential Signal Range	V_{BIAS} ± 0.65	Volts	For Both Noninverting and Inverting Analog Inputs
Single-Ended Signal Range	V_{BIAS} ± 1.3	Volts	For Noninverting Analog Inputs; Inverting Analog Inputs = V_{BIAS}
V_{BIAS}	0.65 to (V_{AA}–0.65)	Volts min/max	Differential
	1.3 to (V_{AA}–1.3)	Volts min/max	Single-Ended
Input Range Accuracy	±7.5	%	
Accuracy			
Bias Offset Error	±7.5	mV	Autocalibration; V_{BIAS} = min/max
	±55	mV	User Calibration; I & Q Offset Adjust Registers Equal to Zero
Dynamic Specifications			
CMRR	–40	dB typ	Measured Using an Input Sine Wave of 3 kHz with Both Noninverting and Inverting Inputs Tied Together
Dynamic Range	70	dB typ	Digital Mode Filter; CR11 = 0
	65	dB typ	Analog Mode Filter; CR11 = 1
SNR[2]	65	dB min	Digital Mode Filter; CR11 = 0
	68	dB typ	
	60	dB min	Analog Mode Filter; CR11 = 1
	63	dB typ	
Input Sampling Rate	1.5552/1.28	MHz	MCLK = 6.2208 MHz/5.12 MHz; MCLK/4
Output Word Rate	97.2/80	kHz	MCLK = 6.2208 MHz/5.12 MHz; 4 × Sampling of the Symbol Rate, MCLK/64
	48.6/40	kHz	MCLK = 6.2208 MHz/5.12 MHz; 2 × Sampling of the Symbol Rate, MCLK/128
RECEIVE DIGITAL FILTERS			
Digital Mode			MCLK = 6.2208 MHz
Root-Raised-Cosine	α = 0.35		
Settling Time	329.2	µs	
Absolute Group Delay	164.6	µs	
Frequency Response			
0–7.8975 kHz	±0.05	dB max	
11.9 kHz	–3.0	dB	
16.4025 kHz	–19	dB	
> 30 kHz	–66	dB max	
Analog Mode			MCLK = 5.12 MHz
Brick Wall Filter			
Settling Time	400	µs	
Absolute Group Delay	200	µs	
Frequency Response			
0–8 kHz	0 to –0.5	dB max	
11.4 kHz	–3.0	dB	
15 kHz	–24	dB	
>17 kHz	–68	dB max	
TIA IS-54 RECEIVE SPECIFICATIONS			
Error Vector Magnitude[3]	2	% rms typ	Measured Using a Full-Scale Input
Error Offset Magnitude[3]	1	% rms typ	

Parameter	AD7013A			Units	Test Conditions/Comments
AUXILIARY SECTION					
	AUX DAC1	AUX DAC2	AUX DAC3		
Resolution	10	8	8	Bits	
DC Accuracy					
Integral	±3	±1	±1	LSBs max	
Differential	–1.5/+4	±1	±1	LSBs max	AUX DAC2 & AUX DAC3 Guaranteed Monotonic
Zero Code Leakage	±500	±500	±500	nA max	
Gain Error	±7.5	±7.5	±7.5	% max	
Output Full-Scale Current	566	280	280	µA	R_{SET} = 18 kΩ
Output Impedance[4]		2		MΩ typ	
Output Voltage Compliance		2.6		Volts max	
Coding		Binary			
Power Down Option		Yes			
REFERENCE SPECIFICATIONS					
V_{REF}		1.23		Volts typ	
Reference Accuracy		±5		% max	
Reference Impedance		20		kΩ typ	
LOGIC INPUTS					
V_{INH}, Input High Voltage		V_{DD}–0.9		V min	
V_{INL}, Input Low Voltage		0.9		V max	
I_{INH}, Input Current		10		µA max	
C_{IN}, Input Capacitance		10		pF max	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage		V_{DD}–0.4		V min	$\|I_{OUT}\| \le 40$ µA
V_{OL}, Output Low Voltage		0.4		V max	$\|I_{OUT}\| \le 1.6$ mA
POWER SUPPLIES					
V_{DD}		4.5/5.5		V_{MIN}/V_{MAX}	
I_{DD}[5]					
All Sections Active		10.5		mA max	CR14 = CR15 = CR16 = CR17 = 1
		9		mA typ	MCLK = 6.2208 MHz; 80 pF Load on DxCLK
ADCs Active Only		8.6		mA max	CR14 = 1; CR15 = CR16 = CR17 = 0 MCLK = 6.2208 MHz; 80 pF Load on DxCLK
AUX DACs Active Only		2.2		mA max	CR14 = 0; CR15 = CR16 = CR17 = 1; MCLK Inactive, MCLK = 0 V
10-Bit AUX DAC Active		1.6		mA max	CR14 = CR15 = CR16 = 0; CR17 = 1; MCLK Inactive, MCLK = 0 V
All Sections Powered Down[6]		2		mA max	CR14 = CR15 = CR16 = CR17 = 0 MCLK = 6.2208 MHz; 80 pF Load on DxCLK
		30		µA typ	MCLK =100 kHz; 80 pF Load on DxCLK
		10		µA max	MCLK Inactive, MCLK = 0 V

NOTES
[1]Operating temperature ranges as follows: A version: –40°C to +85°C.
[2]SNR calculation includes noise and distortion components.
[3]See Terminology.
[4]Sampled tested only.
[5]Measured while the digital inputs are static and equal to 0 V or V_{DD}.
[6]With all sections powered down, I_{DD} is proportional to the capacitive load on DxCLK. For example, I_{DD} is typically 1.7 mA with 80 pF load and 600 µA with 10 pF load.
Specifications subject to change without notice.

TERMINOLOGY

Sampling Rate
This is the rate at which the modulators on the receive channels sample the analog input.

Output Rate
This is the rate at which data words are made available at the RxDATA pin.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the DAC or ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the DAC or ADC.

Dynamic Range
Dynamic Range is the ratio of the maximum rms input signal to the rms noise of the converter, expressed logarithmically, in decibels (dB = 20 $\log_{10}$ [ratio]).

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the receive channel. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for a sine wave is given by:

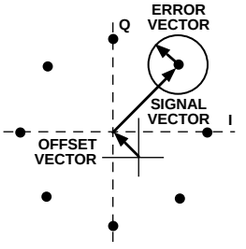
$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Settling Time
This is the digital filter settling time in the AD7013 receive section.

Bias Offset Error
This is the amount of offset in the receive channel ADC when the differential inputs are tied together.

Receive Error Vector Magnitude
This is a measure of the rms signal error vector introduced by the receive Root-Raised Cosine digital filter. This is measured by applying an ideal transmit signal (i.e., an ideal π/4 DQPSK modulator and an ideal transmit Root-Raised Cosine filter) to the receive channel and measuring the resulting rms error vector.

Offset Vector Magnitude
This is a measure of the offset vector introduced by the AD7013 as illustrated in the figure below. The offset vector is calculated so as to minimize the rms error vector for each of the constellation points.



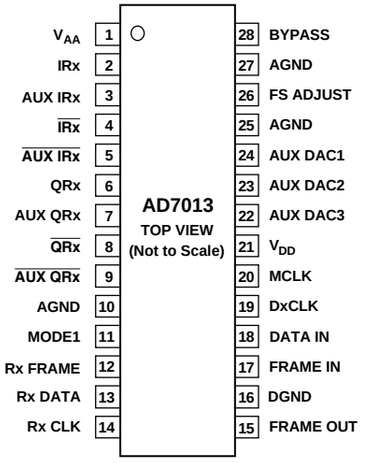
ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{AA}, V_{DD} to GND ..... –0.3 V to +7 V
AGND to DGND ..... –0.3 V to +0.3 V
Digital I/O Voltage to DGND ..... –0.3 V to V_{DD} +0.3 V
Analog I/O Voltage to AGND ..... –0.3 V to V_{DD} +0.3 V
Operating Temperature Range
  Industrial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Junction Temperature ..... +150°C
SSOP θ_{JA} Thermal Impedance ..... +122°C/W
Lead Temperature Soldering
  Vapor Phase (60 sec) ..... +215°C
  Infrared (15 sec) ..... +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7013ARS	–40°C to +85°C	RS-28

*RS = SSOP.

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

SSOP Pin Number	Mnemonic	Function
POWER SUPPLY		
1	V_{AA}	Positive Power Supply for Analog section. A 0.1 µF decoupling capacitor should be connected between this pin and AGND.
21	V_{DD}	Positive Power Supply for Digital section. A 0.1 µF decoupling capacitor should be connected between this pin and DGND. Both V_{AA} and V_{DD} should be externally tied together.
10, 25, 27	AGND	Analog Ground.
16	DGND	Digital Ground. Both AGND and DGND should be externally tied together.
ANALOG SIGNAL AND REFERENCE		
28	BYPASS	Reference Decoupling Output. A 10 nF decoupling capacitor should be connected between this pin and AGND.
2, 4	IRx, $\overline{\text{IRx}}$	Differential Analog Inputs for the I receive channel. These are the primary receive analog inputs and are selected by setting CR12 to a zero in the command register.
6, 8	QRx, $\overline{\text{QRx}}$	Differential Analog Inputs for the Q receive channel. These are the primary receive analog inputs and are selected by setting CR12 to a zero in the command register.
3, 5	AUX IRx, $\overline{\text{AUX IRx}}$	Auxiliary Differential Analog Inputs for the I receive channel. The Auxiliary inputs are selected by setting CR12 to a one in the command register.
7, 9	AUX QRx, $\overline{\text{AUX QRx}}$	Auxiliary Differential Analog Inputs for the Q receive channel. The Auxiliary inputs are selected by setting CR12 to a one in the command register.
24	AUX DAC1	Analog output from the 10-bit auxiliary DAC.
3, 22	AUX DAC2, AUX DAC3	Analog outputs from the 8-bit auxiliary DACs.
26	FS ADJUST	An external resistor is connected from this pin to ground to determine the full-scale current for AUX DAC1, AUX DAC2, and AUX DAC3.
SERIAL INTERFACE AND CONTROL		
20	MCLK	Master Clock, Digital Input. When operating in IS-54 Digital mode this pin should be driven by a 6.2208 MHz CMOS compatible clock source and 5.12 MHz clock source for Analog Mode.
19	DxCLK	Transmit Clock, Digital Output. This is a continuous clock equal to MCLK/2 which can be used to clock the serial port of a DSP.
17	FRAME IN	Digital Input. This is used to frame the clocking in of 16-bit words for the control registers serial interface.
18	DATA IN	Digital Input. Transmit Serial Data, digital input. This pin is used to clock in data for the serial interface on the rising edge of DxCLK.
15	FRAME OUT	Digital Output. This output represents a buffered version of FRAME IN and is controlled by the MODE1 pin. This pin can be used to daisy chain the FRAME IN signal.
11	MODE1	Digital Input. This pin determines the state of FRAME OUT. When MODE1 is high, FRAME IN is buffered and made available on FRAME OUT. When MODE1 is low, FRAME OUT is in 3-STATE.
RECEIVE INTERFACE AND CONTROL		
14	RxCLK	Output Clock for the receive section interface.
12	RxFRAME	Synchronization output for framing I and Q data at the receive interface.
13	RxDATA	Receive Data, digital output. I and Q data are available at this pin via a 16-bit serial interface. Data is valid on the falling edge of RxCLK. I and Q data are clocked out as two 16-bits words, with the I word being clocked first. The last bit in each 16-bit word is a I/$\overline{\text{Q}}$ flag bit, indicating whether that word is an I word or a Q word.

CONTROL SERIAL INTERFACE TIMING[1]

(V_{AA} = +5 V ± 10%; V_{DD} = +5 V ± 10%; AGND = DGND = 0 V, f_{MCLK} = 6.2208 MHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_A = –40°C to +85°C	Units	Description
t_1	160	ns min	MCLK Cycle Time
t_2	65	ns min	MCLK High Time
t_3	65	ns min	MCLK Low Time
t_4	20	ns min	MCLK Rising Edge to DxCLK Rising Edge Propagation Delay
	60	ns max	
t_5	$2t_1$	ns	DxCLK Cycle Time
t_6	t_1–20	ns min	DxCLK Minimum High Time
t_7	t_1–20	ns min	DxCLK Minimum Low Time
t_8	25	ns min	DxCLK Rising Edge to FRAME IN Setup Time
t_9	10	ns min	DxCLK Rising Edge to FRAME IN Hold Time
t_{10}	$16t_5$	ns min	FRAME IN Cycle Time
t_{11}	25	ns min	DxCLK Rising Edge to DATA IN Setup Time
t_{12}	10	ns min	DxCLK Rising Edge to DATA IN Hold Time
t_{13}	0	ns min	FRAME IN Rising Edge to FRAME OUT Rising Edge Propagation Delay
	25	ns max	
t_{14}	25	ns max	MODE1 Low to FRAME OUT 3-STATE
t_{15}	25	ns max	MODE1 High to FRAME OUT Active

NOTE
[1]t_{14} is derived from the measured time taken by the FRAME OUT pin to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 80 pF capacitor. This means that the time quoted in the Timing Characteristics is the

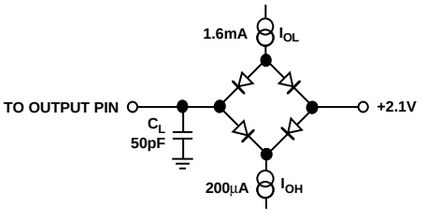


Figure 1. Load Circuit for Digital Outputs

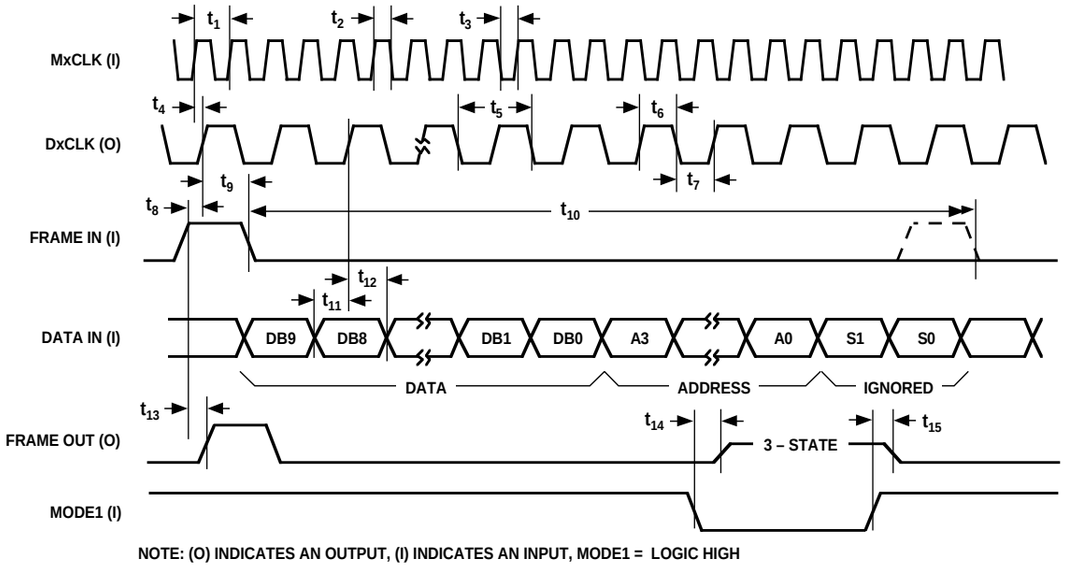


Figure 2. 16-Bit Serial Interface for Writing to the AD7013 Internal Registers

RECEIVE SECTION TIMING

(V_{AA} = +5 V ± 10%; V_{DD} = +5 V ± 10%; AGND = DGND = 0 V, f_{MCLK} = 6.2208 MHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_A = –40°C to +85°C	Units	Description
t_{16}			Power-Up Receive to RxCLK
	$10240t_1$	ns max	CR13 = 0, Rx Offset Autocalibration On
	$6144t_1$	ns max	CR13 = 1, Rx Offset Autocalibration Off
t_{17}	30	ns min	Propagation Delay from MCLK Rising Edge to RxCLK Rising Edge
	85	ns max	
t_{18}	$2t_1$	ns	RxCLK Cycle Time; CR10 = 1; 4× Sampling of the Symbol Rate
t_{19}	t_1–20	ns min	RxCLK High Pulse Width; CR10 = 1
t_{20}	t_1–20	ns min	RxCLK Low Pulse Width; CR10 = 1
t_{21}	–10	ns min	RxCLK Rising Edge to RxFRAME Rising Edge
	10	ns max	
t_{22}	$32t_1$	ns	RxFRAME Cycle Time; CR10 = 1
t_{23}	$2t_1$	ns	RxFRAME High Pulse Width; CR10 = 1
t_{24}	–10	ns min	RxDATA Valid After RxCLK Rising Edge
	10	ns max	
t_{25}	$10t_1$	ns min	DxCLK Rising Edge to Last Falling Edge RxCLK
	$64t_1$	ns max	

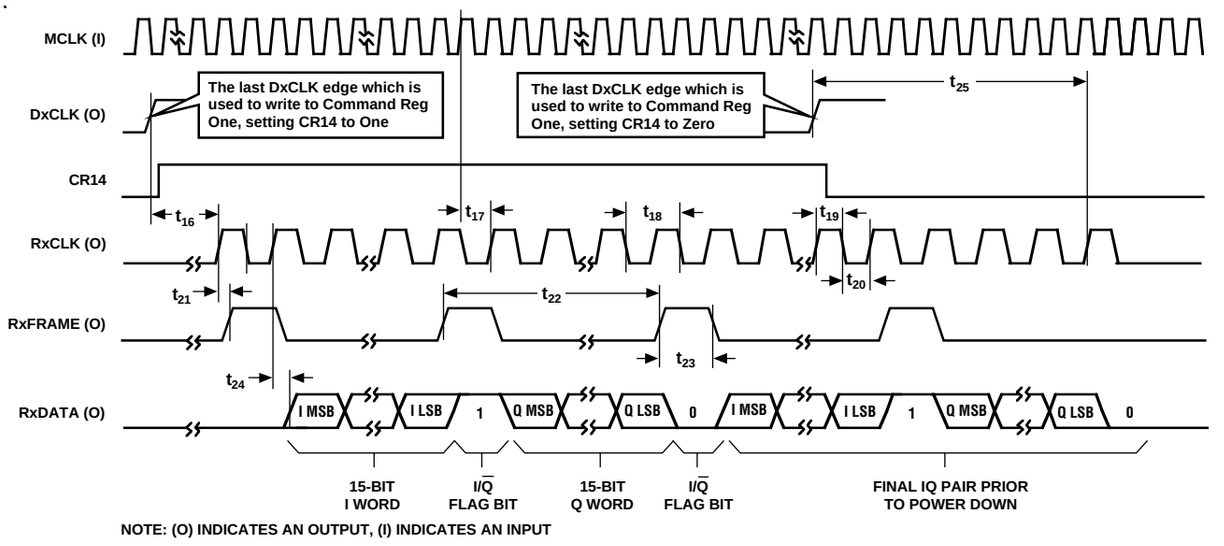


Figure 3. Receive Serial Interface Timing with 4× Sampling of the Symbol Rate (CR10 = 1)

RECEIVE SECTION TIMING

(V_{AA} = +5 V ± 10%; V_{DD} = +5 V ± 10%; AGND = DGND = 0 V, f_{MCLK} = 6.2208 MHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_A = −40°C to +85°C	Units	Description
t_{26}			Power up Receive to RxCLK
	$10240t_1$	ns max	CR13 = 0; Rx Offset Autocalibration On
	$6144t_1$	ns max	CR13 = 1; Rx Offset autocalibration Off
t_{27}	30	ns min	Propagation Delay from MCLK Rising Edge to RxCLK Rising Edge
	85	ns max	
t_{28}	$4t_1$	ns	RxCLK Cycle Time; CR10 = 0; 2x Sampling of the Symbol Rate
t_{29}	$2t_1$–20	ns min	RxCLK High Pulse Width; CR10 = 0
t_{30}	$2t_1$–20	ns min	RxCLK Low Pulse Width; CR10 = 0
t_{31}	–10	ns min	RxCLK Rising Edge to RxFRAME Rising Edge
	+10	ns max	RxCLK to RxFRAME Propagation Delay
t_{32}	$64t_1$	ns	RxFRAME Cycle Time; CR10 = 0
t_{33}	$4t_1$	ns	RxFRAME High Pulse Width; CR10 = 0
t_{34}	–10	ns min	Propagation Delay from RxCLK Rising Edge to RxDATA Valid
	+10	ns max	
t_{35}	$12t_1$	ns min	DxCLK Rising Edge to Last Falling Edge of RxCLK
	$128t_1$	ns max	
t_{36}	$2t_1$ + 20	ns max	3-State to Receive Channel Valid
t_{37}	$2t_1$ + 20	ns max	Receive Channel to 3-State Relinquish Time

[1]t_{37} is derived from the measured time taken by the receive channel outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 80 pF capacitor. This means that the time quoted in the Timing Characteristics is the true relinquish time of the part and as such is independent of external loading capacitance.

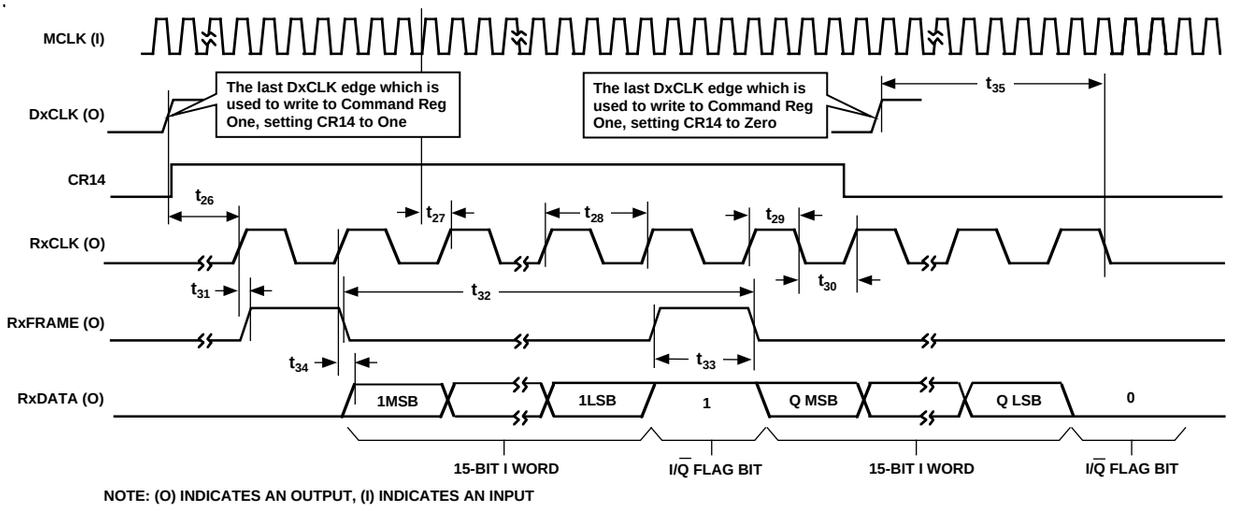


Figure 4. Receive Serial Interface Timing with 2× Sampling of the Symbol Rate (CR10 = 0)

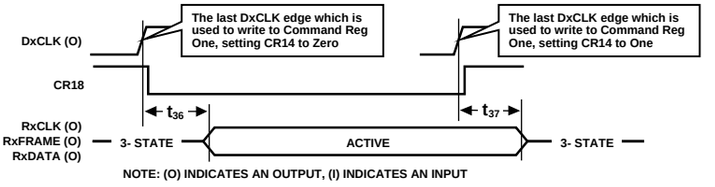


Figure 5. Receive Serial Interface 3-State Timing

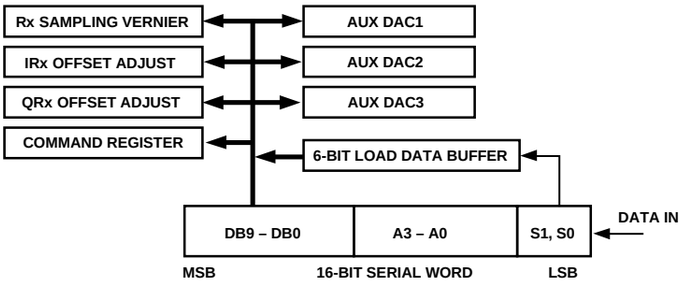


Figure 6. AD7013 Registers

Table I. Description and Address Map for AD7013 Internal Registers

Register Name	Address A3	A2	A1	A0	Register Size	Reset State	Description
COMMAND	0	0	1	0	9 Bits	All Zeros	The COMMAND register is used to select various operating modes of the AD7013. A detailed description of the COMMAND register is given in Table II.
VERNIER	0	1	0	0	4 Bits	All Zeros	The VERNIER register allows additional group delay to be introduced into the I and Q ADCs. This provides a means to vary the ADC sampling instant.
IRx OFFSET	0	1	0	1	10 Bits	All Zeros	The contents of the IRx OFFSET register are substracted from the I channel ADC word. When autocalibration is selected, this register is automatically loaded by the AD7013 at the beginning of a normal operation. When user calibration is selected, this register can be externally loaded with a twos complement offset 10-bit word to be subtracted from subsequent ADC samples.
QRx OFFSET	0	1	1	0	10 Bits	All Zeros	The contents of the QRx OFFSET register are substracted from the Q channel ADC word. When auto calibration is selected, this register is automatically loaded by the AD7013 at the beginning of a normal operation. When user calibration is selected this register can be externally loaded with a twos complement offset 10-bit word to be subtracted from subsequent ADC samples.
AUX DAC1	0	1	1	1	10 Bits	All Zeros	The 10-bit auxiliary DAC current output is determined by this register. The output current is equal to $\{AUX\ DAC1_{FULL\ SCALE} * N/2^{10}\}$ where N is the 10-bit word contained in the AUX DAC1 register and $AUX\ DAC1_{FULL\ SCALE}$ is determined by the value of R_{SET} connected between FSADJUST and AGND.
AUX DAC2	1	0	0	0	8 Bits	All Zeros	The 8-bit auxiliary DAC current output is determined by this register. The output current is equal to $\{AUX\ DAC1_{FULL\ SCALE} * N/2^{8}\}$ where N is the 8-bit word contained in the AUX DAC2 register and $AUX\ DAC2_{FULL\ SCALE}$ is determined by the value of RSET connected between FS ADJUST and AGND.
AUX DAC3	1	0	0	1	8 Bits	All Zeros	The 8-bit auxiliary DAC current output is determined by this register. The output current is equal to $\{AUX\ DAC3_{FULL\ SCALE} * N/2^{8}\}$ where N is the 8-bit word contained in the AUX DAC3 register and $AUX\ DAC3_{FULL\ SCALE}$ is determined by the value of R_{SET} connected between FS ADJUST and AGND.
RESET	0	0	0	1	N/A	N/A	When this address in selected, all of the internal registers are initialized to their reset state.
6-Bit LOAD	0	0	1	1	N/A	N/A	When this address is used, a special loading sequence, as shown in Table IV, is used to write to any of the internal registers.
N/A	0	0	0	0	N/A	N/A	No Action.
N/A	1	1	1	1	N/A	N/A	No Action.

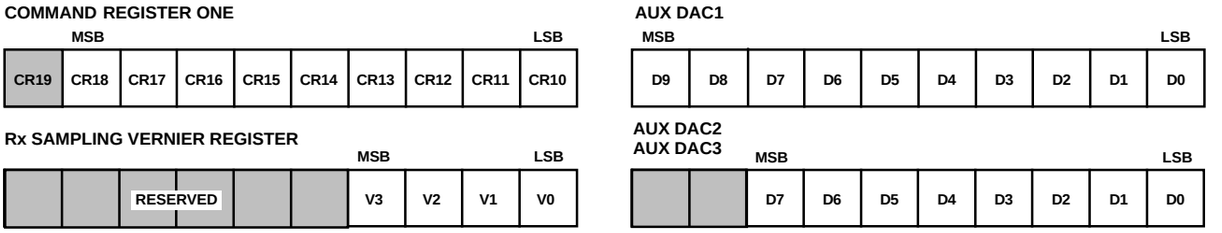


Figure 7. Internal AD7013 Registers

Table II. Command Register One

CR10	= 0	Low ADC sample rate. The sample rate of the receive ADCs are equal to 2× the symbol rate or equal to MCLK/128.
	= 1	High ADC sample rate. The sample rate of the ADCs are equal to 4× the symbol rate or equal to MCLK/64.
CR11	= 0	RRC Receive FIR filter. This selects the root-raised consine filter response for the receive sigma-delta ADCs. This is used to match the transmit RRC filter as required by the IS-54 standard. The frequency response is shown in Figure 16.
	= 1	Analog Mode FIR filter. This selects a filter response which has a sharper roll-off than the RRC FIR filter and the frequency response has also been scaled to operate at a master clock frequency of 5.12 MHz. This allows the sampling rate of the receive ADCs to be a multiple of 10 kHz as required for analog cellular. The frequency response is shown in Figure 17.
CR12	= 0	Primary ADC inputs. This selects IRx and $\overline{\text{IRx}}$ as the I channel inputs and QRx and $\overline{\text{QRx}}$ as the Q channel inputs.
	= 1	Auxiliary ADC inputs. This selects AUX IRx and $\overline{\text{AUX IRx}}$ as the I channel inputs and AUX QRx and $\overline{\text{AUX QRx}}$ as the Q channel inputs.
CR13	= 0	Auto ADC offset calibration. If auto calibration is selected, then an offset word for both ADCs is calculated each time the receive ADCs are brought out of sleep mode. This allows ADC offsets within the AD7013 to be automatically calibrated out.
	= 1	User ADC offset calibration. When user calibration is selected, then contents of the offset registers are not updated by the AD7013 when brought out of sleep mode. This allows the user to load the offset register externally thereby allowing the AD7013 to also calibrate out external offsets.
CR14	= 0	Receive ADC sleep mode. This enters the I and Q ADCs into a low power sleep mode after outputting the current IQ sample.
	= 1	Receive ADC active mode. This activates the receive ADCs for normal operation.
CR15	= 0	8-Bit AUX DAC3 sleep mode. This enters the 8-bit auxiliary DAC into a low power sleep mode.
	= 1	8-Bit AUX DAC3 active mode. This activates the 8-bit auxiliary DAC for normal operation.
CR16	= 0	8-Bit AUX DAC2 sleep mode. This enters the 8-bit auxiliary DAC into a low power sleep mode
	= 1	8-Bit AUX DAC2 active mode. This activates the 8-bit auxiliary DAC for normal operation.
CR17	= 0	10-Bit AUX DAC1 sleep mode. This enters the 10-bit auxiliary DAC into a low power sleep mode.
	= 1	10-Bit AUX DAC1 active mode. This activates the 10-bit auxiliary DAC for normal operation.
CR18	= 0	3-State Enable. This enables the 3-state buffers on the receive serial interface.
	= 1	3-State Disable. This disables the 3-state buffers on the receive serial interface, entering the serial interface into 3-state.
CR19	= X	No Action.

RECEIVE SECTION

The receive section consists of I and Q receive channels, each comprising of a simple switched-capacitor filter followed by a 15-bit sigma-delta ADC. The data is available on a 16-bit serial interface, interfacing easily to most DSPs. On-board digital filters, which form part of the sigma-delta ADCs, also perform system level filtering. A choice of two digital filter responses are available, optimized for either π/4 DQPSK digital mode or the existing analog cellular system. For digital mode, Root-Raised Cosine digital filters can be selected; whereas for analog mode, digital filters with a –3 dB point of 11.4 kHz can be selected. Their amplitude and phase response characteristics provide excellent adjacent channel rejection. A means is also provided to calibrate either on-chip or receive path offsets in both the I and Q channels. The receive section is also provided with a low power sleep mode, drawing only minimal current between receive bursts.

Switched Capacitor Input

The receive section analog front-end is sampled at MCLK/4 by a switched-capacitor filter. The filter has a zero at MCLK/8 as shown in Figure 8a. The receive channel also contains a digital low-pass filter (further details are contained in the following section) which operates at a clock frequency of MCLK/8. Due to the sampling nature of the digital filter, the pass band is repeated about the operating clock frequency (MCLK/8) and at multiples of the clock frequency (Figure 8b). Because the first null of the switched-capacitor filter coincides with the first image of the digital filter, this image is attenuated by an additional 30 dBs (Figure 8c) further simplifying the external antialiasing requirements. A simple R-C Network can be used to attenuate the digital filter image at MCLK/8 as shown in Figure 9.

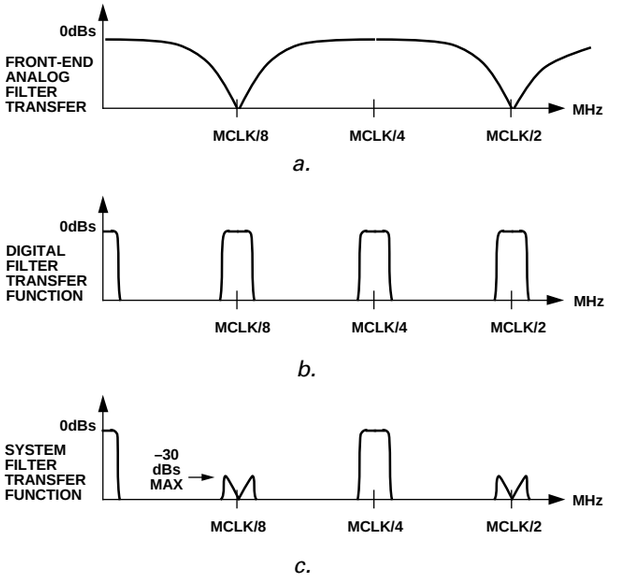


Figure 8. Switched Capacitor and Digital Filter Transfer Functions

Receive Channel Differential Inputs

The receive channel uses differential inputs to interface more easily to IQ demodulators and also to provide common-mode noise rejection. However, if required the receive channel inputs can also be configured for single ended operation. The primary and auxiliary channels have similar performance and either can be used for differential operation or single-ended operation. The CR12 control bit determines whether the primary or auxiliary inputs are connected to the differential inputs of the sigma-delta modulator.

Figure 9 illustrates an antialiasing filter comprised of a single pole RC network with a –3 dB frequency of 159 kHz. The low-pass filter provides sufficient rejection at images of the FIR digital filter illustrated in Figure 10c.

For single ended operation, the inverting input should be connected to a bias voltage and the noninverting input should swing ±1.3 V around this bias voltage in order to exercise the entire ADC range. In applications where the full ±1.3 V range is not required, the on-chip 1.23 V reference can be used to provide the bias voltage. For instance as in Figure 10, an OP295 rail-to-rail low power op amp is used to buffer the BYPASS pin in order to generate a 1.23 V_{BIAS}. The V_{BIAS} is connected to the inverting input thereby setting the single-ended input range equal to 0 V to 2.46 V. Also with the addition of an attenuator circuit the input range can be expanded to 0 V to 4.92 V as shown on the second ADC channel. If the inverting input is tied to AGND, then only half the ADC range is available.

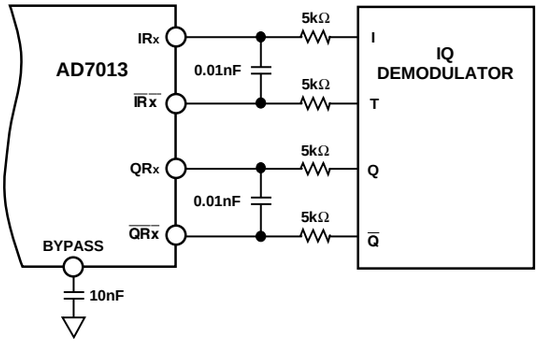


Figure 9. External RC Network for Differential Signals

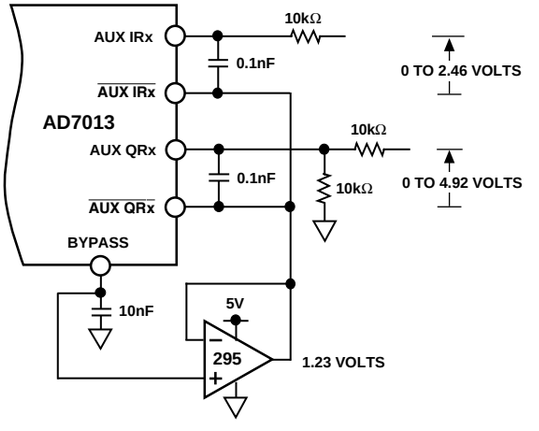


Figure 10. External RC Network for Single-Ended Signals

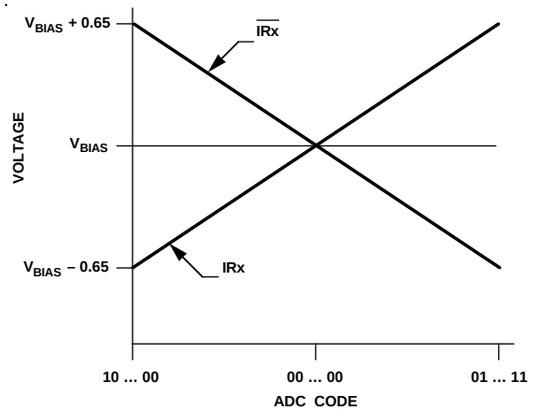


Figure 11. ADC Transfer Function for Differential Operation

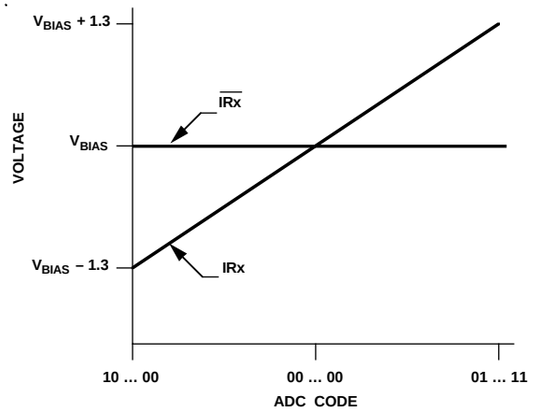


Figure 12. ADC Transfer Function for Single-Ended Operation

SIGMA-DELTA ADC

The AD7013 receive channels employ a sigma-delta conversion technique, which provides a high resolution 15-bit output for both I and Q channels with system filtering being implemented on-chip.

The output of the switched-capacitor filter is continuously sampled at MCLK/8, by a charge-balanced modulator, and is converted into a digital pulse train whose duty cycle contains the digital information. Due to the high oversampling rate which spreads the quantization noise from 0 to $f_S/2$, the noise energy which is contained in the band of interest is reduced (Figure 13a). To reduce the quantization noise still further, a high order modulator is employed to shape the noise spectrum, so that most of the noise energy is shifted out of the band of interest (Figure 13b).

The digital filter that follows the modulator removes the large out of band quantization noise (Figure 13c), while converting the digital pulse train into parallel 15-bit wide binary data. The 15-bit I and Q data plus an I/Q flag bit is made available, via a serial interface, as a 16-bit word, MSB first.

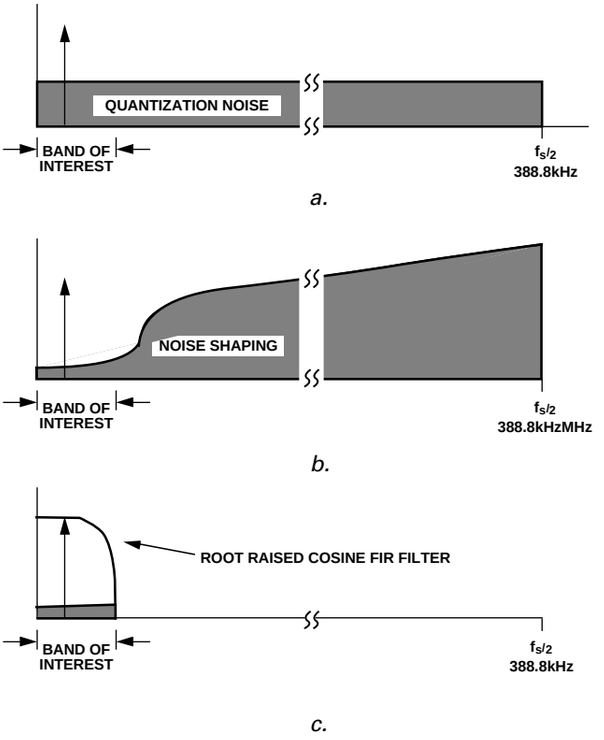


Figure 13. a. Effect of High Oversampling Ratio.
b. Use of Noise Shaping to Further Improve SNR.
c. Use of Digital Filtering to Remove the Out of Band Quantization Noise

Digital Filter

The digital filters used in the AD7013 receive section carry out two important functions. First, they remove the out of band quantization noise which is shaped by the analog modulator. Second, they are also designed to perform system level filtering, providing the Root-Raised Cosine filter as required for TIA IS-54.

Since digital filtering occurs after the A/D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this. Also, the digital filter combines low passband ripple with a steep roll off, while also maintaining a linear phase response. This is very difficult to achieve with analog filters.

Filter Characteristics

The digital filter is a 256-tap FIR filter, clocked at 1/8 the master clock frequency. A choice of two frequency responses are available: a Root-Raised Cosine response (CR11 = 0) and a brick wall response at 11.4 kHz (CR11 = 1) for analog mode. Figure 16 and Figure 17 illustrate the respective frequency responses for both digital mode and analog mode while Figure 18 compares the low frequency response of the digital filters.

Due to the low-pass nature of the receive filters there is a settling time associated with step input functions. Output data will not be meaningful until all the digital filter taps have been loaded with data samples taken after the step change. Hence, the AD7013 digital filters have a settling time of $256 \times 8t_1$ (i.e., 329.2 µs when MCLK = 6.2208 MHz and 400 µs when MCLK = 5.12 MHz).

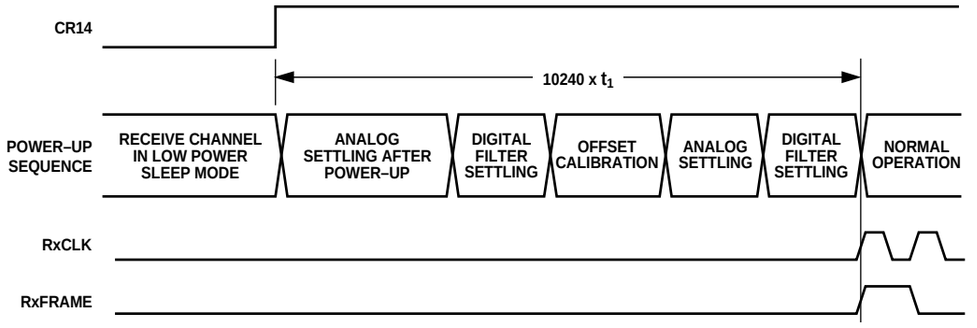


Figure 14. Autocalibration Routine After Exiting Low Power Sleep Mode

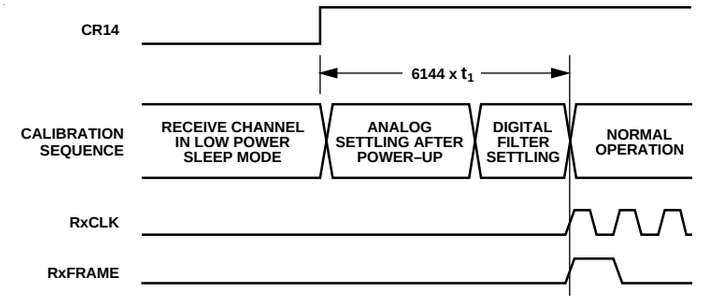


Figure 15. User-Calibration Routine After Exiting Low Power Sleep Mode

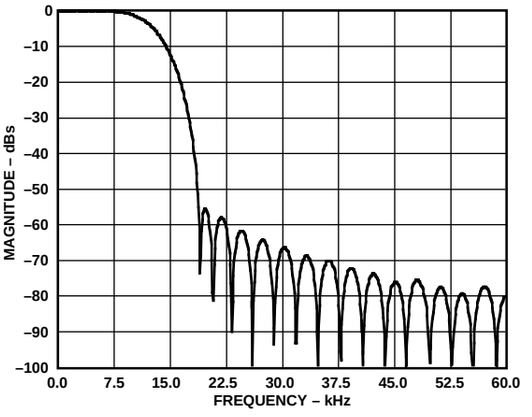


Figure 16. Receive Root Raised Cosine FIR Filter; CR11 = 0, MCLK = 6.2208 MHz

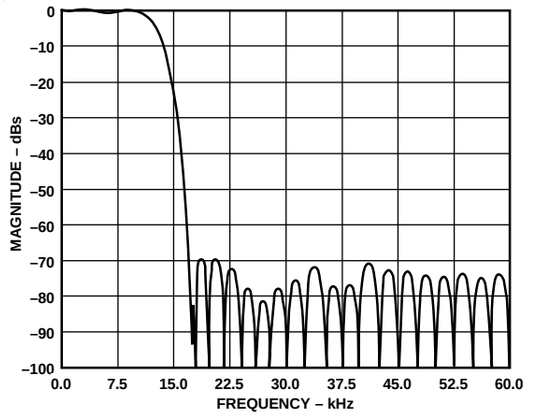


Figure 17. Receive Analog Mode FIR Filter; CR11 = 1, MCLK = 5.12 MHz

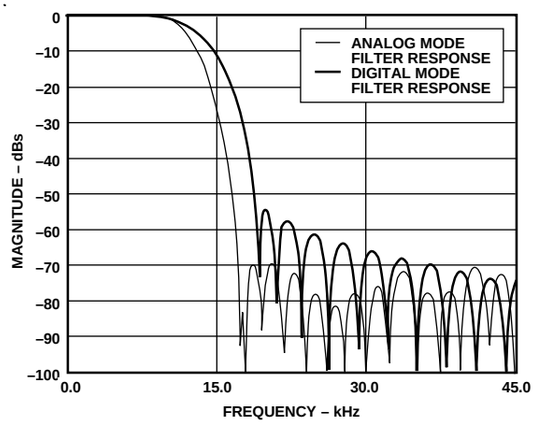


Figure 18. Comparision of the Two Frequency Responses Where Digital Mode was Clocked at 6.2208 MHz and Analog Mode was Clocked at 5.12 MHz

Receive Offset Calibration

Included in the digital filter is a means by which receive signal offsets may be calibrated out. Each channel of the digital low-pass filter section has an offset register. The offset register can be made to contain a value representing the dc offset of the preceding analog circuitry. In normal operation, the value stored in the offset register is subtracted from the filter output data before the data appears on the serial output pin. By so doing, dc offsets in the I and Q channels get calibrated out. Autocalibration or user calibration can be selected. Autocalibration will remove internal offsets only while user calibration allows the user to write to the offset register in order to also remove external offsets.

The offset registers have enough resolution to hold the value of any dc offset between ±153 mV (1/8th of the input range). The 10-bit offset register represents a twos-complement value which is mapped to a 15-bit twos-complement word as shown in Figure 19. The contents of the offset registers are subtracted from their respective ADC samples.

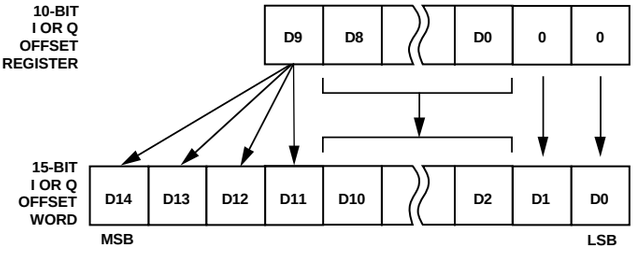


Figure 19. Position of the 10-Bit Offset Word Within the 15-Bit ADC Word

Receive Offset Adjust: Auto-Calibration (CR13 = 0)

If receive autocalibration has been selected (CR13 = 0), then the AD7013 will initiate an autocalibration routine each time the receive path is brought out of the low power sleep mode (CR14 = 0). The AD7013 internally disconnects the differential inputs from the input pins and shorts the differential inputs to measure the resulting ADC offset. This is then averaged 16 times to reduce ADC noise, and the averaged result is then placed in the offset register. The input to the ADC is then switched back for normal operation, and after allowing for both analog settling and digital filter settling, the first IQ sample pair is output (Figure 14). Autocalibration will only remove on-chip offsets.

Receive Offset Adjust: User Calibration (CR13 = 1)

When user calibration has been selected, the receive offset register can be written to, allowing offsets in the IF/RF demodulation circuitry to be also calibrated out. However, the user is now responsible for calibrating out receive offsets belonging to the AD7013. When the receive path enters the low power mode (CR14 = 0), the offset registers remain valid. After powering up, the first IQ sample pair is output once time has elapsed for both the analog circuitry to settle and also for the output of the digital filter to settle as shown in Figure 15.

ADC Sampling Vernier

Also included in the digital filter is the means to vary the sampling instant, as Figure 20 illustrates. The absolute group delay can be varied from a minimum of four symbols to a maximum of four and a half symbols allowing the user to define the sampling instant to a resolution 1/32 of the symbol rate. The vernier can be used to seek the optimum sampling instant for minimum Inter-Symbol-Interference (ISI).

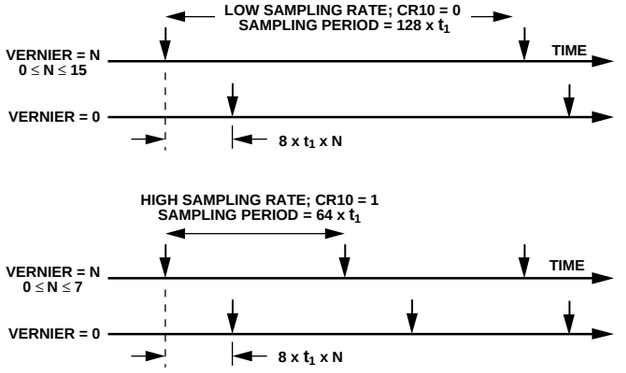


Figure 20. I and Q ADC Sampling Vernier for 2× the Symbol Rate and 4× the Symbol Rate

A 4-bit vernier register is used to set the sampling instant for both the I and Q receive ADCs. When the vernier register is programmed with zero the ADCs will have a minimum group delay of approximately 165 µs. Nonzero values in the vernier register will add additional group delay thereby moving the sampling instant for both ADCs. After programming the sampling vernier it takes eight symbols (≈330 µs) for the digital filter to settle. When the ADC is operating at the high rate, vernier values from 8 to 15 yield similar sampling instants as vernier values from 0 to 7, but delayed by an additional 1/4 of a symbol period.

Table III. Loading Sequence for the 16-Bit Interface

DB9–DB0	A3–A0	S1, S0	Action
D9–D0	Destination Address	Ignored	Destination Reg←D9–D0

Table IV. Loading Sequence for the 6-Bit Interface

DB9–DB0	A3–A0	S1, S0	Action
Ignored	0011	D9, D8	D9←S1 and D8←S0
Ignored	Destination Address	D7, D6	D7←S1 and D6←S0
Ignored	Destination Address	D5, D4	D5←S1 and D4←S0
Ignored	Destination Address	D3, D2	D3←S1 and D2←S0
Ignored	Destination Address	D1, D0	D1←S1 and D0←S0
			Destination Reg←D9–D0

Receive Section Digital Interface

The receive interface can be connected to DSP processors requiring the use of only one serial port. The 15-bit I and Q samples are made available as 16-bit words, where the last bit in each word is an I/Q flag bit.

The serial data is made available on the RxDATA pin, with the I/Q flag indicating whether the 16-bit word being clocked out is an I sample or a Q sample. Although the I data is clocked out before the Q data, internally both samples are processed together. The receive interface (RxCLK, RxFRAME & RxDATA) can be 3-Stated by setting CR18 to zero, CR18 should be set high for normal operation.

When the receive section is put into sleep mode, by setting CR14 to zero, the receive interface will complete the current IQ cycle before entering into a low power sleep mode.

High Sampling Rate (CR10 =1)

The timing diagram for the receive interface is shown in Figure 3. The output word rate per channel is equal to 97.2 kHz (MCLK/64) which corresponds to 4 times the symbol rate.

When the receive section is brought out of sleep mode (CR14 = 1), the receive section will initiate an offset autocalibration routine if CR13 = 0. Once the receive offset calibration routine is complete then RxCLK will continuously shift out I and Q data, always beginning with I data. RxFRAME provides a framing signal that is used to indicate the beginning of an I or Q, 16-bit data word that is valid on the next falling edge of RxCLK. On coming out of sleep, RxFRAME goes high one clock cycle before the beginning of I data, and subsequently goes high in the same clock cycle as the last bit of each 16-bit word (both I and Q). RxDATA is valid on the falling edge of RxCLK and is clocked out MSB first, with the I/Q flag bit indicating whether the 16-bit word is an I sample or a Q sample.

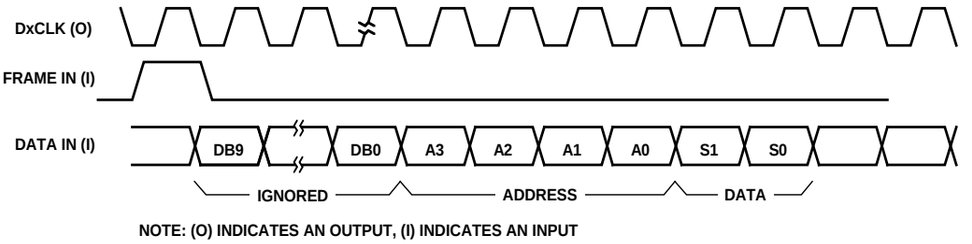


Figure 21. 6-Bit Serial Interface for Internal AD7013 Registers

Low Sampling Rate (CR10 = 0)
The timing diagram for the receive interface is shown in Figure 4. The output word rate per channel is equal to 48.6 kHz (MCLK/128) which corresponds to two times the symbol rate. The low sampling rate operates in a similar manner to that described for the high sampling rate.

AUXILIARY DACs
One 10-bit auxiliary DAC and two 8-bit auxiliary DACs are provided for extra control functions such as automatic gain control, automatic frequency control and power control. Figure 22 illustrates a simplified block diagram of the auxiliary DACs. The AUX DACs consist of high impedance current sources, designed to operate at very low currents while maintaining their DC accuracy. The DACs are designed using a current segmented architecture. The bit currents corresponding to each digital input are either routed to the analog output (bit = 1) or to AGND (bit = 0).

Each of the auxiliary DACs has independent low power sleep modes. The command register has three control bits CR17, CR16 and CR15 which control AUX DAC1, AUX DAC2 and AUX DAC3 respectively. A logic 0 represents low power sleep mode and a logic 1 represents normal operation.

The full-scale currents of the auxiliary DACs are controlled by a single external resistor, R_{SET}, connected between the FS ADJUST pin and AGND. The relationship between full-scale current and R_{SET} is given as follows:

10-*Bit AUX DAC*

$$AUX\ DAC_{FULL\ SCALE}\ (mA) = 7992 \times V_{REF}\ (V)/\ R_{SET}\ (\Omega)$$

8-*Bit AUX DACs*

$$AUX\ DAC_{FULL\ SCALE}\ (mA) = 3984 \times V_{REF}\ (V)/\ R_{SET}\ (\Omega)$$

By using smaller values of R_{SET}, thereby increasing AUX DAC full-scale current, improved INL and DNL performance is possible as shown in Table V.

Table V. AUX DAC1 INL and DNL as a Function of R_{SET}

R_{SET}	Worst Case INL (LSBs)	Worst Case DNL (LSBs)
18 kΩ	–1.45	+1.83
9 kΩ	+1.22	+1.59
4.5 kΩ	+1.18	+1.38

Digital Interface
Communication with the Command register, auxiliary DACs, ADC offset registers and ADC vernier is accomplished via the 3-pin serial interface. Either one of two loading formats may be used to write to any of the AD7013's internal registers. The first format consists of a single 16-bit serial word to write to any internal register (Table III). The second format consists of five 16-bit serial words, where only the last 6 bits in each 16-bit word are used to load five 2-bit data nibbles. The load sequence for this format is given is Table IV. The second format is only enable when the Register Address 3 is used as the destination register as shown in Table I.

PCB Layout Considerations
The use of an analog ground plane is recommended, where the ground plane extends around the analog circuitry. Both AGND and DGND should be externally tied together and connected to the analog ground plane.

Good power supply decoupling is very important for best ADC performance. A 0.1 µF ceramic decoupling capacitor should be connected between V_{AA} and the ground plane. The physical placement of the capacitor (surface mount if possible) is important and should be placed as close to the pin of the device as is physically possible. This is also applied to the V_{DD} pin. Poor power supply decoupling can lead to a degradation in ADC offsets and SNR.

The Bypass pin should be decoupled to the ground plane using a 10 nF capacitor. Large capacitor values are not recommended as this can cause the reference not to reach its final value, on power up, before ADC autocalibration has commenced.

Capacitive loading of digital outputs should be minimized as much as possible if power dissipation is a critical factor. The charging and discharging of external load capacitances can be a significant contribution to power dissipation, especially when the AD7013 is in a low power sleep mode as the DxCLK remains active.

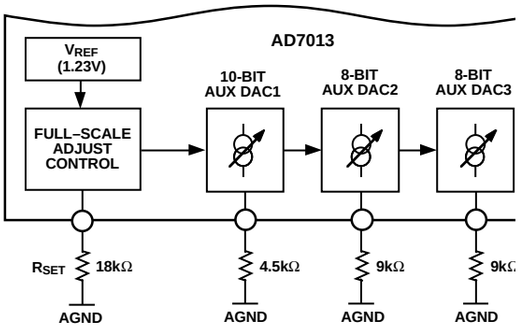


Figure 22. AUX DACs

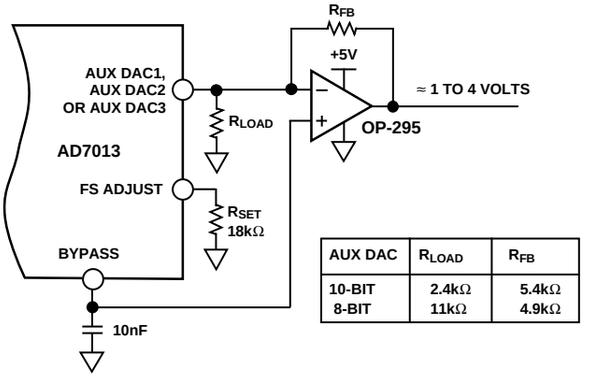
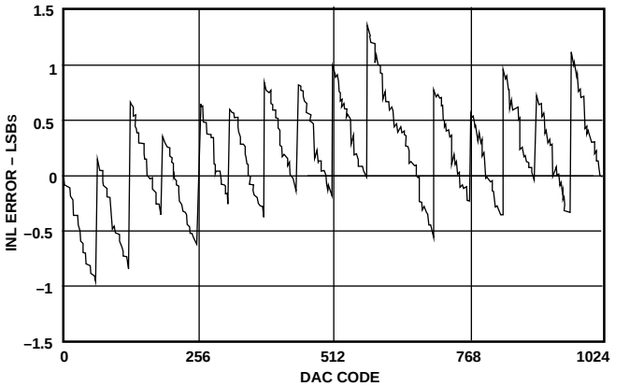
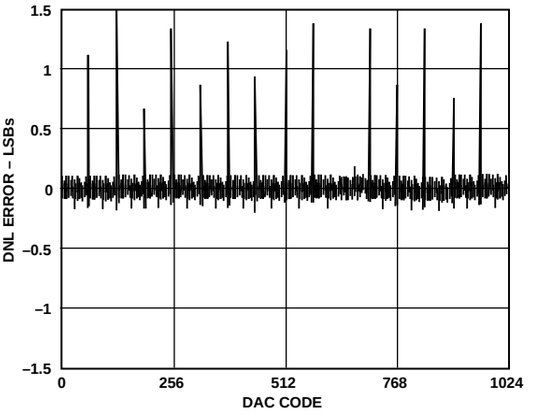


Figure 23. External Op Amp Circuitry to Extend Output Voltage Range

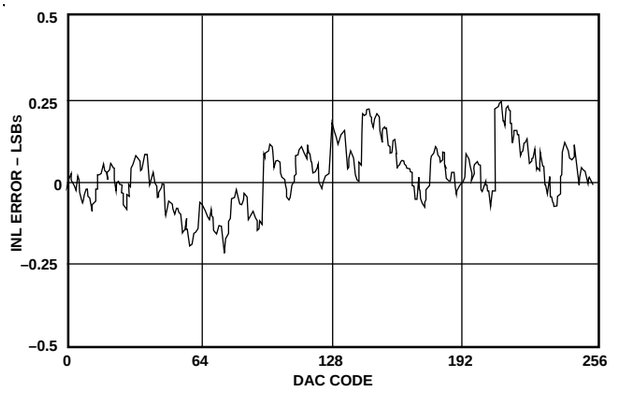
APPENDIX 1



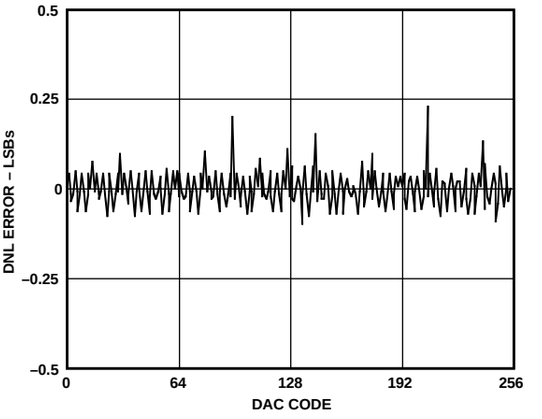
10-Bit AUX DAC1 Integral Nonlinearities (INL)



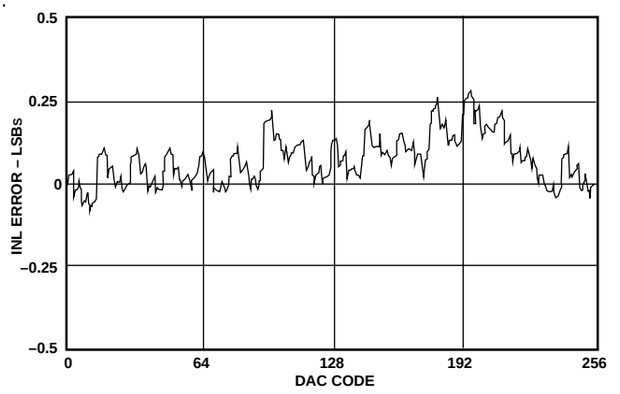
10-Bit AUX DAC1 Differential Nonlinearities (DNL)



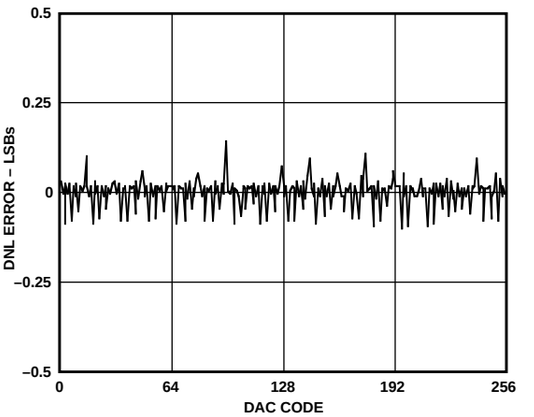
8-Bit AUX DAC2 Integral Nonlinearities (INL)



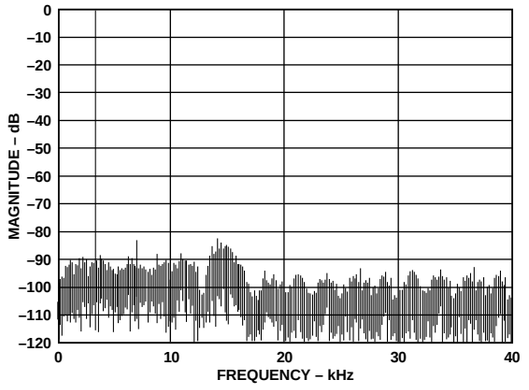
8-Bit AUX DAC2 Differential Nonlinearities (DNL)



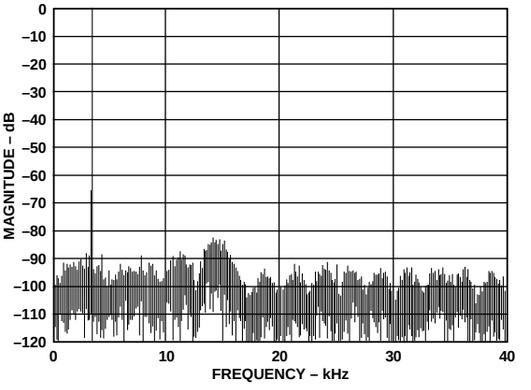
8-Bit AUX DAC3 Integral Nonlinearities (INL)



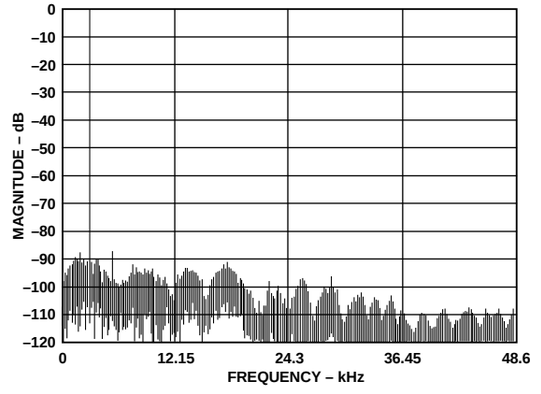
8-Bit AUX DAC3 Differential Nonlinearities (DNL)



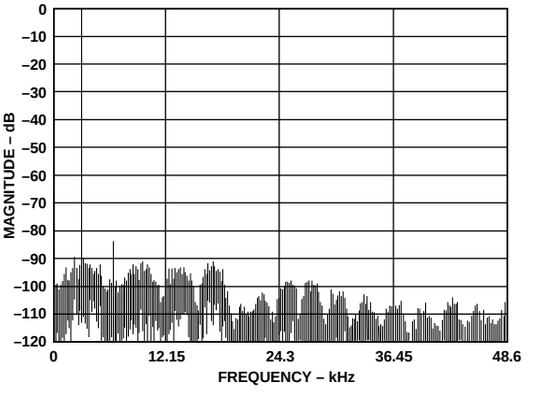
I Channel Analog Mode FFT; MCLK = 5.12 MHz



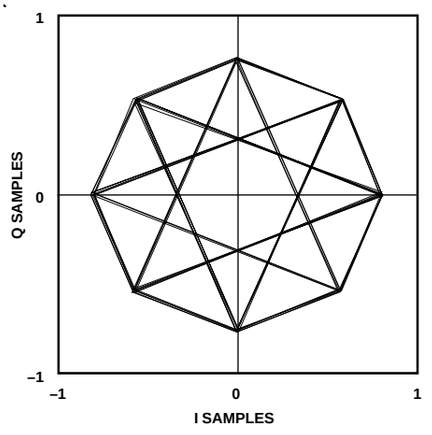
Q Channel Analog Mode FFT; MCLK = 5.12 MHz



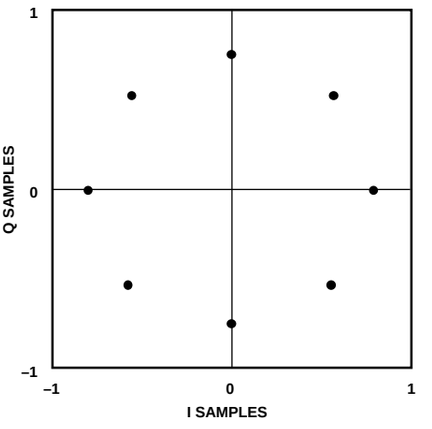
I Channel Digital Mode FFT; MCLK = 6.2208 MHz



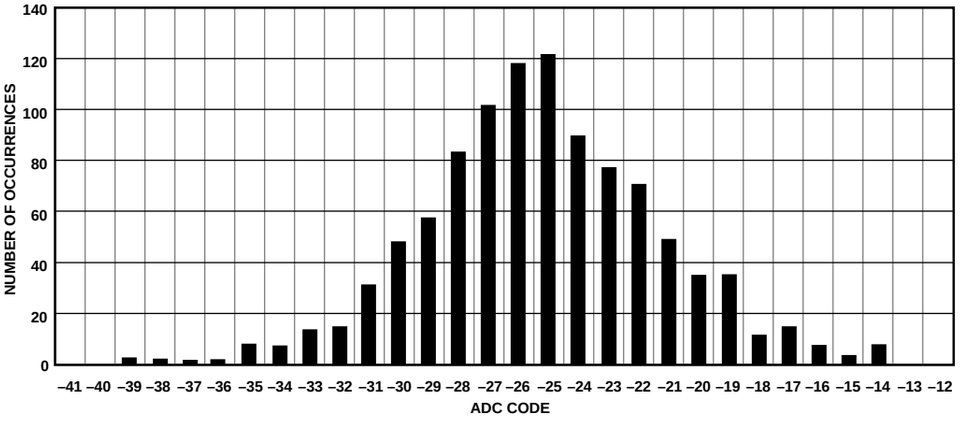
Q Channel Digital Mode FFT; MCLK = 6.2208 MHz



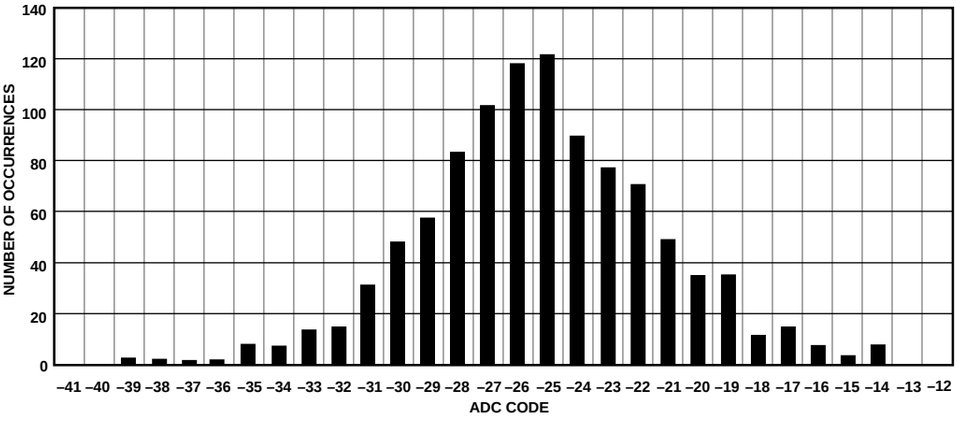
π/4 DQPSK I and Q Receive Samples



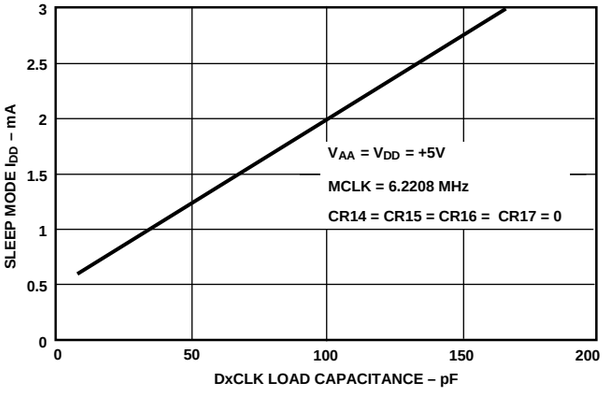
π/4 DQPSK Constellation Diagram; Typical Error Vector 2% RMS



I Channel ADC Noise Histogram with IRx and $\overline{IRx}$ Tied Together and Offset Register = 0; Number Codes = 1000, Standard Deviation = 4.44 Codes



Q Channel ADC Noise Histogram with QRx and $\overline{QRx}$ Tied Together and Offset Register = 0; Number Codes = 1000, Standard Deviation = 3.82 Codes

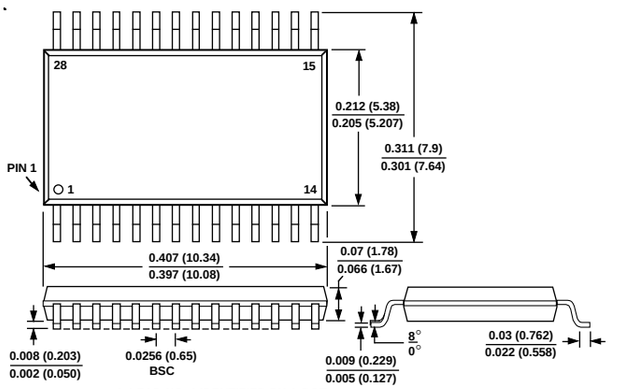


AD7013 Sleep Current as a Function of DxCLK Load Capacitance

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead SSOP
(RS-28)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

C1862a–7.5–7/94

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