- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- *EPIC*™ **(Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \bullet B \bullet C \bullet D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The 54AC11020 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11020 is characterized for operation from −40°C to 85°C.

54AC11020 . . . J PACKAGE
74AC11020 . . . D OR N PACKAGE
(TOP VIEW)

1B	1		14	NC
1A	2		13	1C
1Y	3		12	1D
GND	4		11	V_{CC}
2Y	5		10	2A
2D	6		9	2B
2C	7		8	NC

54AC11020 . . . FK PACKAGE
(TOP VIEW)

Top pins (left to right): 1C, 1D, NC, V_{CC}, 2A
Pin numbers top: 3, 2, 1, 20, 19

NC	4		18	2B
NC	5		17	NC
1B	6		16	NC
NC	7		15	NC
1A	8		14	2C

Bottom pin numbers: 9, 10, 11, 12, 13
Bottom pins (left to right): 1Y, GND, NC, 2Y, 2D

NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS				OUTPUT
A	**B**	**C**	**D**	**Y**
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

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54AC11020, 74AC11020
DUAL 4-INPUT POSITIVE-NAND GATES
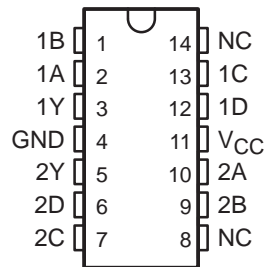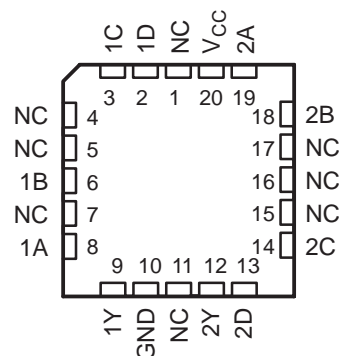
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logic symbol†

```
1A  2 ──────┐  ┌──────────────┐
1B  1 ──────┤  │      &       │
1C 13 ──────┤  │              │── 3 ── 1Y
1D 12 ──────┤  │              │
            │  │              │
2A 10 ──────┤  │              │
2B  9 ──────┤  │              │── 5 ── 2Y
2C  7 ──────┤  │              │
2D  6 ──────┘  └──────────────┘
```
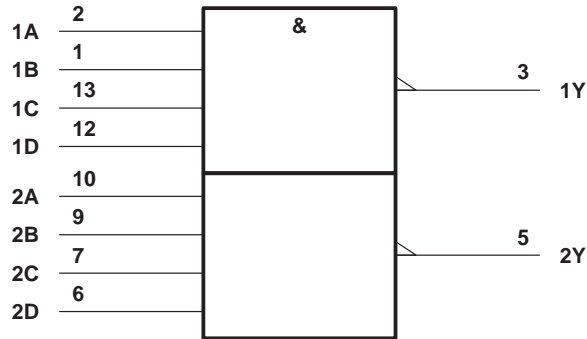
logic diagram (positive logic)

```
1A  2 ──────┐
1B  1 ──────┤ ╲
1C 13 ──────┤  )o── 3 ── 1Y
1D 12 ──────┘ ╱

2A 10 ──────┐
2B  9 ──────┤ ╲
2C  7 ──────┤  )o── 5 ── 2Y
2D  6 ──────┘ ╱
```
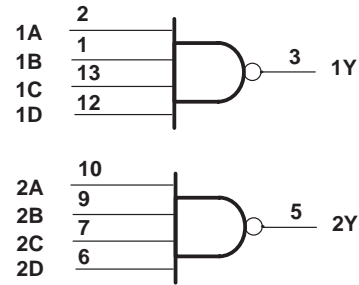
† This symbol is in accordance with ANSI/IEEE Std 91-1984
  and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±100 mA
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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recommended operating conditions

			54AC11020			74AC11020			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1			2.1			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 5.5$ V	3.85			3.85			
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V			0.9			0.9	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 5.5$ V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V			−4			−4	mA
		$V_{CC} = 4.5$ V			−24			−24	
		$V_{CC} = 5.5$ V			−24			−24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V			12			12	mA
		$V_{CC} = 4.5$ V			24			24	
		$V_{CC} = 5.5$ V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54AC11020		74AC11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = −50$ μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = −4$ mA	3 V	2.58			2.4		2.48		
	$I_{OH} = −24$ mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = −50$ mA†	5.5 V				3.85				
	$I_{OH} = −75$ mA†	5.5 V						3.85		
V_{OL}	$I_{OL} = 50$ μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 12$ mA	3 V			0.36		0.5		0.44	
	$I_{OL} = 24$ mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50$ mA†	5.5 V					1.65			
	$I_{OL} = 75$ mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

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54AC11020, 74AC11020
DUAL 4-INPUT POSITIVE-NAND GATES

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## switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11020		74AC11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	6.4	8.6	1.5	10	1.5	9.4	ns
t_{PHL}			1.5	6.4	9.2	1.5	10.7	1.5	10.1	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11020		74AC11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	4.3	8.1	1.5	7	1.5	6.7	ns
t_{PHL}			1.5	4.4	7.8	1.5	7.7	1.5	7.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	19	pF

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

VOLTAGE WAVEFORMS
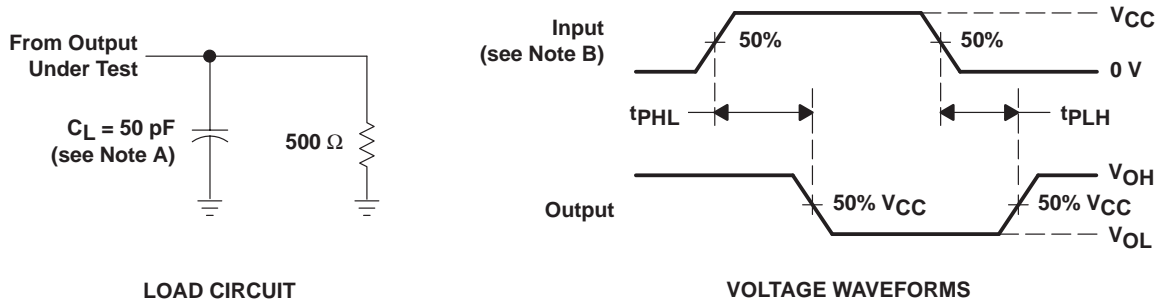
NOTES: A. C_L includes probe and jig capacitance.
       B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
       C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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