

## 74AC244 • 74ACT244

### Octal Buffer/Line Driver with 3-STATE Outputs

#### General Description

The AC/ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

#### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- ACT244 has TTL-compatible inputs

#### Ordering Code:

Order Number	Package Number	Package Description
74AC244SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC244SCX_NL (Note 1)	M20B	Pb-Free 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC244SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC244MTCX_NL (Note 1)	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC244PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT244SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT244SCX_NL (Note 1)	M20B	Pb-Free 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT244SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT244MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ACT244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT244MTCX_NL (Note 1)	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT244PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

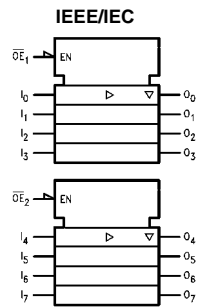
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** "\_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Please use order number as indicated.

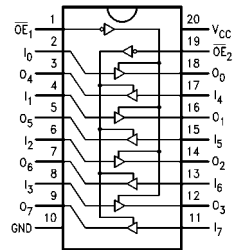
FACT™ is a trademark of Fairchild Semiconductor Corporation.

74AC244 • 74ACT244 Octal Buffer/Line Driver with 3-STATE Outputs

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$O_0-O_7$	Outputs

### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	$I_n$	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	$I_n$	
L	L	L
L	H	H
H	X	Z

X = Immaterial  
Z = High Impedance

**Absolute Maximum Ratings**(Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-out exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics for AC**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits		Guaranteed Limits		Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15	3.15	3.15	3.15			
		5.5	2.75	3.85	3.85	3.85	3.85	3.85			
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35	1.35	1.35	1.35			
		5.5	2.75	1.65	1.65	1.65	1.65	1.65			
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	2.9	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		4.5	4.49	4.4	4.4	4.4	4.4	4.4			
		5.5	5.49	5.4	5.4	5.4	5.4	5.4			
		3.0		2.56	2.4	2.46			V	$I_{OH} = 12 \text{ mA}$ $I_{OH} = 24 \text{ mA}$ $I_{OH} = 24 \text{ mA (Note 3)}$	
		4.5		3.86	3.7	3.76					
		5.5		4.86	4.7	4.76					
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1	0.1	0.1	0.1			
		5.5	0.001	0.1	0.1	0.1	0.1	0.1			
		3.0		0.36	0.50	0.44			V	$I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 3)}$	
		4.5		0.36	0.50	0.44					
		5.5		0.36	0.50	0.44					
$I_{IN}$ (Note 5)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	$V_I = V_{CC}, \text{GND}$	
$I_{OZ}$	Maximum 3-STATE Current	5.5		$\pm 0.25$	$\pm 5.0$	$\pm 2.5$	$\pm 2.5$	$\mu\text{A}$	$V_I (\text{OE}) = V_{IL}, V_{IH}$ $V_I = V_{CC}, V_{GND}$ $V_O = V_{CC}, \text{GND}$		
$I_{OLD}$	Minimum Dynamic Output Current (Note 4)	5.5			50	75	75	mA	$V_{OLD} = 1.65V \text{ Max}$		
$I_{OHD}$	Output Current (Note 4)	5.5			-50	-75	-75	mA	$V_{OHD} = 3.85V \text{ Min}$		
$I_{CC}$ (Note 5)	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND		

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

## DC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -55°C to +125°C	T <sub>A</sub> = -40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level	4.5	1.5	2.0	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
	Input Voltage	5.5	1.5	2.0	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level	4.5	1.5	0.8	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
	Input Voltage	5.5	1.5	0.8	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I <sub>OUT</sub> = -50 μA
		5.5	5.49	5.4	5.4	5.4		
	4.5		3.86	3.70	3.76	V	I <sub>OH</sub> = 12 I <sub>OH</sub> = 24 mA	
	5.5		4.86	4.70	4.76	V	I <sub>OH</sub> = 24 mA (Note 6)	
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		5.5	0.001	0.1	0.1	0.1		
	4.5		0.36	0.50	0.44	V	I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 24 mA	
	5.5		0.36	0.50	0.44	V	I <sub>OL</sub> = 24 mA (Note 6)	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>OZ</sub>	Maximum 3-STATE Current	5.5		±0.25	±5.0	±2.5	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.6	1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	Minimum Dynamic	5.5			50	75	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current (Note 7)	5.5			-50	-75	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Note 6:** All outputs loaded; thresholds on input associated with output under test.

**Note 7:** Maximum test duration 2.0 ms, one output loaded at a time.

**AC Electrical Characteristics for AC**

Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	3.3	2.0	6.5	9.0	1.0	12.5	1.5	10.0	ns
	Data to Output	5.0	1.5	5.0	7.0	1.0	9.5	1.0	7.5	
t <sub>PHL</sub>	Propagation Delay	3.3	2.0	6.5	9.0	1.0	12.0	2.0	10.0	ns
	Data to Output	5.0	1.5	5.0	7.0	1.0	9.0	1.0	7.5	
t <sub>PZH</sub>	Output Enable Time	3.3	2.0	6.0	10.5	1.0	11.5	1.5	11.0	ns
		5.0	1.5	5.0	7.0	1.0	9.0	1.5	8.0	
t <sub>PZL</sub>	Output Enable Time	3.3	2.5	7.5	10.0	1.0	13.0	2.0	11.0	ns
		5.0	1.5	5.5	8.0	1.0	10.5	1.5	8.5	
t <sub>PHZ</sub>	Output Disable Time	3.3	3.0	7.0	10.0	1.0	12.5	1.5	10.5	ns
		5.0	2.5	6.5	9.0	1.0	10.5	1.0	9.5	
t <sub>PLZ</sub>	Output Disable Time	3.3	2.5	7.5	10.5	1.0	13.0	2.5	11.5	ns
		5.0	2.0	6.5	9.0	1.0	11.0	2.0	9.5	

**Note 8:** Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

**AC Electrical Characteristics for ACT**

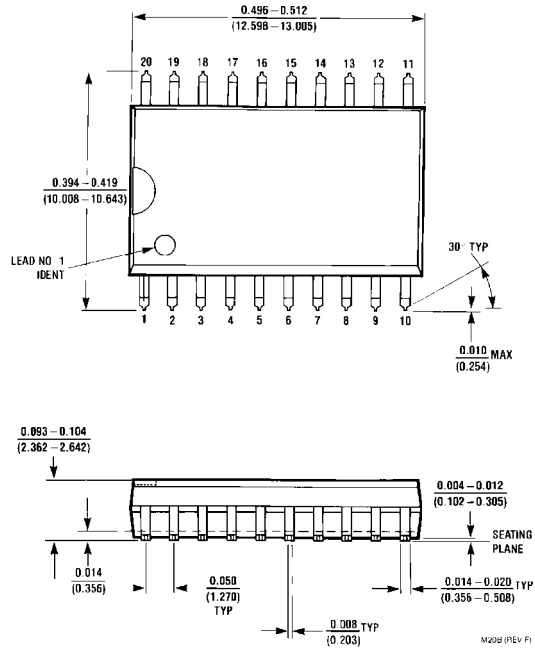
Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	5.0	2.0	6.5	9.0	1.0	10.0	1.5	10.0	ns
	Data to Output									
t <sub>PHL</sub>	Propagation Delay	5.0	2.0	7.0	9.0	1.0	10.0	1.5	10.0	ns
	Data to Output									
t <sub>PZH</sub>	Output Enable Time	5.0	1.5	6.0	8.5	1.0	9.5	1.0	9.5	ns
t <sub>PZL</sub>	Output Enable Time	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	2.5	7.5	10.0	1.0	11.5	2.0	10.5	ns

**Note 9:** Voltage Range 5.0 is 5.0V ± 0.5V

**Capacitance**

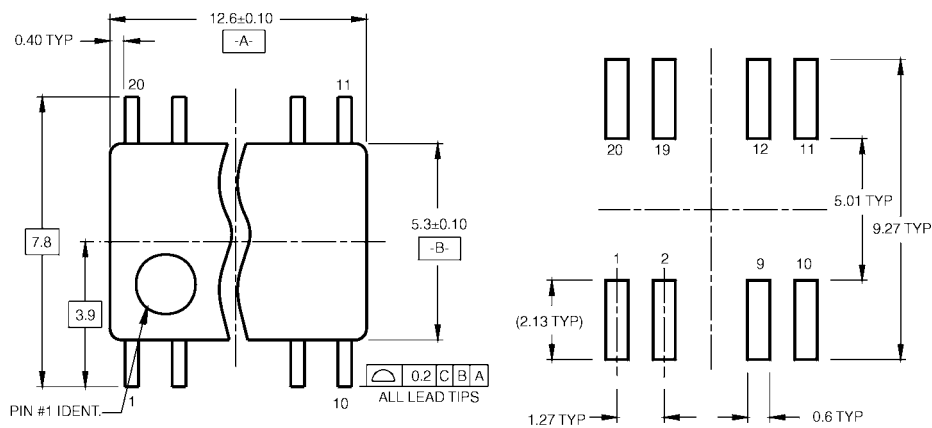
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	45.0	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B**

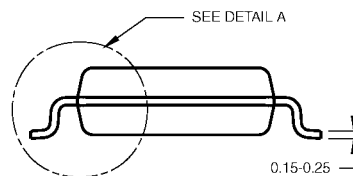
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

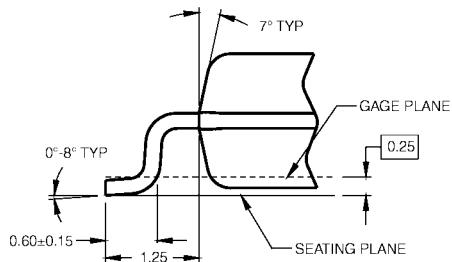


DIMENSIONS ARE IN MILLIMETERS



- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

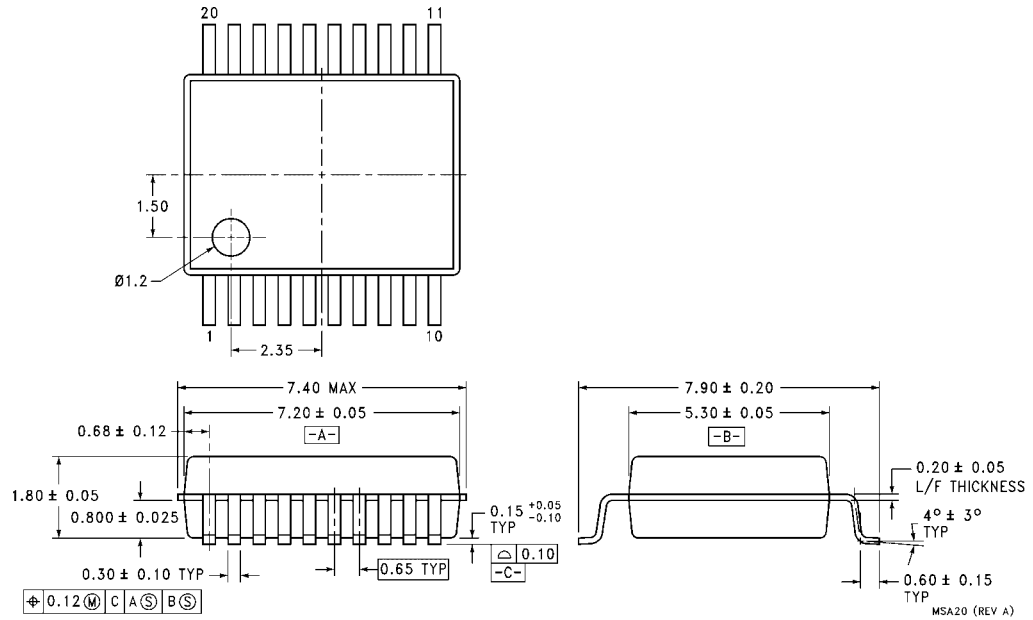
M20DRevB1



DETAIL A

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

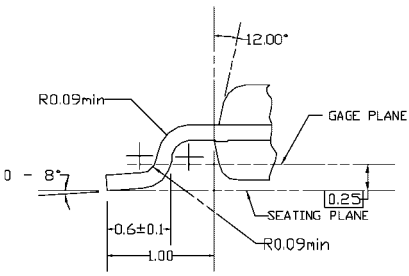
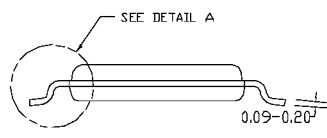
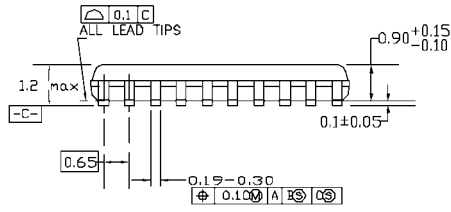
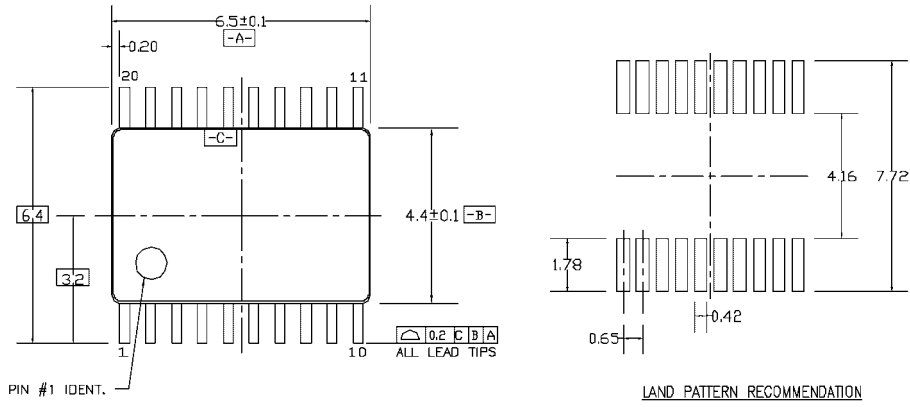
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide  
Package Number MSA20**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)