
HD74AC139/HD74ACT139

Dual 1-of-4 Decoder/Demultiplexer

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Description

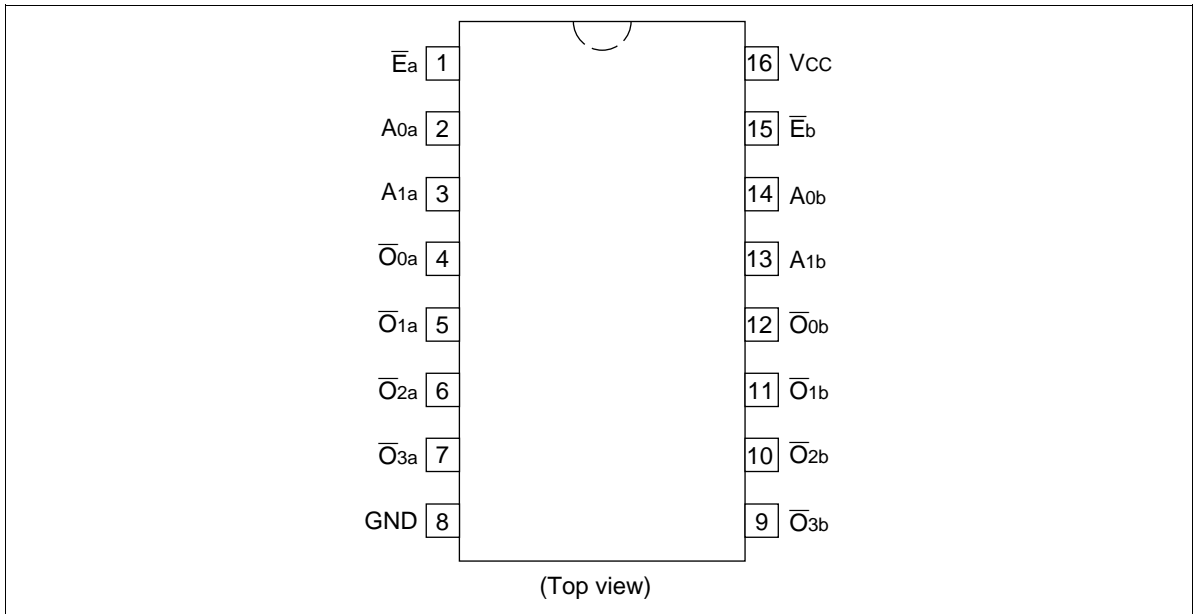
The HD74AC139/HD74ACT139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually-exclusive active-Low outputs. Each decoder has an active-Low Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the HD74AC139/HD74ACT139 can be used as a function generator providing all four minterms of two variables.

Features

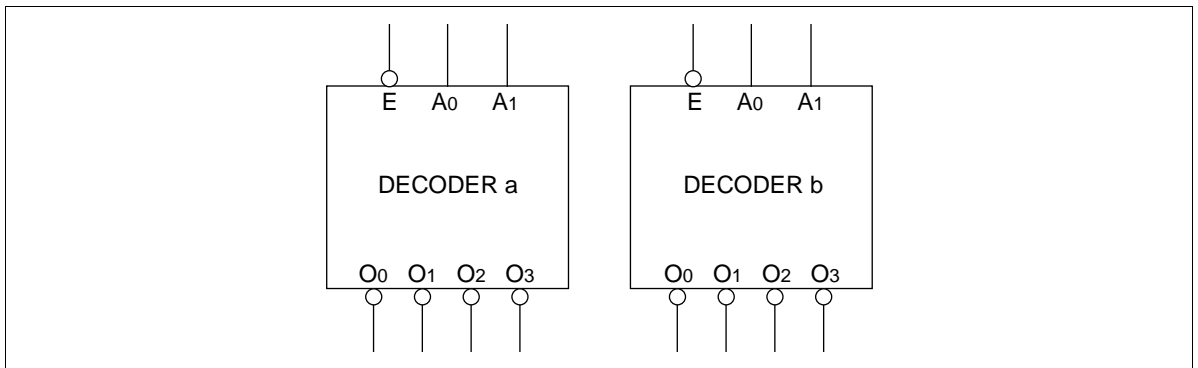
- Multifunction Capability
- Two Completely Independent 1-of-4 Decoders
- Active Low Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- HD74ACT139 has TTL-Compatible Inputs

HD74AC139/HD74ACT139

Pin Arrangement



Logic Symbol



Pin Names

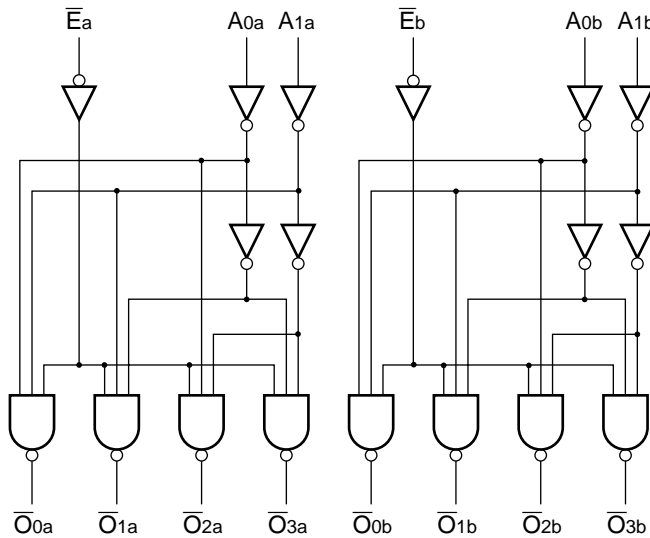
A_0, A_1 Address Inputs

\bar{E} Enable Inputs

\bar{O}_0 to \bar{O}_3 Outputs

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Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The HD74AC139/HD74ACT139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0 to A_1) and provides four mutually exclusive active-Low outputs (\bar{O}_0 to \bar{O}_3). Each decoder has an active-Low enable (\bar{E}). When \bar{E} is High all outputs are forced High. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the HD74AC139/HD74ACT139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure a, and thereby reducing the number of packages required in a logic network.

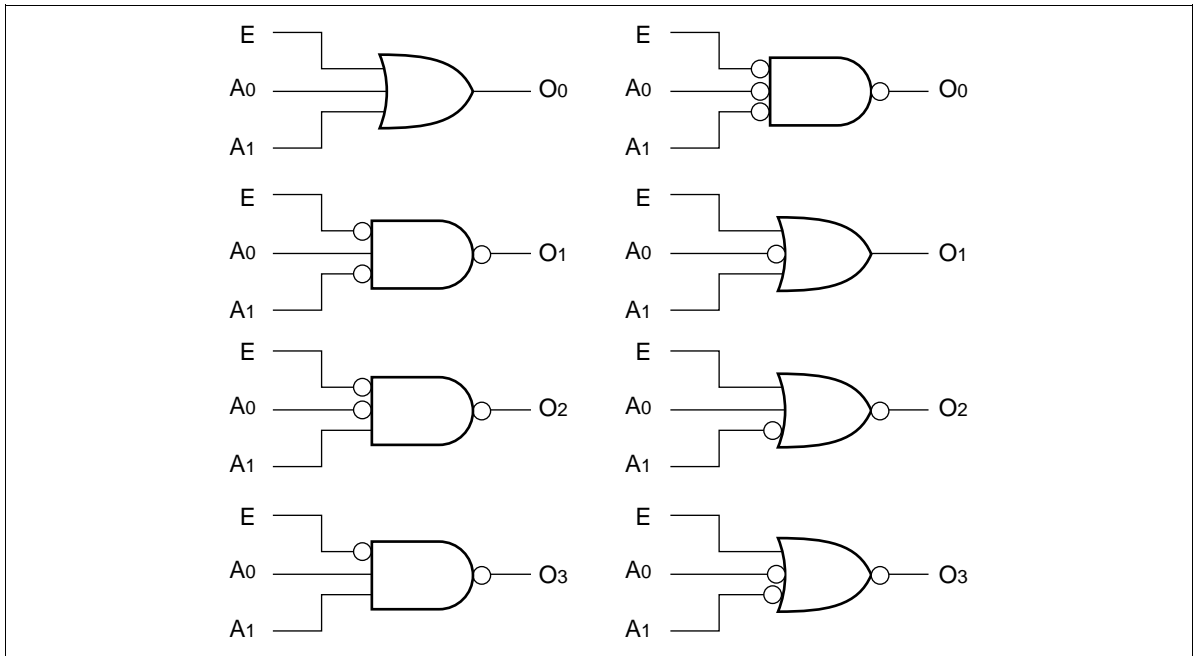
Truth Table

| Inputs | | | Outputs | | | |
|-----------|-------|-------|-------------|-------------|-------------|-------------|
| \bar{E} | A_0 | A_1 | \bar{O}_0 | \bar{O}_1 | \bar{O}_2 | \bar{O}_3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | H | L | H | L | H | H |
| L | L | H | H | H | L | H |
| L | H | H | H | H | H | L |

H : High Voltage Level
 L : Low Voltage Level
 X : Immaterial

HD74AC139/HD74ACT139

Figure a: Gate Functions (each half)



DC Characteristics (unless otherwise specified)

| Item | Symbol | Max | Unit | Condition |
|--|-----------|-----|---------|--|
| Maximum quiescent supply current | I_{CC} | 80 | μA | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$ |
| Maximum quiescent supply current | I_{CC} | 8.0 | μA | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^\circ C$ |
| Maximum I_{CC}/input (HD74ACT139) | I_{CCT} | 1.5 | mA | $V_{IN} = V_{CC} - 2.1 V$, $V_{CC} = 5.5 V$ $T_a = \text{Worst case}$ |

AC Characteristics: HD74AC139

| Item | Symbol | V _{CC} (V)* ¹ | Ta = +25°C C _L = 50 pF | | | Ta = -40°C to +85°C C _L = 50 pF | | Unit |
|---|------------------|-----------------------------------|--------------------------------------|-----|------|---|------|------|
| | | | Min | Typ | Max | Min | Max | |
| Propagation delay A _n to \overline{O}_n | t _{PLH} | 3.3 | 1.0 | 8.0 | 11.5 | 1.0 | 13.0 | ns |
| | | 5.0 | 1.0 | 6.5 | 8.5 | 1.0 | 9.5 | |
| Propagation delay A _n to \overline{O}_n | t _{PHL} | 3.3 | 1.0 | 7.0 | 10.0 | 1.0 | 11.0 | ns |
| | | 5.0 | 1.0 | 5.5 | 7.5 | 1.0 | 8.5 | |
| Propagation delay \overline{E}_n to \overline{O}_n | t _{PLH} | 3.3 | 1.0 | 9.5 | 12.0 | 1.0 | 13.0 | ns |
| | | 5.0 | 1.0 | 7.0 | 8.5 | 1.0 | 10.0 | |
| Propagation delay \overline{E}_n to \overline{O}_n | t _{PHL} | 3.3 | 1.0 | 8.0 | 10.0 | 1.0 | 11.0 | ns |
| | | 5.0 | 1.0 | 6.0 | 7.5 | 1.0 | 8.5 | |

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

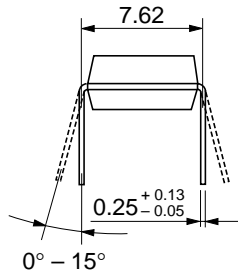
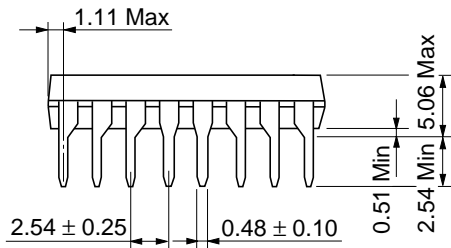
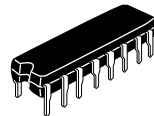
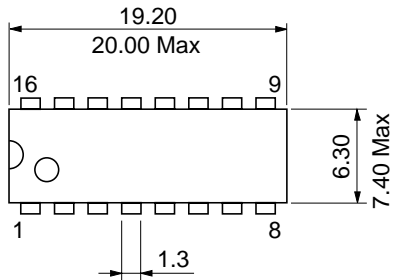
AC Characteristics: HD74ACT139

| Item | Symbol | V _{CC} (V)* ¹ | Ta = +25°C C _L = 50 pF | | | Ta = -40°C to +85°C C _L = 50 pF | | Unit |
|---|------------------|-----------------------------------|--------------------------------------|-----|------|---|------|------|
| | | | Min | Typ | Max | Min | Max | |
| Propagation delay A _n to \overline{O}_n | t _{PLH} | 5.0 | 1.0 | 6.0 | 8.5 | 1.0 | 9.5 | ns |
| Propagation delay A _n to O _n | t _{PHL} | 5.0 | 1.0 | 6.0 | 9.5 | 1.0 | 10.5 | ns |
| Propagation delay \overline{E}_n to \overline{O}_n | t _{PLH} | 5.0 | 1.0 | 7.0 | 10.0 | 1.0 | 11.0 | ns |
| Propagation delay \overline{E}_n to O _n | t _{PHL} | 5.0 | 1.0 | 7.0 | 9.5 | 1.0 | 10.5 | ns |

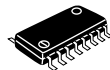
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

| Item | Symbol | Typ | Unit | Condition |
|-------------------------------|-----------------|------|------|-------------------------|
| Input capacitance | C _{IN} | 4.5 | pF | V _{CC} = 5.5 V |
| Power dissipation capacitance | C _{PD} | 40.0 | pF | V _{CC} = 5.0 V |



| | |
|--------------------------|----------|
| Hitachi Code | DP-16 |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 1.07 g |



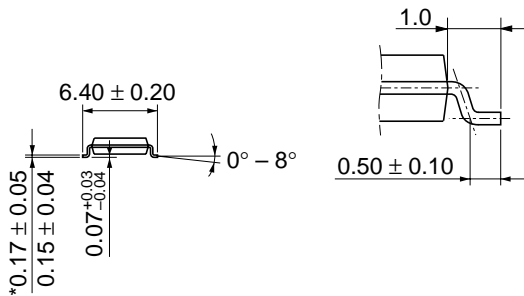
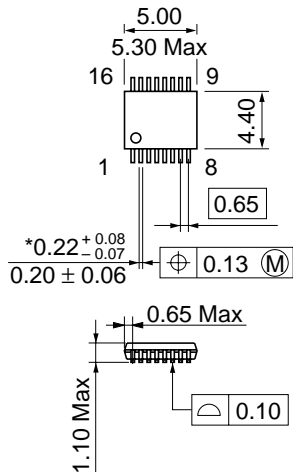
*Dimension including the plating thickness
Base material dimension

| | |
|--------------------------|----------|
| Hitachi Code | FP-16DA |
| JEDEC | — |
| EIAJ | Conforms |
| Weight (reference value) | 0.24 g |



*Dimension including the plating thickness
Base material dimension

| | |
|--------------------------|----------|
| Hitachi Code | FP-16DN |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 0.15 g |



*Dimension including the plating thickness
 Base material dimension

| | |
|--------------------------|----------|
| Hitachi Code | TTP-16DA |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.05 g |

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