

74F112

Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 74F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on \bar{S}_D or \bar{C}_D prevents clocking and forces Q or \bar{Q} HIGH, respectively.

Simultaneous LOW signals on \bar{S}_D and \bar{C}_D force both Q and \bar{Q} HIGH.

Asynchronous Inputs:

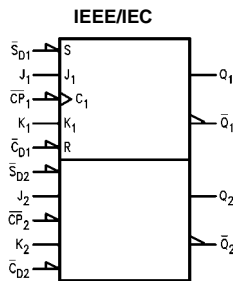
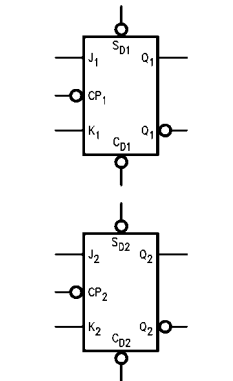
- LOW input to \bar{S}_D sets Q to HIGH level
- LOW input to \bar{C}_D sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

Ordering Code:

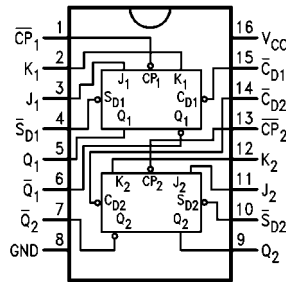
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74F112SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| 74F112SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F112PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

| Pin Names | Description | U.L. | Input I_{IH}/I_{IL} |
|--|--|----------|------------------------|
| | | HIGH/LOW | Output I_{OH}/I_{OL} |
| J_1, J_2, K_1, K_2 | Data Inputs | 1.0/1.0 | 20 μ A/-0.6 mA |
| $\overline{CP}_1, \overline{CP}_2$ | Clock Pulse Inputs (Active Falling Edge) | 1.0/4.0 | 20 μ A/-2.4 mA |
| $\overline{CD}_1, \overline{CD}_2$ | Direct Clear Inputs (Active LOW) | 1.0/5.0 | 20 μ A/-3.0 mA |
| $\overline{SD}_1, \overline{SD}_2$ | Direct Set Inputs (Active LOW) | 1.0/5.0 | 20 μ A/-3.0 mA |
| $Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$ | Outputs | 50/33.3 | -1 mA/20 mA |

Truth Table

| Inputs | | | | | Outputs | |
|------------------|------------------|-----------------|---|---|------------------|------------------|
| \overline{S}_D | \overline{C}_D | \overline{CP} | J | K | Q | \overline{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H | H |
| H | H | \sim | h | h | \overline{Q}_0 | Q_0 |
| H | H | \sim | l | h | L | H |
| H | H | \sim | h | l | H | L |
| H | H | \sim | l | l | Q_0 | \overline{Q}_0 |

H (h) = HIGH Voltage Level

L (l) = LOW Voltage Level

X = Immaterial

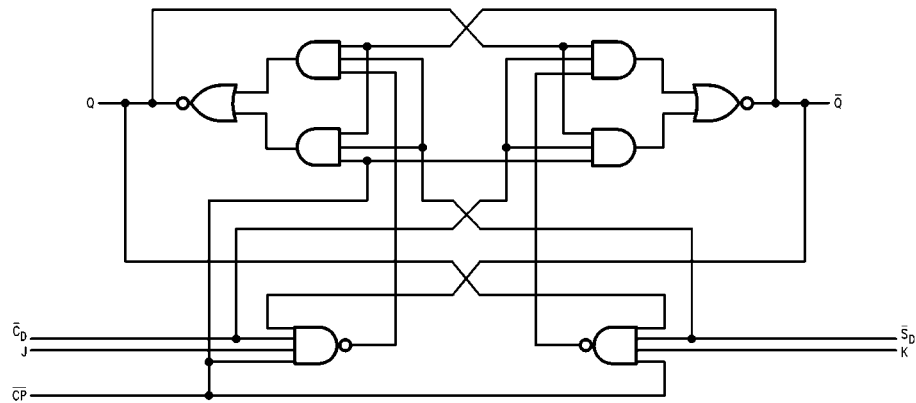
\sim = HIGH-to-LOW Clock Transition

$Q_0(\overline{Q}_0)$ = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram

(One Half Shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

| | |
|---|-------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |

Voltage Applied to Output

in HIGH State (with V_{CC} = 0V)Standard Output -0.5V to V_{CC}

3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA)**Recommended Operating Conditions**

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

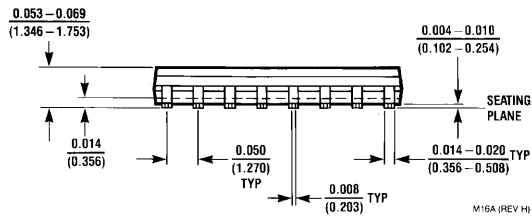
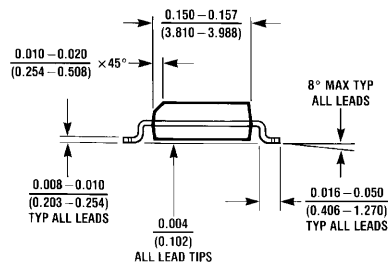
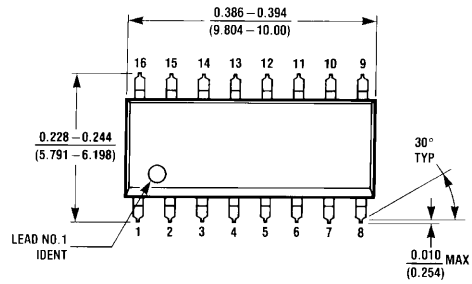
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

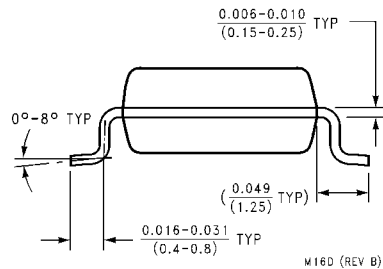
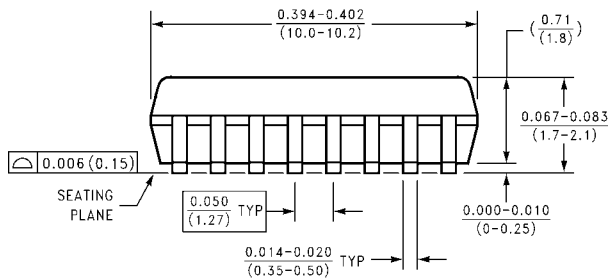
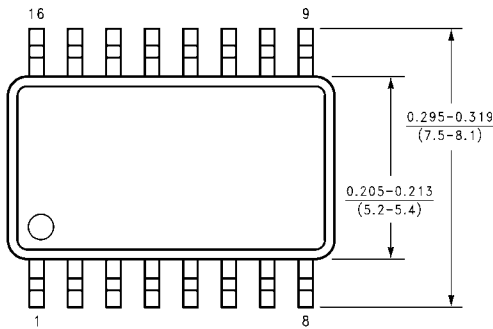
| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|---------------------|-----|------|-------|-----------------|--|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 10% V _{CC} | 2.5 | | V | Min | I _{OH} = -1 mA |
| | | 5% V _{CC} | 2.7 | | | | I _{OH} = -1 mA |
| V _{OL} | Output LOW Voltage | 10% V _{CC} | | 0.5 | V | Min | I _{OL} = 20 mA |
| I _{IH} | Input HIGH Current | | | 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BV1} | Input HIGH Current Breakdown Test | | | 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEX} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA All other pins grounded |
| I _{OD} | Output Leakage Circuit Current | | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All other pins grounded |
| I _{IL} | Input LOW Current | | | -0.6 | mA | Max | V _{IN} = 0.5V (J _n , K _n) |
| | | | | -2.4 | | | V _{IN} = 0.5V (\overline{CP}_n) |
| | | | | -3.0 | | | V _{IN} = 0.5V (\overline{CD}_n , \overline{SD}_n) |
| I _{OS} | Output Short-Circuit Current | -60 | | -150 | mA | Max | V _{OUT} = 0V |
| I _{CCH} | Power Supply Current | | 12 | 19 | mA | Max | V _O = HIGH |
| I _{CCL} | Power Supply Current | | 12 | 19 | mA | Max | V _O = LOW |

| AC Electrical Characteristics | | | | | | | |
|-------------------------------|--|---|-----|--|--|-------|-------|
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
| | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum Clock Frequency | 85 | 105 | | 80 | | MHz |
| t _{PLH} | Propagation Delay | 2.0 | 5.0 | 6.5 | 2.0 | 7.5 | ns |
| t _{PHL} | \overline{CP}_n to Q _n or \overline{Q}_n | 2.0 | 5.0 | 6.5 | 2.0 | 7.5 | |
| t _{PLH} | Propagation Delay | 2.0 | 4.5 | 6.5 | 2.0 | 7.5 | ns |
| t _{PHL} | \overline{C}_{Dn} , \overline{S}_{Dn} to \overline{Q}_n , \overline{Q}_n | 2.0 | 4.5 | 6.5 | 2.0 | 7.5 | |
| AC Operating Requirements | | | | | | | |
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V | | T _A = 0°C to +70°C V _{CC} = +5.0V | | Units | |
| | | Min | Max | Min | Max | | |
| t _S (H) | Setup Time, HIGH or LOW | 4.0 | | 5.0 | | ns | |
| t _S (L) | J _n or K _n to \overline{CP}_n | 3.0 | | 3.5 | | | |
| t _H (H) | Hold Time, HIGH or LOW | 0 | | 0 | | ns | |
| t _H (L) | J _n or K _n to \overline{CP}_n | 0 | | 0 | | | |
| t _W (H) | \overline{CP} Pulse Width | 4.5 | | 5.0 | | ns | |
| t _W (L) | HIGH or LOW | 4.5 | | 5.0 | | | |
| t _W (L) | Pulse Width, LOW \overline{C}_{Dn} or \overline{S}_{Dn} | 4.5 | | 5.0 | | ns | |
| t _{REC} | Recovery Time \overline{S}_{Dn} , \overline{C}_{Dn} to \overline{CP} | 4.0 | | 5.0 | | ns | |

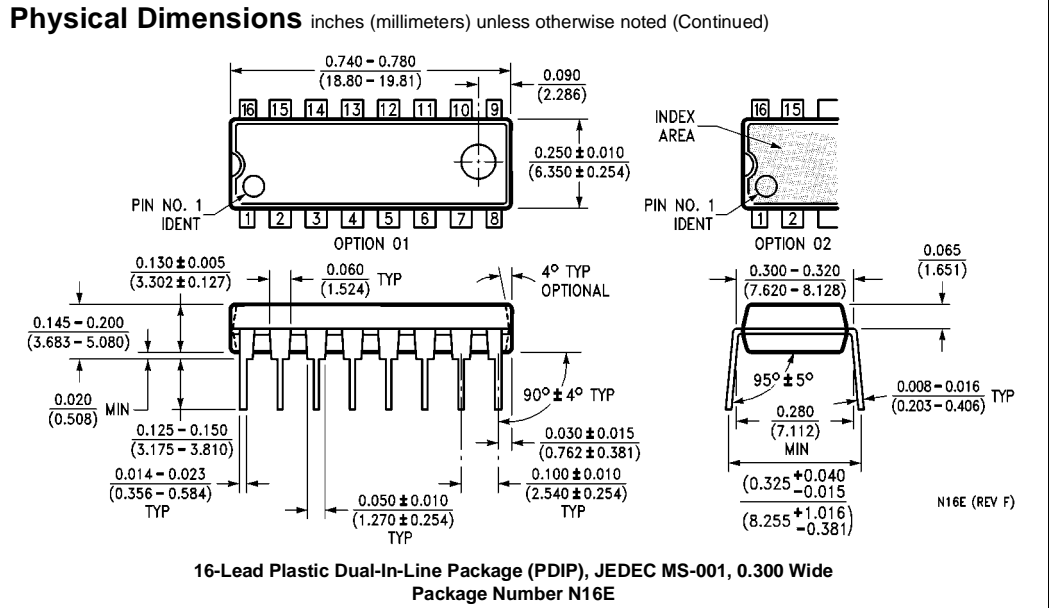
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D



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