FAIRCHILD SEMICONDUCTOR™

April 1988
Revised August 1999

74F251A
8-Input Multiplexer with 3-STATE Outputs

General Description

The 74F251A is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

Features

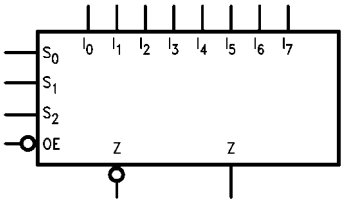
- Multifunctional capability
- On-chip select logic decoding
- Inverting and non-inverting 3-STATE outputs

Ordering Code:

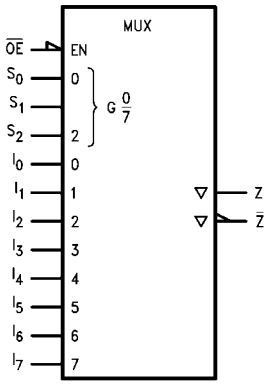
Order Number	Package Number	Package Description
74F251ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F251ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F251APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

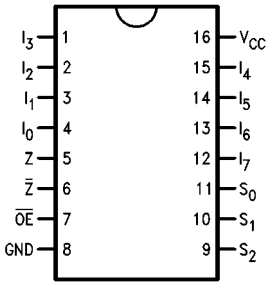
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
S_0–S_2	Select Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{OE}$	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
I_0–I_7	Multiplexer Inputs	1.0/1.0	20 µA/–0.6 mA
Z	3-STATE Multiplexer Output	150/40 (33.3)	–3 mA/24 mA (20 mA)
$\overline{Z}$	Complementary 3-STATE Multiplexer Output	150/40 (33.3)	–3 mA/24 mA (20 mA)

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 +$$
$$I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 +$$
$$I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 +$$
$$I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

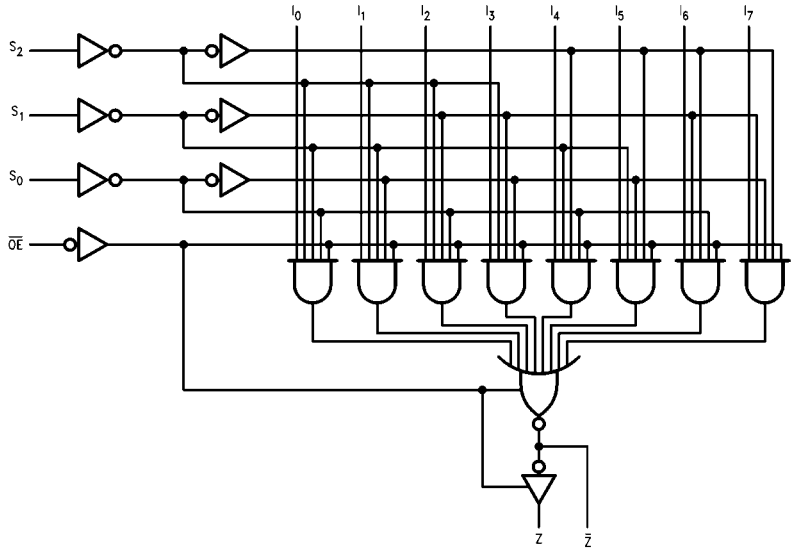
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

Truth Table

Inputs				Outputs	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

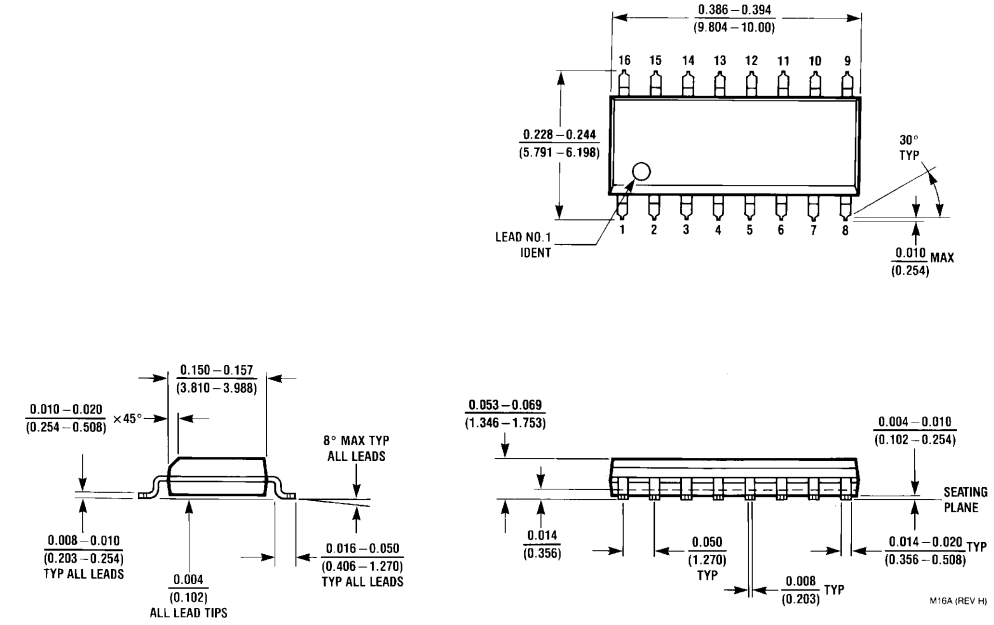
DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		10% V_{CC}	2.4					I_{OH} = −3 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 24 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	µA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	µA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CCL}	Power Supply Current			15	22	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			16	24	mA	Max	V_O = HIGH Z

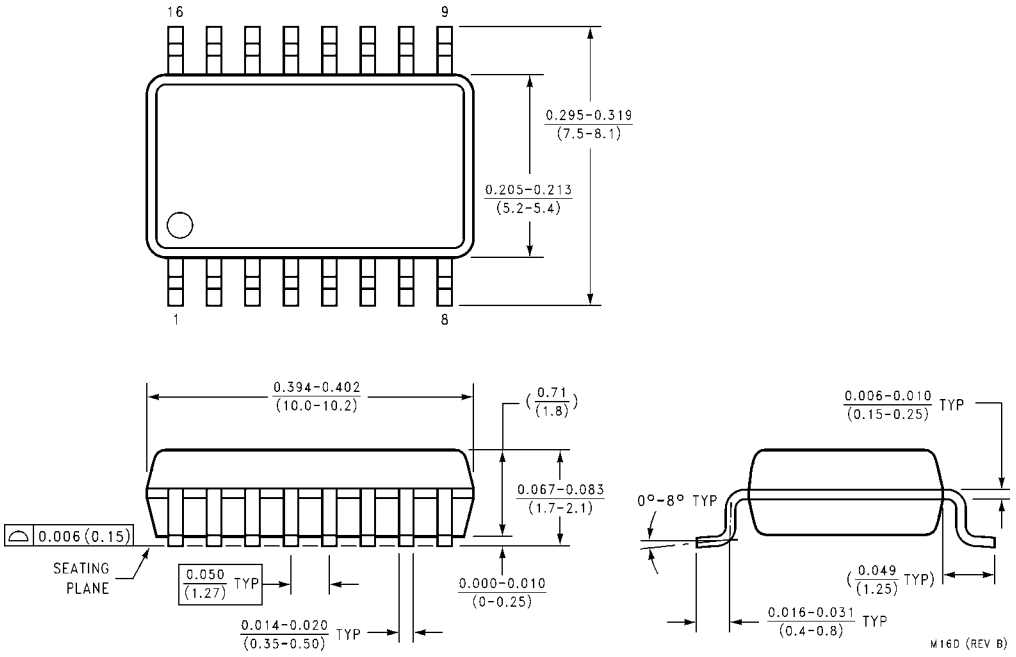
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.5	6.0	9.0	3.5	11.5	3.5	9.5	ns
t_{PHL}	S_n to $\overline{Z}$	3.2	5.0	7.5	3.2	8.0	3.2	7.5	
t_{PLH}	Propagation Delay	4.5	7.5	10.5	3.5	14.0	4.5	12.5	ns
t_{PHL}	S_n to Z	4.0	6.0	8.5	3.0	10.5	4.0	9.0	
t_{PLH}	Propagation Delay	3.0	5.0	6.5	2.5	8.0	3.0	7.0	ns
t_{PHL}	I_n to $\overline{Z}$	1.5	2.5	4.0	1.5	6.0	1.5	5.0	
t_{PLH}	Propagation Delay	3.5	5.0	7.0	2.5	9.0	2.5	8.0	ns
t_{PHL}	I_n to Z	3.5	5.5	7.0	3.5	9.0	3.5	7.5	
t_{PZH}	Output Enable Time	2.5	4.3	6.0	2.0	7.0	2.5	7.0	ns
t_{PZL}	$\overline{OE}$ to $\overline{Z}$	2.5	4.3	6.0	2.5	7.5	2.5	6.5	
t_{PHZ}	Output Disable Time	2.5	4.0	5.5	2.5	6.0	2.5	6.0	
t_{PLZ}	$\overline{OE}$ to $\overline{Z}$	1.5	3.0	4.5	1.5	5.0	1.5	4.5	
t_{PZH}	Output Enable Time	3.5	5.0	7.0	3.0	8.5	3.0	7.5	ns
t_{PZL}	$\overline{OE}$ to Z	3.5	5.5	7.5	3.5	9.0	3.5	8.0	
t_{PHZ}	Output Disable Time	2.0	3.8	5.5	2.0	5.5	2.0	5.5	
t_{PLZ}	$\overline{OE}$ to Z	1.5	3.0	4.5	1.5	5.5	1.5	4.5	

Physical Dimensions inches (millimeters) unless otherwise noted

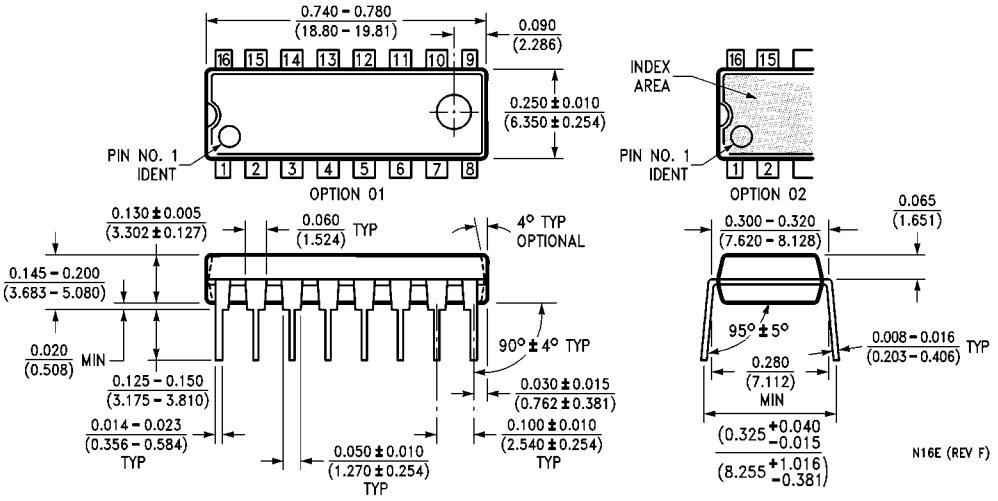


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E