

74F841 10-Bit Transparent Latch

General Description

The 74F841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 74F841 is a 10-bit transparent latch, a 10-bit version of the 74F373.

Features

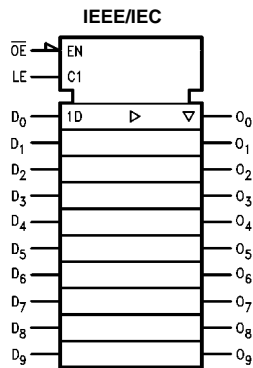
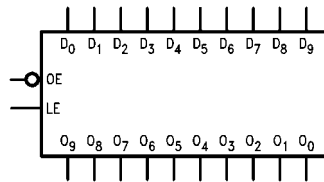
- 3-STATE output

Ordering Code:

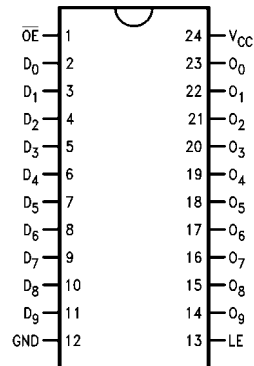
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74F841SC | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74F841SPC | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
|--------------------------------|---------------------|------------------|---|
| D ₀ -D ₉ | Data Inputs | 1.0/1.0 | 20 μ A/-0.6 mA |
| O ₀ -O ₉ | 3-STATE Outputs | 150/40 | -3 mA/24 mA |
| \overline{OE} | Output Enable Input | 1.0/1.0 | 20 μ A/-0.6 mA |
| LE | Latch Enable | 1.0/1.0 | 20 μ A/-0.6 mA |

Functional Description

The 74F841 device consists of ten D-type latches with 3-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

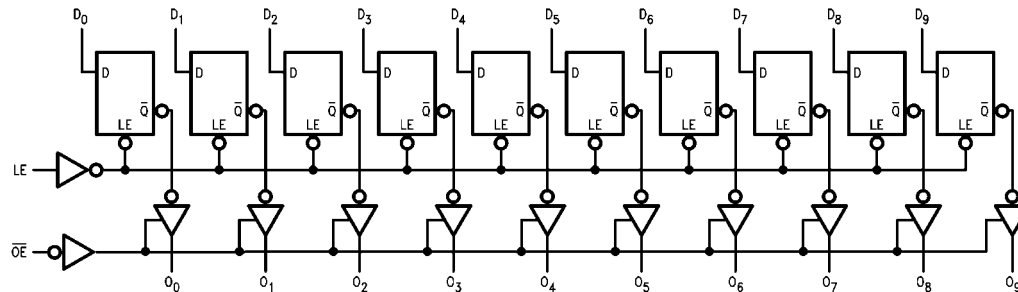
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

Function Table

| Inputs | | | Internal | Output | Function |
|-----------------|----|---|----------|--------|-------------|
| \overline{OE} | LE | D | Q | O | |
| X | X | X | X | Z | High Z |
| H | H | L | L | Z | High Z |
| H | H | H | H | Z | High Z |
| H | L | X | NC | Z | Latched |
| L | H | L | L | L | Transparent |
| L | H | H | H | H | Transparent |
| L | L | X | NC | NC | Latched |
| L | X | X | H | H | Preset |
| L | X | X | L | L | Clear |
| L | X | X | H | H | Preset |
| H | L | X | L | Z | Latched |
| H | L | X | H | Z | Latched |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance
 NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

| | |
|--|--------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| 3-STATE Output | -0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |

Recommended Operating Conditions

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

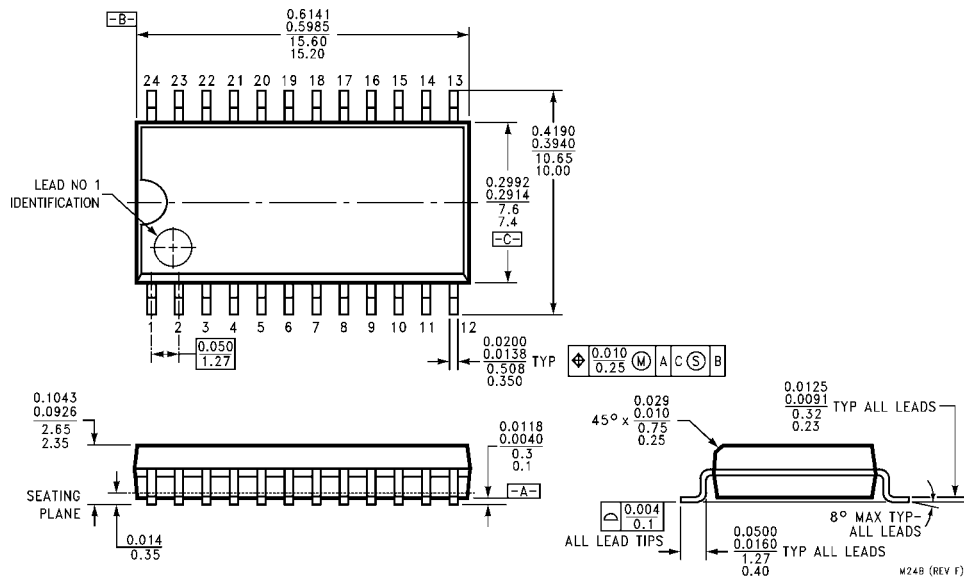
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|--|--------------------------|------|-------|-----------------|--|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 10% V _{CC} 10% V _{CC} 5% V _{CC} 5% V _{CC} | 2.5 2.4 2.7 2.7 | | V | Min | I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA |
| V _{OL} | Output LOW Voltage | 10% V _{CC} | | 0.5 | V | Min | I _{OL} = 24 mA |
| I _{IH} | Input HIGH Current | | | 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEX} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | -0.6 | mA | Max | V _{IN} = 0.5V |
| I _{OZH} | Output Leakage Current | | | 50 | μA | Max | V _{OUT} = 2.7V |
| I _{OZL} | Output Leakage Current | | | -50 | μA | Max | V _{OUT} = 0.5V |
| I _{OS} | Output Short-Circuit Current | -60 | | -150 | mA | Max | V _{OUT} = 0V |
| I _{ZZ} | Bus Drainage Test | | | 500 | μA | 0.0V | V _{OUT} = 5.25V |
| I _{CCZ} | Power Supply Current | | 69 | 92 | mA | Max | V _O = HIGH Z |

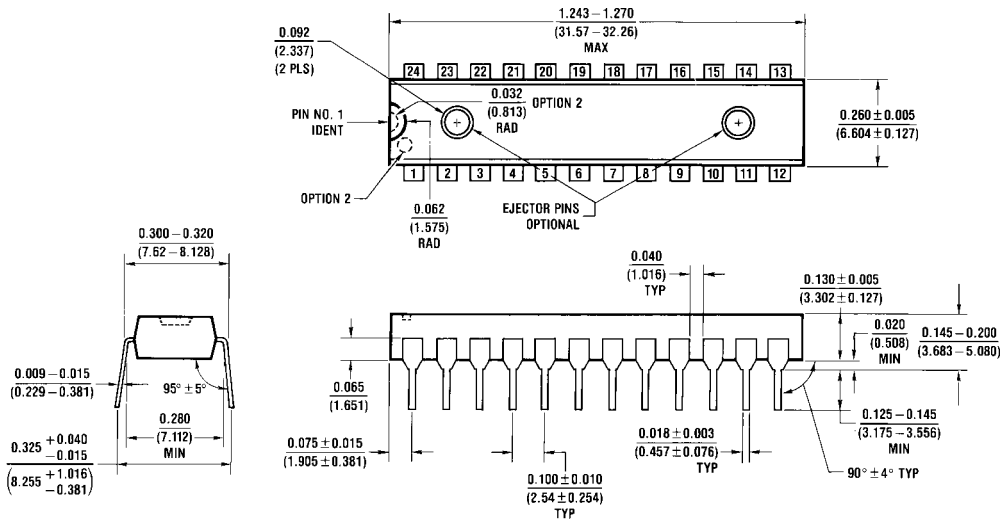
| AC Electrical Characteristics | | | | | | | |
|-------------------------------|--|---|-----|--|--|-------|-------|
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
| | | Min | Typ | Max | Min | Max | |
| t _{PLH} | Propagation Delay | 2.5 | | 8.0 | 2.0 | 9.0 | ns |
| t _{PHL} | D _n to O _n | 1.5 | | 6.5 | 1.5 | 7.0 | |
| t _{PLH} | Propagation Delay | 5.0 | | 12.0 | 4.5 | 13.5 | ns |
| t _{PHL} | LE to O _n | 2.0 | | 7.5 | 2.0 | 8.0 | |
| t _{PZH} | Output Enable Time | 2.5 | | 8.5 | 2.0 | 9.5 | ns |
| t _{PZL} | $\overline{\text{OE}}$ to O _n | 2.5 | | 9.0 | 2.0 | 10.0 | |
| t _{PHZ} | Output Disable Time | 1.0 | | 6.5 | 1.0 | 7.5 | |
| t _{PLZ} | $\overline{\text{OE}}$ to O _n | 1.0 | | 6.5 | 1.0 | 7.5 | |
| AC Operating Requirements | | | | | | | |
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V | | T _A = 0°C to +70°C V _{CC} = +5.0V | | Units | |
| | | Min | Max | Min | Max | | |
| t _S (H) | Setup Time, HIGH or LOW | 2.0 | | 2.5 | | ns | |
| t _S (L) | D _n to LE | 2.0 | | 2.5 | | | |
| t _H (H) | Hold Time, HIGH or LOW | 2.5 | | 3.0 | | ns | |
| t _H (L) | D _n to LE | 3.0 | | 3.5 | | | |
| t _W (H) | LE Pulse Width, HIGH | 4.0 | | 4.0 | | ns | |

Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N24C (REV F)

24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide Package Number N24C

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