National Semiconductor

April 1993

74FCT534
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

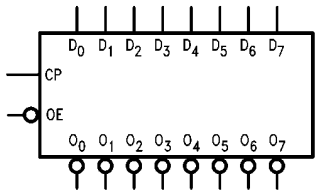
The 'FCT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance. The 'FCT534 is the same as the 'FCT374 except that the outputs are inverted.

Features

- I_{CC} and I_{OZ} reduced to 40.0 μA and $\pm$2.5 μA respectively
- NSC 54/74FCT534 is pin and functionally equivalent to IDT 54/74FCT534
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA
- CMOS power levels
- ESD immunity $\geq$ 4 kV typ

Logic Symbols



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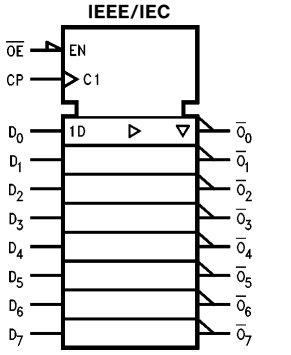

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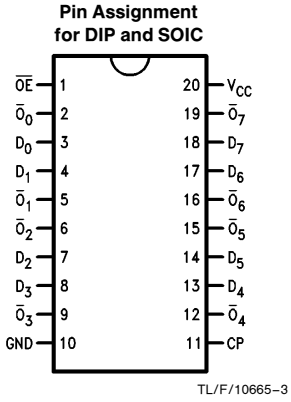
Connection Diagram



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Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs

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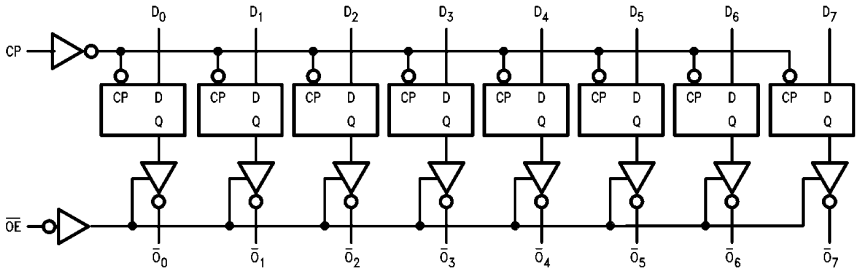
RRD-B30M105/Printed in U. S. A.

Functional Description

The 'FCT534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs			Output
CP	**OE**	**D**	$\overline{\mathbf{O}}$
⌐‾	L	H	L
⌐‾	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐‾ = LOW-to-HIGH Clock Transition
Z = High Impedance
$\overline{O}_0$ = Value stored from previous clock cycle

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
74FCT −0.5V to +7.0V

Temperature Under Bias (T_{BIAS})
74FCT −55°C to +125°C

Storage Temperature (T_{STG})
74FCT −55°C to +125°C

DC Output Current (I_{OUT}) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
74FCT 4.75V to 5.25V

Input Voltage 0V to V_{CC}

Output Voltage 0V to V_{CC}

Operating Temperature (T_A)
74FCT −0°C to +70°C

Junction Temperature (T_J)
PDIP 140°C

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	74FCTA			Units	Conditions	
		Min	Typ	Max			
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			2.5 2.5 −2.5 −2.5	μA	V_{CC} = Max	V_O = V_{CC} V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4	V_{CC} 4.3			V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA I_{OH} = −15 mA
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3	0.2 0.5		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		1.0	40.0	μA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.25	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_I = 5 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHz f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8			V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Numbers of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics

Symbol	Parameter	74FCT	74FCT		Units
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} =$ Com $C_L = 50$ pF		
		Typ	Min (Note 1)	Max	
t_{PLH} t_{PHL}	Propagation Delay C_P to $\overline{O}n$	6.5	1.5	10.0	ns
t_{PZH} t_{PZL}	Output Enable Time	9.0	1.5	12.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time	6.0	1.5	8.0	ns
t_s	Set Up Time High or Low Dn to CP	1.0	2.0		ns
t_h	Hold Time High or Low Dn to CP	0.5	1.5		ns
t_w	CP Pulse Width High or Low	4.0	7.0		ns

Note 1: Minimum limits guaranteed but not tested on propagation delays.

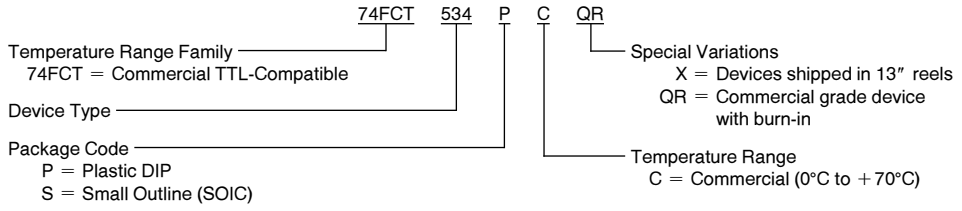
Capacitance $T_A = +25°C$, $f_I = 1.0$ MHz

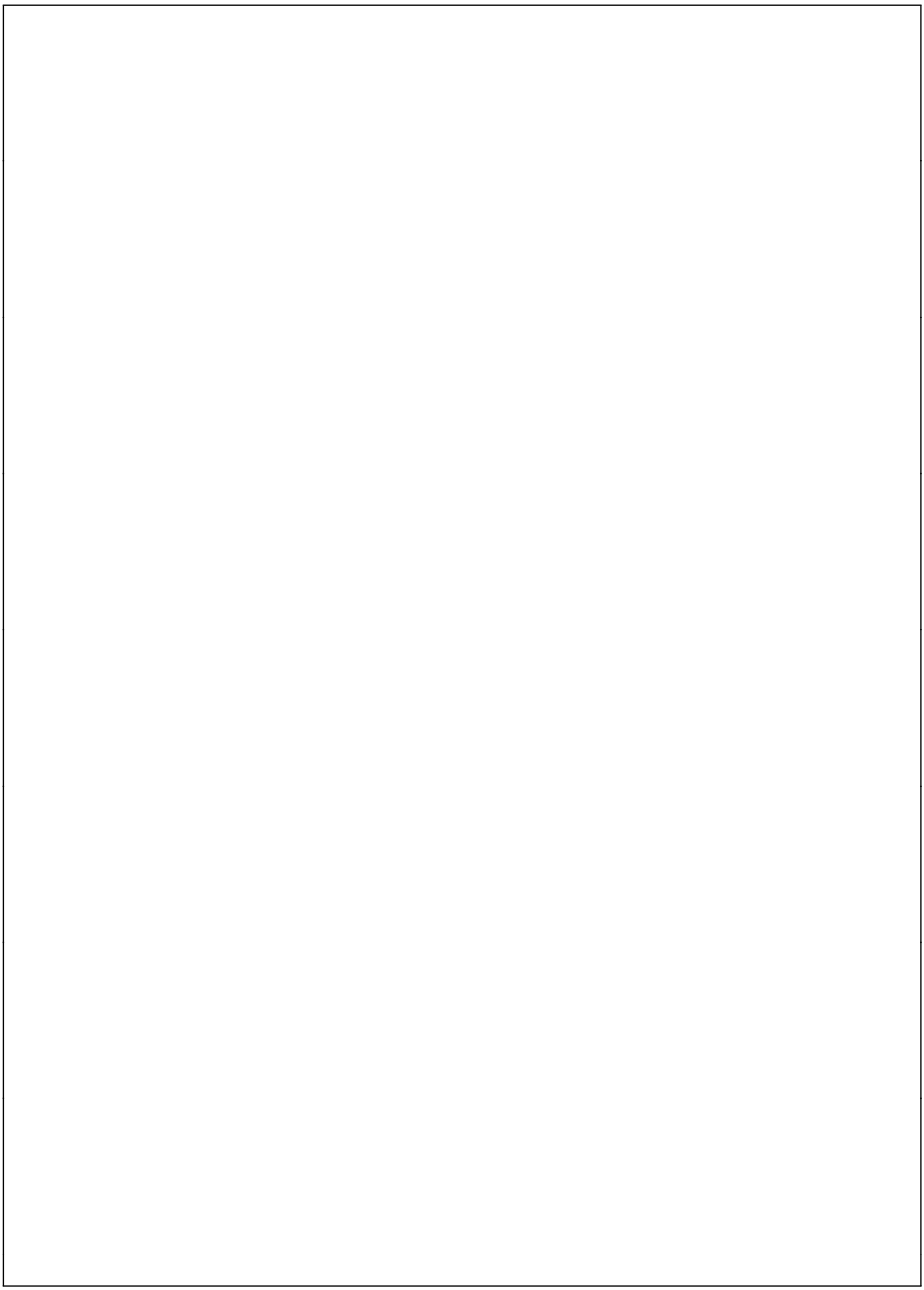
Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured at characterization but not tested.
C_{OUT} for 74FCT only.

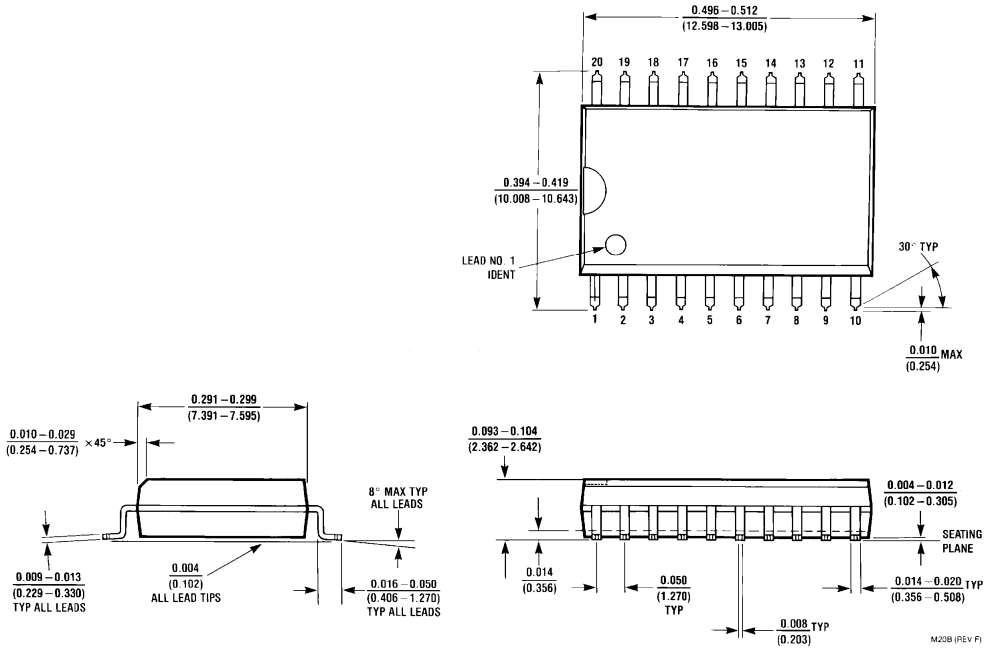
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



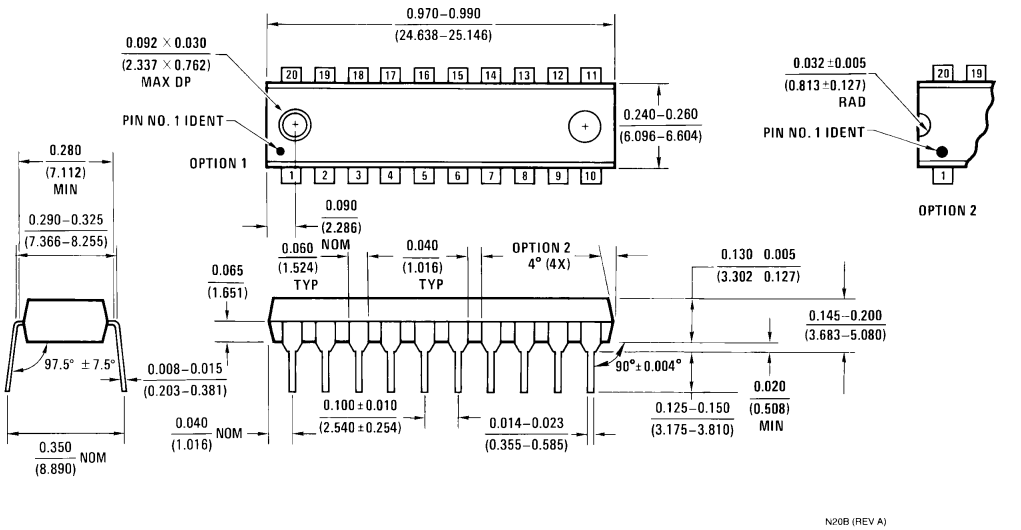


Physical Dimensions inches (millimeters)



20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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