DATA SHEET

74HC2G86; 74HCT2G86
Dual 2-input exclusive-OR gate

Product specification
Supersedes data of 2002 Jul 17

2003 Jul 28

Philips
Semiconductors

PHILIPS

Dual 2-input exclusive-OR gate 74HC2G86; 74HCT2G86

FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Very small 8 pins package
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.

DESCRIPTION

The 74HC2G/HCT2G86 is a high-speed Si-gate CMOS device.

The 74HC2G/HCT2G86 provides dual 2-input exclusive-OR gate.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 6.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC2G86	HCT2G86	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 50 pF; V_{CC} = 4.5 V	11	11	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	9	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total switching outputs;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. For 74HC2G86 the condition is V_I = GND to V_{CC}.
   For 74HCT2G86 the condition is V_I = GND to V_{CC} – 1.5 V.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nA	nY
L	L	L
L	H	H
H	L	H
H	H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC2G86DP	–40 to +125 °C	8	TSSOP8	plastic	SOT505-2	H86
74HCT2G86DP	–40 to +125 °C	8	TSSOP8	plastic	SOT505-2	T86
74HC2G86DC	–40 to +125 °C	8	VSSOP8	plastic	SOT765-1	H86
74HCT2G86DC	–40 to +125 °C	8	VSSOP8	plastic	SOT765-1	H86

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input 1A
2	1B	data input 1B
3	2Y	data output 2Y
4	GND	ground (0 V)
5	2A	data input 2A
6	2B	data input 2B
7	1Y	data output 1Y
8	V_{CC}	supply voltage

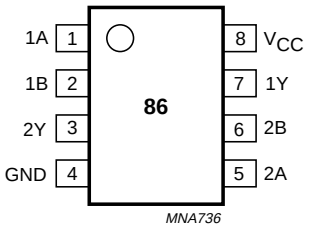


Fig.1 Pin configuration.

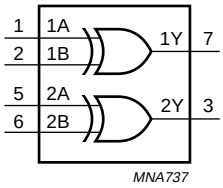


Fig.2 Logic symbol.

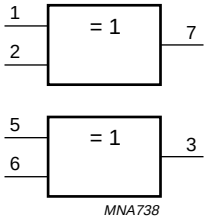


Fig.3 IEC logic symbol.

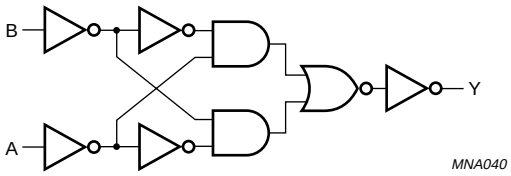


Fig.4 Logic diagram (one driver).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC2G86			74HCT2G86			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	–	1000	–	–	–	ns
		V_{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V_{CC} = 6.0 V	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_O	output source or sink current	$–0.5 \text{ V} < V_O < V_{CC} + 0.5$ V; note 1	–	25	mA
I_{CC}	V_{CC} or GND current	note 1	–	50	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 110 °C the value of P_D derates linearly with 8 mW/K.

DC CHARACTERISTICS

Type 74HC2G86

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V_{IL}	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	2.0	1.9	2.0	–	V
		I_O = –20 μA	4.5	4.4	4.5	–	V
		I_O = –20 μA	6.0	5.9	6.0	–	V
		I_O = –4.0 mA	4.5	4.18	4.32	–	V
		I_O = –5.2 mA	6.0	5.68	5.81	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	2.0	–	0	0.1	V
		I_O = 20 μA	4.5	–	0	0.1	V
		I_O = 20 μA	6.0	–	0	0.1	V
		I_O = 4.0 mA	4.5	–	0.15	0.26	V
		I_O = 5.2 mA	6.0	–	0.16	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	–	±0.1	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	6.0	–	–	1.0	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	2.0	1.9	–	–	V
		I_O = –20 μA	4.5	4.4	–	–	V
		I_O = –20 μA	6.0	5.9	–	–	V
		I_O = –4.0 mA	4.5	4.13	–	–	V
		I_O = –5.2 mA	6.0	5.63	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	2.0	–	–	0.1	V
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 20 μA	6.0	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.33	V
		I_O = 5.2 mA	6.0	–	–	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	–	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	6.0	–	–	10	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	2.0	1.9	–	–	V
		I_O = –20 μA	4.5	4.4	–	–	V
		I_O = –20 μA	6.0	5.9	–	–	V
		I_O = –4.0 mA	4.5	3.7	–	–	V
		I_O = –5.2 mA	6.0	5.2	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	2.0	–	–	0.1	V
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 20 μA	6.0	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.4	V
		I_O = 5.2 mA	6.0	–	–	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	–	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	6.0	–	–	20	μA

Type 74HCT2G86

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	4.5	4.4	4.5	–	V
		I_O = –4.0 mA	4.5	4.18	4.32	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	4.5	–	0	0.1	V
		I_O = 4.0 mA	4.5	–	0.15	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±0.1	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	1.0	μA
ΔI_{CC}	additional supply current per input	V_I = V_{CC} – 2.1 V; I_O = 0	4.5 to 5.5	–	–	300	μA
T_{amb} = –40 to +85 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	4.5	4.4	–	–	V
		I_O = –4.0 mA	4.5	4.13	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	10	μA
ΔI_{CC}	additional supply current per input	V_I = V_{CC} – 2.1 V; I_O = 0	4.5 to 5.5	–	–	375	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	4.5	4.4	–	–	V
		I_O = –4.0 mA	4.5	3.7	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	20	μA
ΔI_{CC}	additional supply current per input	V_I = V_{CC} – 2.1 V; I_O = 0	4.5 to 5.5	–	–	410	μA

AC CHARACTERISTICS

Type 74HC2G86

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

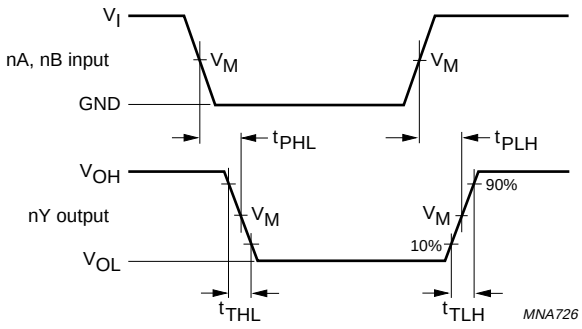
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = 25 °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 5 and 6	2.0	–	34	120	ns
			4.5	–	11	20	ns
			6.0	–	9	17	ns
t_{THL}/t_{TLH}	output transition time	see Figs 5 and 6	2.0	–	18	75	ns
			4.5	–	6	15	ns
			6.0	–	5	13	ns
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 5 and 6	2.0	–	–	150	ns
			4.5	–	–	25	ns
			6.0	–	–	21	ns
t_{THL}/t_{TLH}	output transition time	see Figs 5 and 6	2.0	–	–	95	ns
			4.5	–	–	19	ns
			6.0	–	–	16	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 5 and 6	2.0	–	–	180	ns
			4.5	–	–	36	ns
			6.0	–	–	30	ns
t_{THL}/t_{TLH}	output transition time	see Figs 5 and 6	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	20	ns

Type 74HCT2G86

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

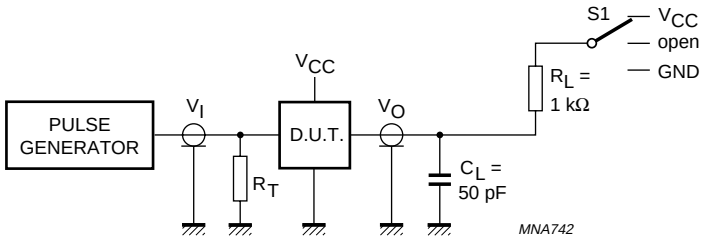
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = 25 °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 5 and 6	4.5	–	11	19	ns
t_{THL}/t_{TLH}	output transition time	see Figs 5 and 6	4.5	–	6	15	ns
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 5 and 6	4.5	–	–	23	ns
t_{THL}/t_{TLH}	output transition time	see Figs 5 and 6	4.5	–	–	19	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 5 and 6	4.5	–	–	48	ns
t_{THL}/t_{TLH}	output transition time	see Figs 5 and 6	4.5	–	–	22	ns

AC WAVEFORMS



For HC2G: V_M = 50%; V_I = GND to V_{CC}.
For HCT2G: V_M = 1.3 V; V_I = GND to 3.0 V.

Fig.5 The input (nA, nB) to output (nY) propagation delays.



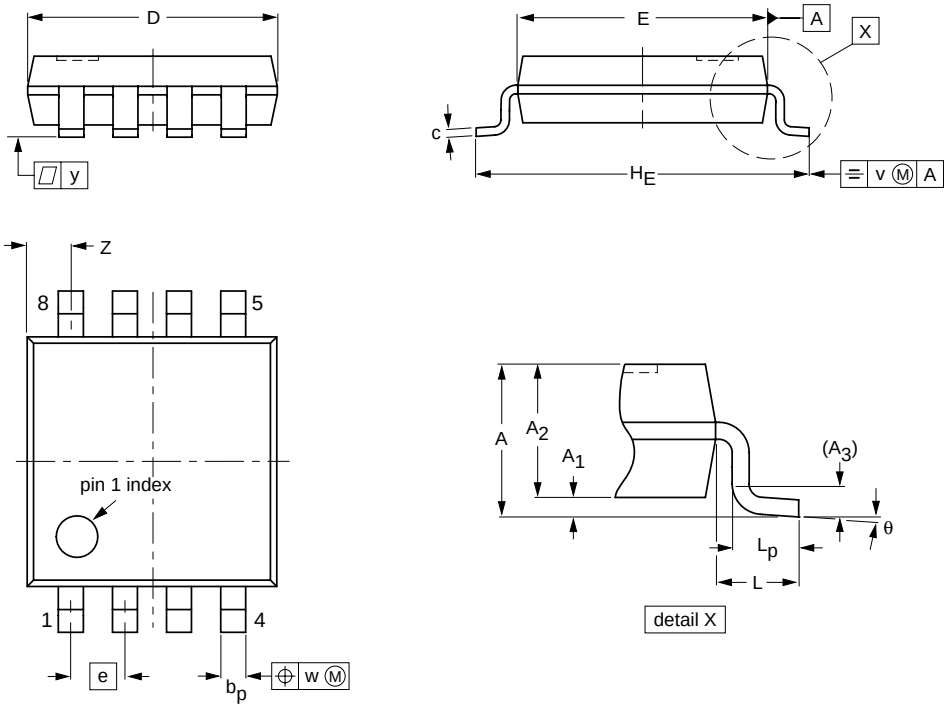
TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.6 Load circuitry for switching times.

PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

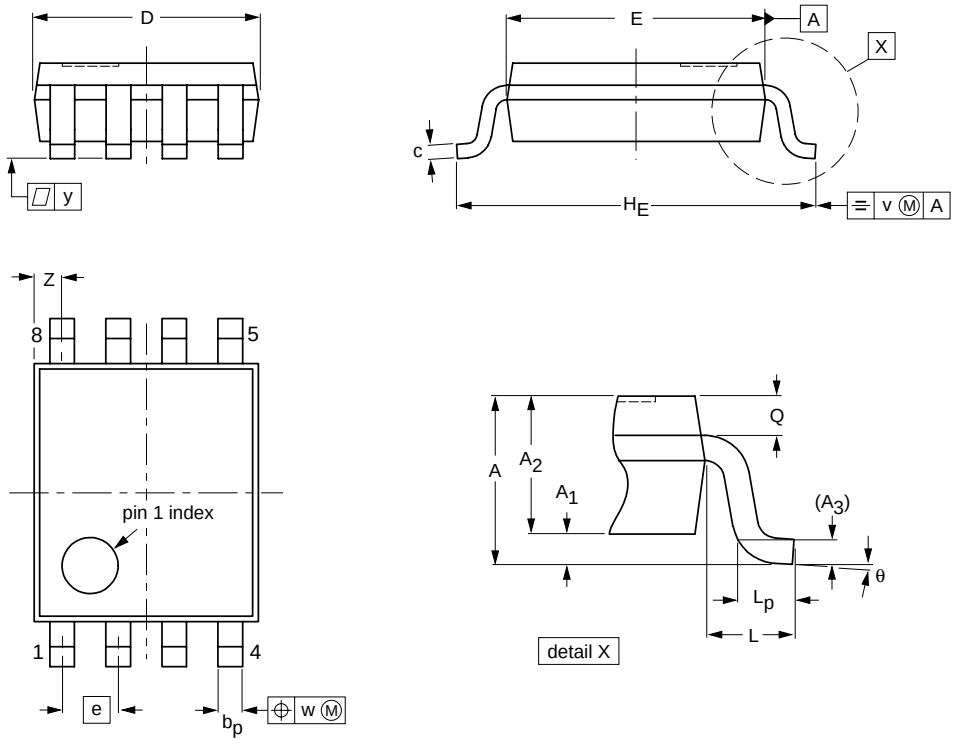
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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