

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT4518**

### **Dual synchronous BCD counter**

Product specification  
File under Integrated Circuits, IC06

December 1990

## Dual synchronous BCD counter

## 74HC/HCT4518

## FEATURES

- Output capability: standard
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT4518 are high-speed Si-gate CMOS devices and are pin compatible with the "4518" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4518 are dual 4-bit internally synchronous BCD counters with an active HIGH clock input ( $nCP_0$ ) and an active LOW clock input ( $n\overline{CP}_1$ ), buffered outputs from

all four bit positions ( $nQ_0$  to  $nQ_3$ ) and an active HIGH overriding asynchronous master reset input ( $nMR$ ).

The counter advances on either the LOW-to-HIGH transition of  $nCP_0$  if  $n\overline{CP}_1$  is HIGH or the HIGH-to-LOW transition of  $n\overline{CP}_1$  if  $nCP_0$  is LOW. Either  $nCP_0$  or  $n\overline{CP}_1$  may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on  $nMR$  resets the counter ( $nQ_0$  to  $nQ_3 = \text{LOW}$ ) independent of  $nCP_0$  and  $n\overline{CP}_1$ .

## APPLICATIONS

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $nCP_0$ , $n\overline{CP}_1$ to $nQ_n$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	20	24	ns
$t_{PHL}$	propagation delay $nMR$ to $nQ_n$		13	14	ns
$f_{max}$	maximum clock frequency		61	55	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per counter	notes 1 and 2	29	27	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

## ORDERING INFORMATION

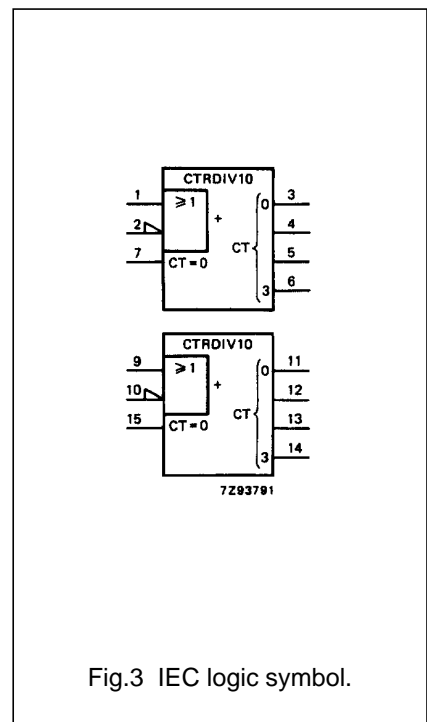
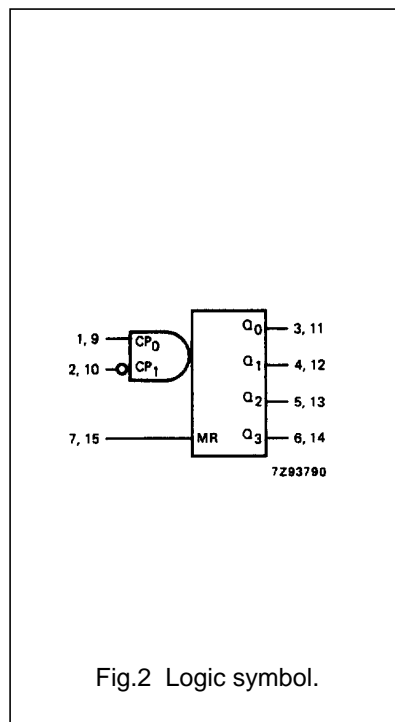
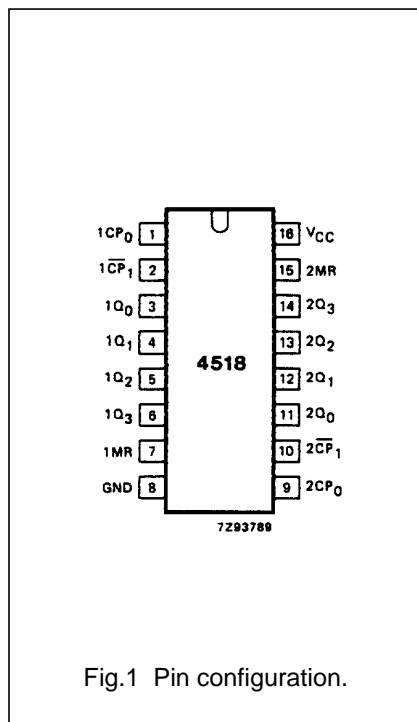
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# Dual synchronous BCD counter

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1CP <sub>0</sub> , 2CP <sub>0</sub>	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	1CP <sub>1</sub> , 2CP <sub>1</sub>	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	1Q <sub>0</sub> to 1Q <sub>3</sub>	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	2Q <sub>0</sub> to 2Q <sub>3</sub>	data outputs
16	V <sub>CC</sub>	positive supply voltage



# Dual synchronous BCD counter

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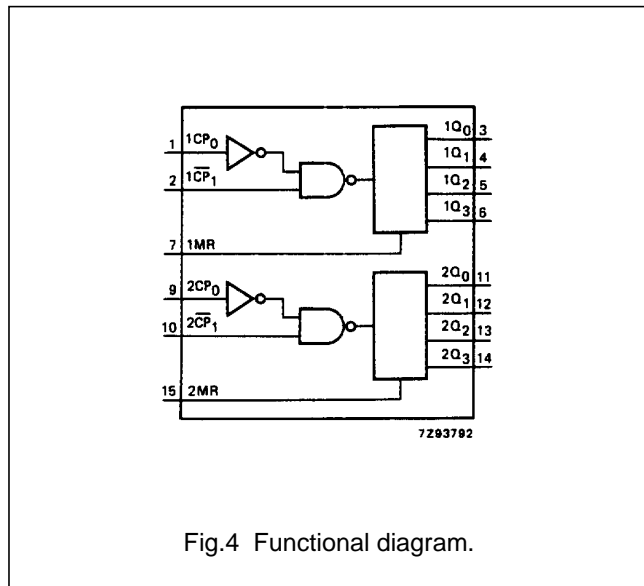


Fig.4 Functional diagram.

### FUNCTION TABLE

nCP <sub>0</sub>	nCP <sub>1</sub>	MR	MODE
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	Q <sub>0</sub> to Q <sub>3</sub> = LOW

### Notes

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
↑ = LOW-to-HIGH clock transition  
↓ = HIGH-to-LOW clock transition

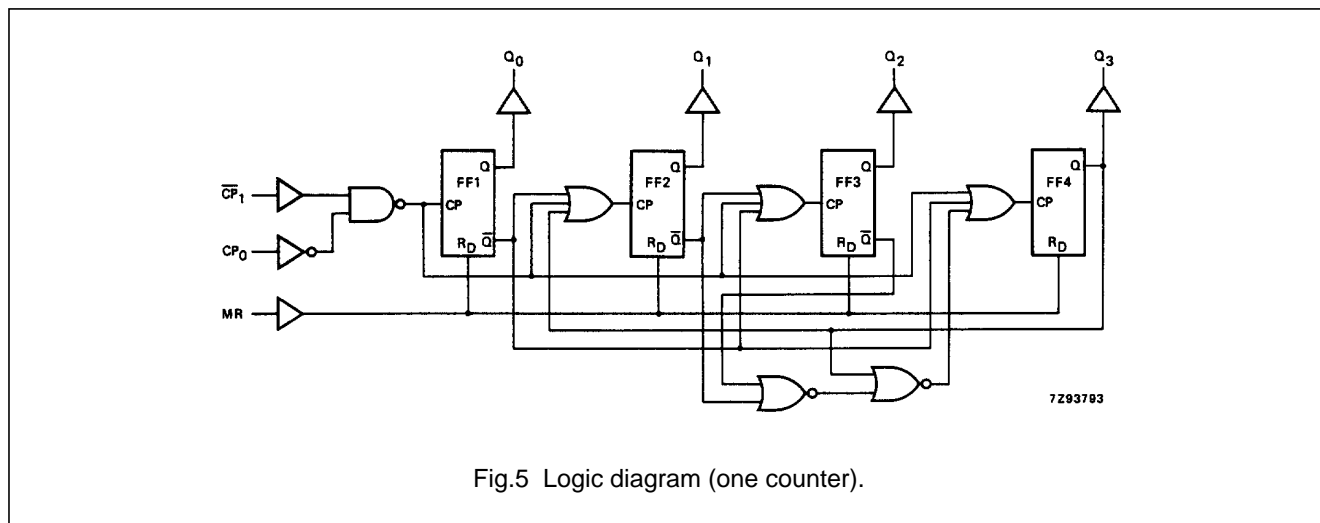


Fig.5 Logic diagram (one counter).

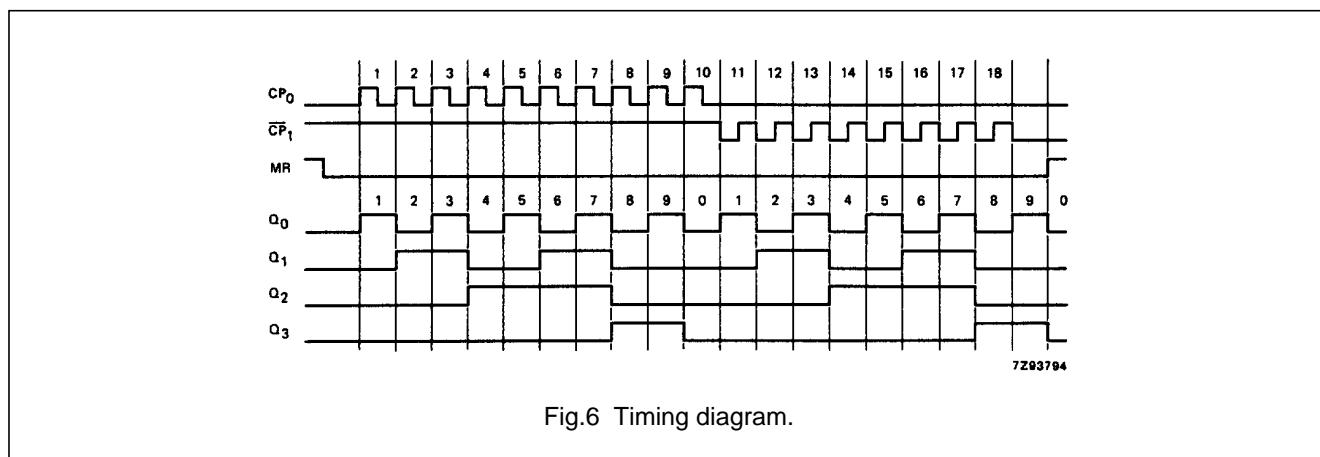


Fig.6 Timing diagram.

## Dual synchronous BCD counter

## 74HC/HCT4518

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> , nCP <sub>1</sub> to nQ <sub>n</sub>		66 24 19	210 42 36		265 53 45		315 63 59	ns	2.0 4.5 6.0	Fig.9
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.9
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>w</sub>	master reset pulse width HIGH	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig.8
t <sub>rem</sub>	removal time nMR to nCP <sub>0</sub> , nCP <sub>1</sub>	0 0 0	-22 -8 -6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.8
t <sub>su</sub>	set-up time nCP <sub>1</sub> to nCP <sub>0</sub> ; nCP <sub>0</sub> to nCP <sub>1</sub>	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
f <sub>max</sub>	maximum clock pulse frequency nCP <sub>0</sub> , nCP <sub>1</sub>	6.0 30 35	18 55 66		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.8

## Dual synchronous BCD counter

## 74HC/HCT4518

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$nCP_0, n\overline{CP}_1$	0.80
nMR	1.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)							UNIT	TEST CONDITIONS	
		74HCT								$V_{CC}$ (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL}/t_{PLH}$	propagation delay $nCP_0, n\overline{CP}_1$ to $nQ_n$		28	53		66		80	ns	4.5	Fig.9
$t_{PHL}$	propagation delay nMR to $nQ_n$		17	35		44		53	ns	4.5	Fig.8
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig.9
$t_W$	clock pulse width HIGH or LOW	20	11		25		30		ns	4.5	Fig.8
$t_W$	master reset pulse width HIGH	20	11		25		30		ns	4.5	Fig.8
$t_{rem}$	removal time nMR to $nCP_0, n\overline{CP}_1$	0	-11		0		0		ns	4.5	Fig.8
$t_{su}$	set-up time $n\overline{CP}_1$ to $nCP_0$ ; $nCP_0$ to $n\overline{CP}_1$	16	5		20		24		ns	4.5	Fig.7
$f_{max}$	maximum clock pulse frequency $nCP_0, n\overline{CP}_1$	25	50		20		17		MHz	4.5	Fig.8

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## AC WAVEFORMS

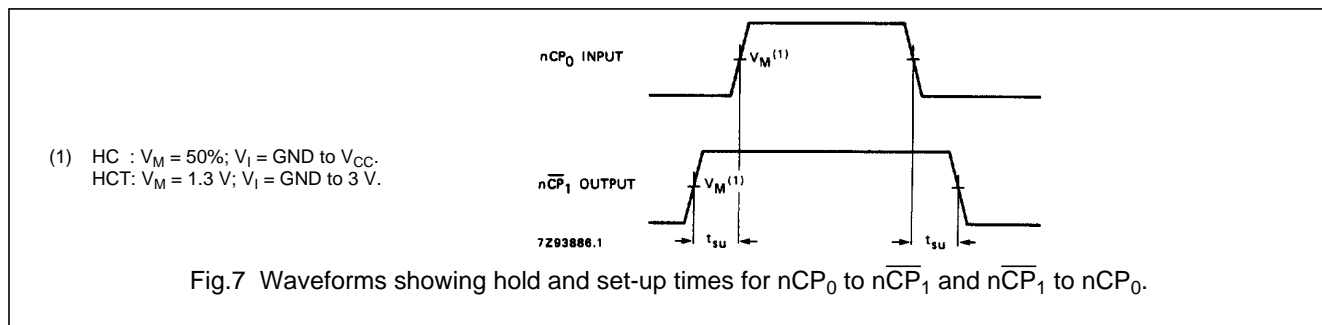


Fig.7 Waveforms showing hold and set-up times for  $n\overline{CP}_0$  to  $n\overline{CP}_1$  and  $n\overline{CP}_1$  to  $n\overline{CP}_0$ .

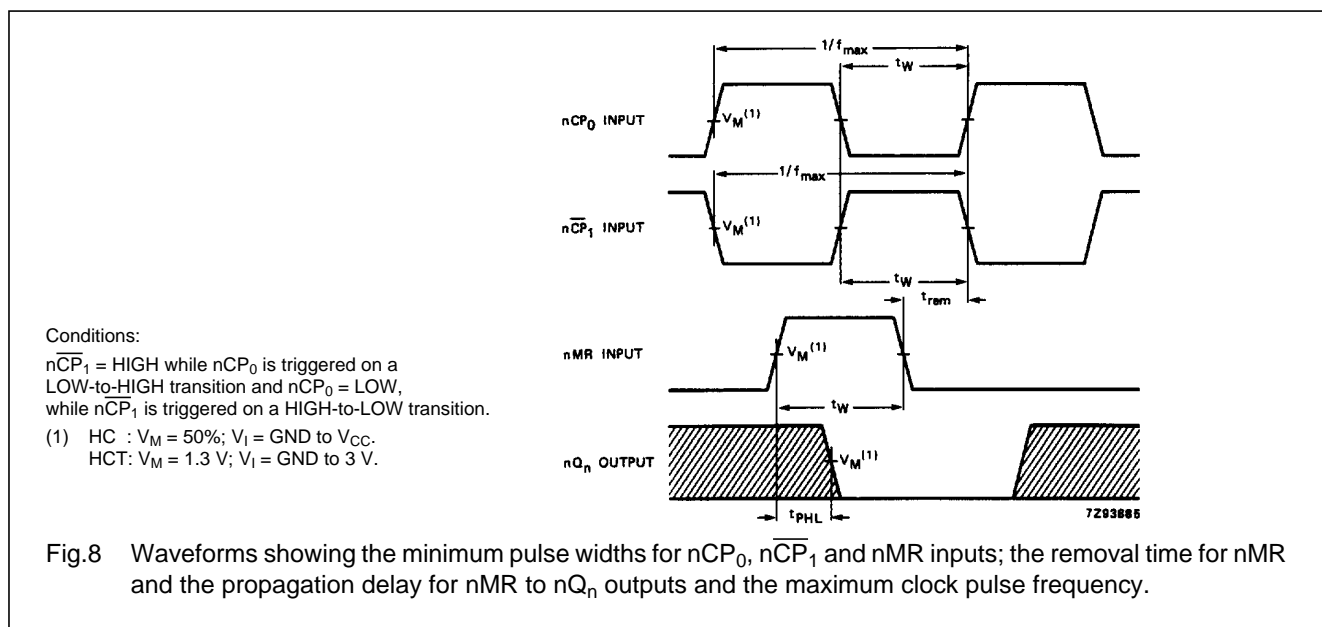


Fig.8 Waveforms showing the minimum pulse widths for  $n\overline{CP}_0$ ,  $n\overline{CP}_1$  and  $n\overline{MR}$  inputs; the removal time for  $n\overline{MR}$  and the propagation delay for  $n\overline{MR}$  to  $nQ_n$  outputs and the maximum clock pulse frequency.

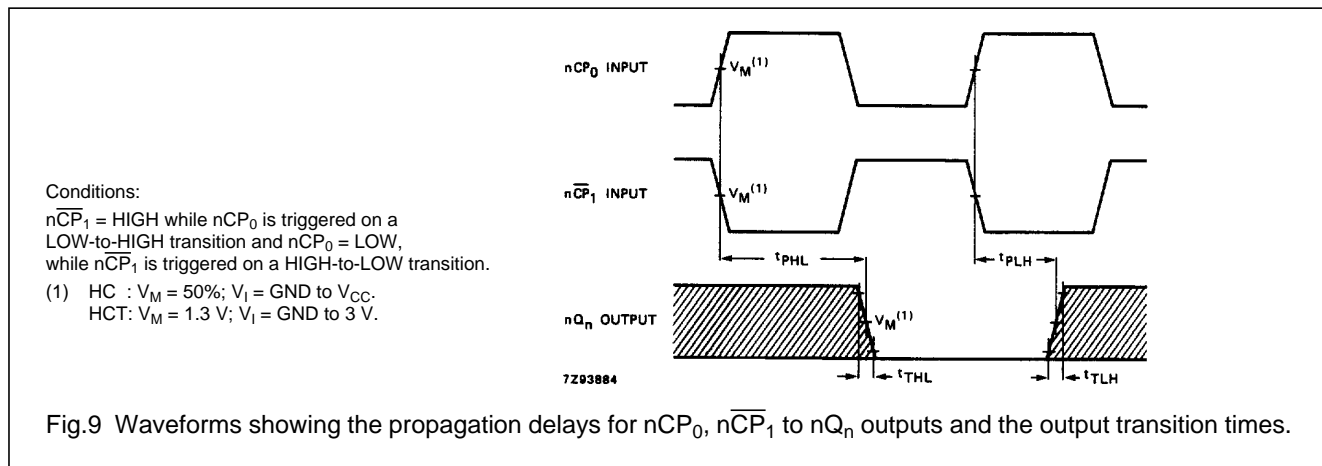


Fig.9 Waveforms showing the propagation delays for  $n\overline{CP}_0$ ,  $n\overline{CP}_1$  to  $nQ_n$  outputs and the output transition times.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".