

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT181 4-bit arithmetic logic unit

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC06

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4-bit arithmetic logic unit

74HC/HCT181

FEATURES

- Full carry look-ahead for high-speed arithmetic operation on long words
- Provides 16 arithmetic operations: add, subtract, compare, double, plus 12 others
- Provides all 16 logic operations of two variables: EXCLUSIVE-OR, compare, AND, NAND, NOR, OR plus 10 other logic operations
- Output capability: standard, A=B open drain
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT181 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT181 are 4-bit high-speed parallel Arithmetic Logic Units (ALU). Controlled by the four function select inputs (S₀ to S₃) and the mode control input (M), they can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands (see function table).

When the mode control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When M is LOW, the carries are enabled and the "181" performs arithmetic operations on the two 4-bit words. The "181" incorporates full internal carry look-ahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the carry propagation (\bar{P}) and carry generate (\bar{G}) signals. \bar{P} and \bar{G} are not affected by carry in.

When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the carry output (C_{n+4}) signal to the carry input (C_n) of the next unit.

For high-speed operation the device is used in conjunction with the "182" carry look-ahead circuit. One carry look-ahead package is required for each group of four "181" devices. Carry look-ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The comparator output (A=B) of the device goes HIGH when all four function outputs (\bar{F}_0 to \bar{F}_3) are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. A=B is an open collector output and can be wired-AND with other A=B outputs to give a comparison for more than 4 bits. The open drain output A=B should be used with an external pull-up resistor in order to establish a logic HIGH level. The A=B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The function table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no under-flow and no carry is generated when there is underflow.

As indicated, the "181" can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs.

For either case the table lists the operations that are performed to the operands.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|--------------------------|---------|--|----------|
| | NAME | DESCRIPTION | VERSION |
| 74HC181N3; 74HCT181N3 | DIP24 | plastic dual in-line package; 24 leads (300 mil) | SOT222-1 |
| 74HC181N; 74HCT181N | DIP24 | plastic dual in-line package; 24 leads (600 mil) | SOT101-1 |
| 74HC181D; 74HCT181D | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |

4-bit arithmetic logic unit

74HC/HCT181

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|--|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay A _n or B _n to A=B C _n to C _{n+4} | C _L = 15 pF; V _{CC} = 5 V | 28 | 30 | ns |
| | | | 17 | 21 | ns |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per L package | notes 1 and 2 | 90 | 92 | pF |

Notes

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

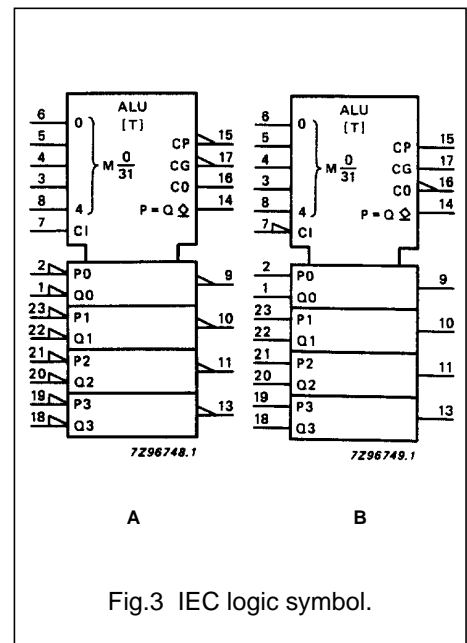
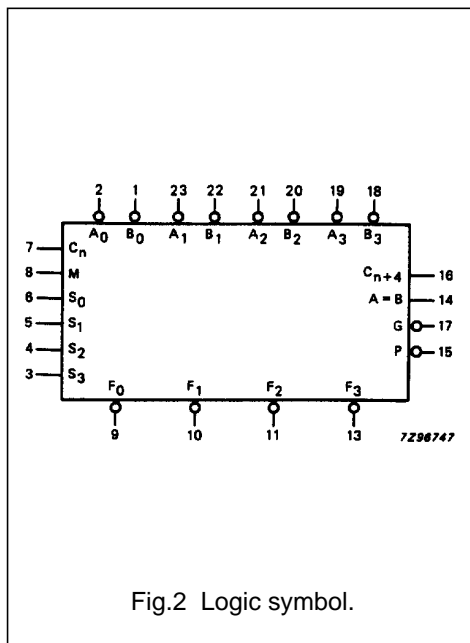
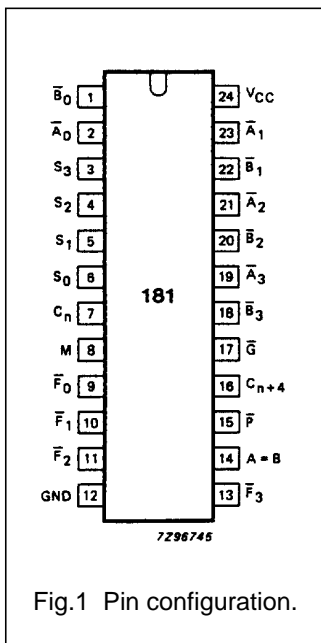
f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

- For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V



4-bit arithmetic logic unit

74HC/HCT181

PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---------------|--------------------------------------|-------------------------------------|
| 1, 22, 20, 18 | \overline{B}_0 to \overline{B}_3 | operand inputs (active LOW) |
| 2, 23, 21, 19 | \overline{A}_0 to \overline{A}_3 | operand inputs (active LOW) |
| 6, 5, 4, 3 | S_0 to S_3 | select inputs |
| 7 | C_n | carry input |
| 8 | M | mode control input |
| 9, 10, 11, 13 | \overline{F}_0 to \overline{F}_3 | function outputs (active LOW) |
| 12 | GND | ground (0 V) |
| 14 | A=B | comparator output |
| 15 | \overline{P} | carry propagate output (active LOW) |
| 16 | C_{n+4} | carry output |
| 17 | \overline{G} | carry generate output (active LOW) |
| 24 | V_{CC} | positive supply voltage |

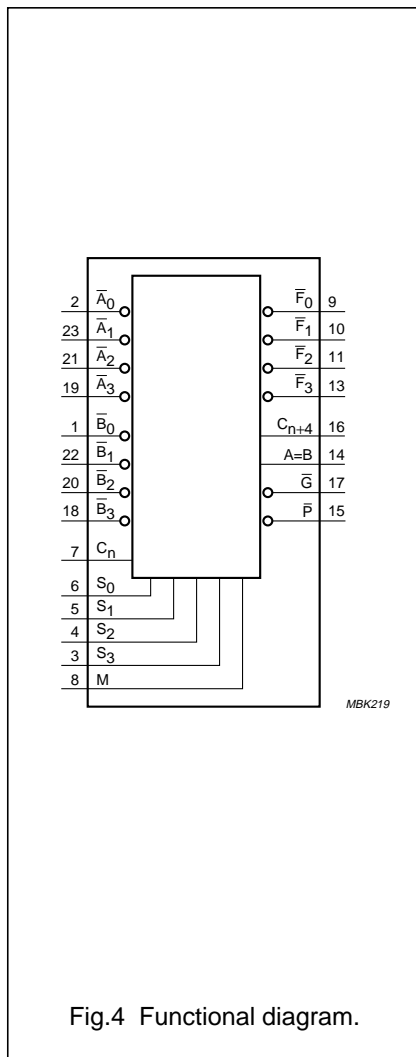


Fig.4 Functional diagram.

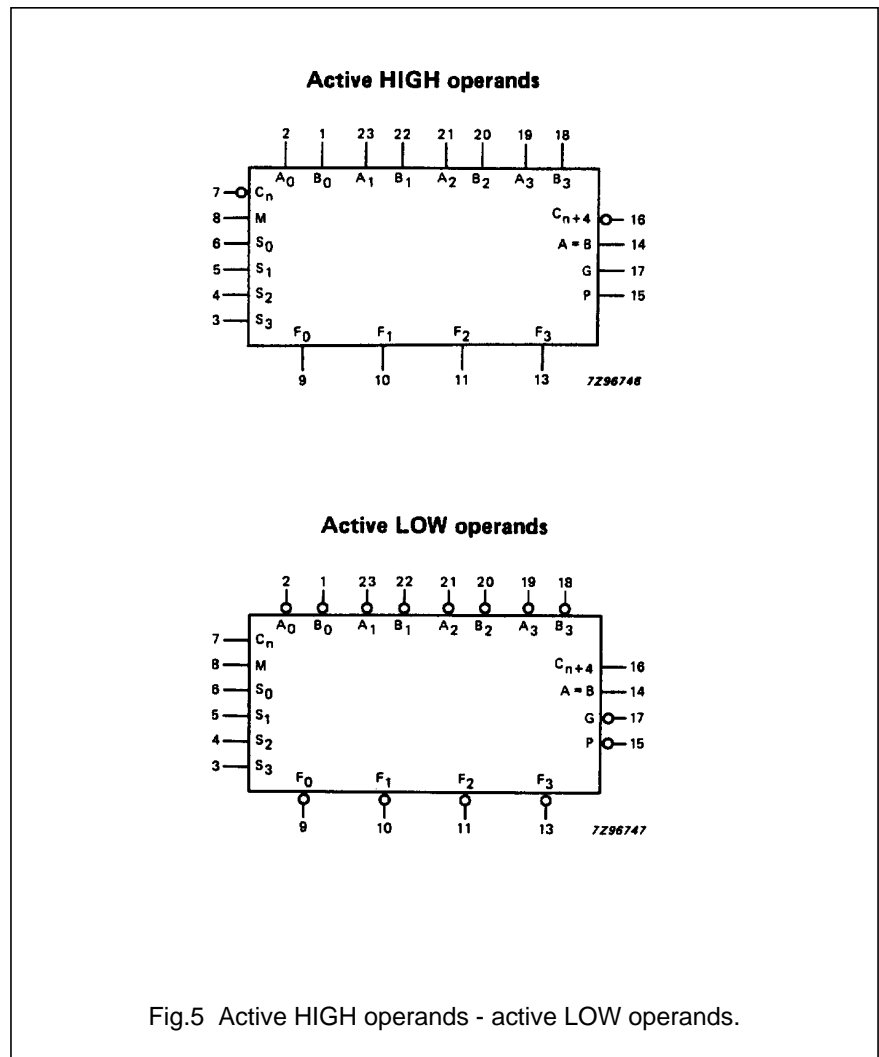


Fig.5 Active HIGH operands - active LOW operands.

4-bit arithmetic logic unit

74HC/HCT181

FUNCTION TABLES

| MODE SELECT INPUTS | | | | ACTIVE HIGH INPUTS AND OUTPUTS | |
|--------------------|----------------|----------------|----------------|--------------------------------|--|
| S ₃ | S ₂ | S ₁ | S ₀ | LOGIC (M=H) | ARITHMETIC ⁽²⁾ (M=L; C _n =H) |
| L | L | L | L | \overline{A} | A |
| L | L | L | H | $\overline{A + B}$ | A + B |
| L | L | H | L | \overline{AB} | A + \overline{B} |
| L | L | H | H | logical 0 | minus 1 |
| L | H | L | L | \overline{AB} | A plus \overline{AB} |
| L | H | L | H | \overline{B} | (A + B) plus \overline{AB} |
| L | H | H | L | $A \oplus B$ | A minus B minus 1 |
| L | H | H | H | \overline{AB} | \overline{AB} minus 1 |
| H | L | L | L | $\overline{A + B}$ | A plus AB |
| H | L | L | H | $\overline{A \oplus B}$ | A plus B |
| H | L | H | L | B | (A + \overline{B}) plus AB |
| H | L | H | H | AB | AB minus 1 |
| H | H | L | L | logical 1 | A plus A ⁽¹⁾ |
| H | H | L | H | $A + \overline{B}$ | (A + B) plus A |
| H | H | H | L | A + B | (A + \overline{B}) plus A |
| H | H | H | H | A | A minus 1 |

Notes to the function tables

1. Each bit is shifted to the next more significant position.
2. Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level
L = LOW voltage level

| MODE SELECT INPUTS | | | | ACTIVE LOW INPUTS AND OUTPUTS | |
|--------------------|----------------|----------------|----------------|-------------------------------|--|
| S ₃ | S ₂ | S ₁ | S ₀ | LOGIC (M=H) | ARITHMETIC ⁽²⁾ (M=L; C _n =L) |
| L | L | L | L | \overline{A} | A minus 1 |
| L | L | L | H | \overline{AB} | AB minus 1 |
| L | L | H | L | $\overline{A + B}$ | \overline{AB} minus 1 |
| L | L | H | H | logical 1 | minus 1 |
| L | H | L | L | $\overline{A + B}$ | A plus (A + \overline{B}) |
| L | H | L | H | \overline{B} | AB plus (A + \overline{B}) |
| L | H | H | L | $\overline{A \oplus B}$ | A minus B minus 1 |
| L | H | H | H | $A + \overline{B}$ | A + \overline{B} |
| H | L | L | L | \overline{AB} | A plus (A + B) |
| H | L | L | H | $A \oplus B$ | A plus B |
| H | L | H | L | B | \overline{AB} plus (A + B) |
| H | L | H | H | A + B | A + B |
| H | H | L | L | logical 0 | A plus A ⁽¹⁾ |
| H | H | L | H | \overline{AB} | AB plus A |
| H | H | H | L | AB | \overline{AB} plus A |
| H | H | H | H | A | A |

Notes to the function tables

1. Each bit is shifted to the next more significant position.
2. Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level
L = LOW voltage level

4-bit arithmetic logic unit

74HC/HCT181

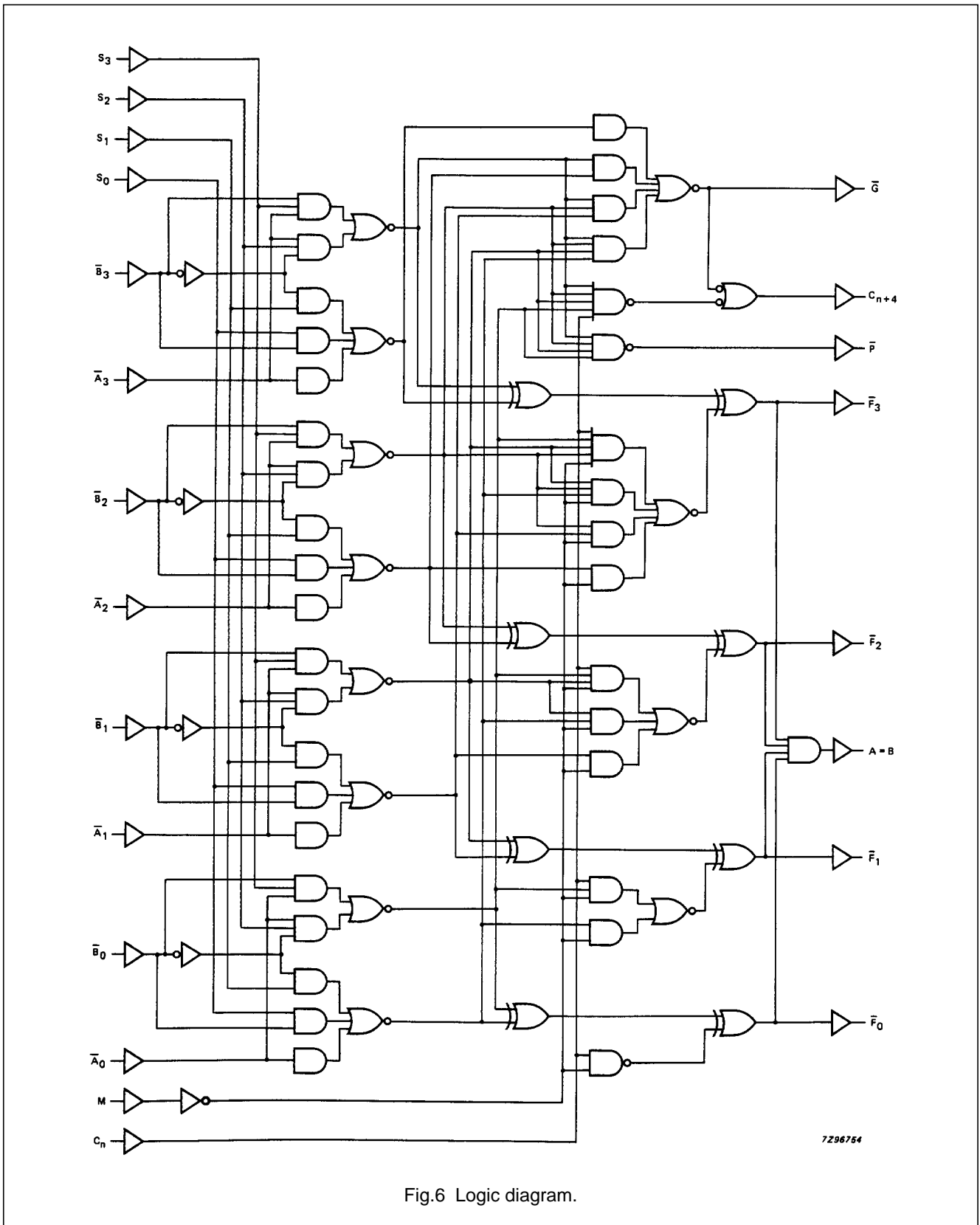


Fig.6 Logic diagram.

4-bit arithmetic logic unit

74HC/HCT181

Table 1 SUM MODE TESTFunction inputs $S_0 = S_3 = 4.5\text{ V}$, $M = S_1 = S_2 = 0\text{ V}$

| PARAMETER | INPUT UNDER TEST | OTHER INPUT, SAME BIT | | OTHER DATA INPUTS | | OUTPUT UNDER TEST |
|-------------------|------------------|-----------------------|-------------|-----------------------------------|---|----------------------------|
| | | Apply 4.5 V | Apply GND | Apply 4.5 V | Apply GND | |
| t_{PLH}/t_{PHL} | \bar{A}_i | \bar{B}_i | none | remaining \bar{A} and \bar{B} | C_n | \bar{F}_i |
| t_{PLH}/t_{PHL} | \bar{B}_i | \bar{A}_i | none | remaining \bar{A} and \bar{B} | C_n | \bar{F}_i |
| t_{PLH}/t_{PHL} | \bar{A}_i | \bar{B}_i | none | none | remaining \bar{A} and \bar{B} , C_n | \bar{P} |
| t_{PLH}/t_{PHL} | \bar{B}_i | \bar{A}_i | none | none | remaining \bar{A} and \bar{B} , C_n | \bar{P} |
| t_{PLH}/t_{PHL} | \bar{A}_i | none | \bar{B}_i | remaining \bar{B} | remaining \bar{A} , C_n | \bar{G} |
| t_{PLH}/t_{PHL} | \bar{B}_i | none | \bar{A}_i | remaining \bar{B} | remaining \bar{A} , C_n | \bar{G} |
| t_{PLH}/t_{PHL} | \bar{A}_i | none | \bar{B}_i | remaining \bar{B} | remaining \bar{A} , C_n | C_{n+4} |
| t_{PLH}/t_{PHL} | \bar{B}_i | none | \bar{A}_i | remaining \bar{B} | remaining \bar{A} , C_n | C_{n+4} |
| t_{PLH}/t_{PHL} | C_n | none | none | all \bar{A} | all \bar{B} | any \bar{F} or C_{n+4} |

Table 2 DIFFERENTIAL MODE TESTFunction inputs $S_1 = S_2 = 4.5\text{ V}$, $M = S_0 = S_3 = 0\text{ V}$

| PARAMETER | INPUT UNDER TEST | OTHER INPUT, SAME BIT | | OTHER DATA INPUTS | | OUTPUT UNDER TEST |
|-------------------|------------------|-----------------------|-------------|-----------------------------|---|----------------------------|
| | | Apply 4.5 V | Apply GND | Apply 4.5 V | Apply GND | |
| t_{PLH}/t_{PHL} | \bar{A}_i | none | \bar{B}_i | remaining \bar{A} | remaining \bar{B} , C_n | \bar{F}_i |
| t_{PLH}/t_{PHL} | \bar{B}_i | \bar{A}_i | none | remaining \bar{A} | remaining \bar{B} , C_n | \bar{F}_i |
| t_{PLH}/t_{PHL} | \bar{A}_i | none | \bar{B}_i | none | remaining \bar{A} and \bar{B} , C_n | \bar{P} |
| t_{PLH}/t_{PHL} | \bar{B}_i | \bar{A}_i | none | none | remaining \bar{A} and \bar{B} , C_n | \bar{P} |
| t_{PLH}/t_{PHL} | \bar{A}_i | \bar{B}_i | none | none | remaining \bar{A} and \bar{B} , C_n | \bar{G} |
| t_{PLH}/t_{PHL} | \bar{B}_i | none | \bar{A}_i | none | remaining \bar{A} and \bar{B} , C_n | \bar{G} |
| t_{PLZ}/t_{PZL} | \bar{A}_i | none | \bar{B}_i | remaining \bar{A} | remaining \bar{B} , C_n | A=B |
| t_{PLZ}/t_{PZL} | \bar{B}_i | \bar{A}_i | none | remaining \bar{A} | remaining \bar{B} , C_n | A=B |
| t_{PLH}/t_{PHL} | \bar{A}_i | \bar{B}_i | none | none | remaining \bar{A} and \bar{B} , C_n | C_{n+4} |
| t_{PLH}/t_{PHL} | \bar{B}_i | none | \bar{A}_i | none | remaining \bar{A} and \bar{B} , C_n | C_{n+4} |
| t_{PLH}/t_{PHL} | C_n | none | none | all \bar{A} and \bar{B} | none | any \bar{F} or C_{n+4} |

Table 3 LOGIC MODE TESTFunction inputs $M = S_1 = S_2 = 4.5\text{ V}$, $S_0 = S_3 = 0\text{ V}$

| PARAMETER | INPUT UNDER TEST | OTHER INPUT, SAME BIT | | OTHER DATA INPUTS | | OUTPUT UNDER TEST |
|-------------------|------------------|-----------------------|-----------|-------------------|---|-------------------|
| | | Apply 4.5 V | Apply GND | Apply 4.5 V | Apply GND | |
| t_{PLH}/t_{PHL} | \bar{A}_i | \bar{B}_i | none | none | remaining \bar{A} and \bar{B} , C_n | \bar{F}_i |
| t_{PLH}/t_{PHL} | \bar{B}_i | \bar{A}_i | none | none | remaining \bar{A} and \bar{B} , C_n | \bar{F}_i |

4-bit arithmetic logic unit

74HC/HCT181

RATINGS (for A=B output only)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | CONDITIONS |
|-----------|----------------------------------|------|------|------|----------------------|
| V_O | DC output voltage | -0.5 | +7.0 | V | |
| $-I_{OK}$ | DC output diode current | | 20 | mA | for $V_O < -0.5$ V |
| $-I_O$ | DC output source or sink current | | 25 | mA | for -0.5 V $< V_O$ |

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | | | |
|-----------------|-----------------------------------|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------------|-------------------------------------|--|
| | | 74HC | | | | | | | | V _{CC} (V) | V _{IL} | OTHER | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | | |
| I _{oz} | HIGH level output leakage current | | | 0.5 | | 5.0 | | 10.0 | μA | 2.0 to 6.0 | V _{IL} | note 1 V _O = 0 or 6 V | |

Note to the DC characteristics

- The maximum operating output voltage (V_{O(max)}) is 6.0 V.

4-bit arithmetic logic unit

74HC/HCT181

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------|---|----------------|----------------|-----------------|------------|-----------------|-------------|-----------------|----|-------------------|-----------------|--|-------|
| | | 74HC | | | | | | | | | V_{CC} (V) | MODE | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | | |
| t_{PHL}/t_{PLH} | propagation delay C_n to C_{n+4} | | 55 20 16 | 165 33 28 | | 205 41 35 | | 250 50 43 | ns | 2.0 4.5 6.0 | sum diff | M = 0 V; Fig.9; Tables 1 and 2 | |
| t_{PHL}/t_{PLH} | propagation delay C_n to \overline{F}_n | | 69 25 20 | 200 40 34 | | 250 50 43 | | 300 60 51 | ns | 2.0 4.5 6.0 | sum diff | M = 0 V; Fig.9; Tables 1 and 2 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{A}_n to \overline{G} | | 72 26 21 | 210 42 36 | | 265 53 45 | | 315 63 54 | ns | 2.0 4.5 6.0 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{B}_n to \overline{G} | | 77 28 22 | 230 46 39 | | 290 58 49 | | 345 69 59 | ns | 2.0 4.5 6.0 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{A}_n to \overline{G} | | 76 26 21 | 215 43 37 | | 270 54 46 | | 320 65 55 | ns | 2.0 4.5 6.0 | diff | M = $S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig.8; Table 2 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{B}_n to \overline{G} | | 77 28 22 | 240 48 41 | | 300 60 51 | | 360 72 61 | ns | 2.0 4.5 6.0 | diff | M = $S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig.8; Table 2 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{A}_n to \overline{P} | | 61 22 18 | 185 37 31 | | 230 46 39 | | 280 56 48 | ns | 2.0 4.5 6.0 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{B}_n to \overline{P} | | 63 23 18 | 195 39 33 | | 245 49 42 | | 295 59 50 | ns | 2.0 4.5 6.0 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{A}_n to \overline{P} | | 55 20 16 | 170 34 29 | | 215 43 37 | | 255 51 43 | ns | 2.0 4.5 6.0 | diff | M = $S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig.8; Table 2 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{B}_n to \overline{P} | | 63 23 18 | 195 39 33 | | 245 49 42 | | 295 59 50 | ns | 2.0 4.5 6.0 | diff | M = $S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig.8; Table 2 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{A}_i to \overline{F}_i | | 77 28 22 | 230 46 39 | | 290 58 49 | | 345 69 59 | ns | 2.0 4.5 6.0 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{B}_i to \overline{F}_i | | 85 31 25 | 255 51 43 | | 320 64 54 | | 385 77 65 | ns | 2.0 4.5 6.0 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{A}_i to \overline{F}_i | | 77 28 22 | 235 47 40 | | 295 59 50 | | 355 71 60 | ns | 2.0 4.5 6.0 | diff | M = $S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig.8; Table 2 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{B}_i to \overline{F}_i | | 83 31 24 | 255 51 43 | | 320 64 54 | | 385 77 65 | ns | 2.0 4.5 6.0 | diff | M = $S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig.8; Table 2 | |

4-bit arithmetic logic unit

74HC/HCT181

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|--|-----------------------|----------------|-----------------|------------|-----------------|-------------|-----------------|------|------------------------|-------|---|
| | | 74HC | | | | | | | | V _{CC} (V) | MODE | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t _{PHL} / t _{PLH} | propagation delay \bar{A}_i to \bar{F}_i | | 74 27 22 | 230 46 39 | | 290 58 49 | | 345 69 59 | ns | 2.0 4.5 6.0 | logic | M = 4.5 V; Fig.8; Table 3 |
| t _{PHL} / t _{PLH} | propagation delay \bar{B}_i to \bar{F}_i | | 83 30 24 | 255 51 43 | | 320 64 54 | | 385 77 65 | ns | 2.0 4.5 6.0 | logic | M = 4.5 V; Fig.8; Table 3 |
| t _{PHL} / t _{PLH} | propagation delay \bar{A}_n to C _{n+4} | | 80 29 23 | 235 47 40 | | 295 59 50 | | 355 71 60 | ns | 2.0 4.5 6.0 | sum | M = S ₁ = S ₂ = 0 V; S ₀ = S ₃ = 4.5 V; Fig.8; Table 1 |
| t _{PHL} / t _{PLH} | propagation delay \bar{B}_n to C _{n+4} | | 80 29 23 | 235 47 40 | | 295 59 50 | | 355 71 60 | ns | 2.0 4.5 6.0 | sum | M = S ₁ = S ₂ = 0 V; S ₀ = S ₃ = 4.5 V; Fig.8; Table 1 |
| t _{PHL} / t _{PLH} | propagation delay \bar{A}_n to C _{n+4} | | 77 28 22 | 235 47 40 | | 295 59 50 | | 355 71 60 | ns | 2.0 4.5 6.0 | diff | M = S ₀ = S ₃ = 0 V; S ₁ = S ₂ = 4.5 V; Fig.10; Table 2 |
| t _{PHL} / t _{PLH} | propagation delay \bar{B}_n to C _{n+4} | | 85 31 25 | 255 51 43 | | 320 64 54 | | 385 77 65 | ns | 2.0 4.5 6.0 | diff | M = S ₀ = S ₃ = 0 V; S ₁ = S ₂ = 4.5 V; Fig.10; Table 2 |
| t _{PZL} / t _{PLZ} | propagation delay \bar{A}_n to A=B | | 80 29 23 | 245 49 42 | | 305 61 52 | | 370 74 63 | ns | 2.0 4.5 6.0 | diff | M = S ₀ = S ₃ = 0 V; S ₁ = S ₂ = 4.5 V; Fig.11; Table 2 |
| t _{PZL} / t _{PLZ} | propagation delay \bar{B}_n to A=B | | 88 32 26 | 270 54 46 | | 340 68 58 | | 405 81 69 | ns | 2.0 4.5 6.0 | diff | M = S ₀ = S ₃ = 0 V; S ₁ = S ₂ = 4.5 V; Fig.11; Table 2 |
| t _{PHL} / t _{PLH} | propagation delay \bar{A}_n to \bar{F}_n | | 83 30 24 | 255 51 43 | | 320 64 54 | | 385 77 65 | ns | 2.0 4.5 6.0 | sum | M = S ₁ = S ₂ = 0 V; S ₀ = S ₃ = 4.5 V; Fig.7; Table 1 |
| t _{PHL} / t _{PLH} | propagation delay \bar{B}_n to \bar{F}_n | | 85 31 25 | 265 53 45 | | 330 66 56 | | 400 80 68 | ns | 2.0 4.5 6.0 | sum | M = S ₁ = S ₂ = 0 V; S ₀ = S ₃ = 4.5 V; Fig.7; Table 1 |
| t _{PHL} / t _{PLH} | propagation delay \bar{A}_n to \bar{F}_n | | 77 28 22 | 240 48 41 | | 300 60 51 | | 360 72 61 | ns | 2.0 4.5 6.0 | diff | M = S ₀ = S ₃ = 0 V; S ₁ = S ₂ = 4.5 V; Fig.8; Table 2 |
| t _{PHL} / t _{PLH} | propagation delay \bar{B}_n to \bar{F}_n | | 88 32 26 | 275 55 47 | | 345 69 59 | | 415 83 71 | ns | 2.0 4.5 6.0 | diff | M = S ₀ = S ₃ = 0 V; S ₁ = S ₂ = 4.5 V; Fig.8; Table 2 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | | note ; Figs 7 and 11 |

Note to the AC characteristics

1. For the open drain output (A=B) only t_{THL} is valid.

4-bit arithmetic logic unit

74HC/HCT181

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|-----------------|-----------------------------------|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------------|-------------------------------------|
| | | 74HCT | | | | | | | | V _{CC} (V) | V _{IL} | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| I _{OZ} | HIGH level output leakage current | | | 0.5 | | 5.0 | | 10.0 | μA | 2.0 to 6.0 | V _{IL} | note 1 V _O = 0 or 6 V |

Note to the DC characteristics

1. The maximum operating output voltage (V_{O(max)}) is 6.0 V.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|---------------------------|-----------------------|
| C _n , M | 0.50 |
| \bar{A}_n , \bar{B}_n | 0.75 |
| S _n | 1.00 |

4-bit arithmetic logic unit

74HC/HCT181

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------|---|----------------|------|------|------------|------|-------------|------|------|-----------------|-------------|--|
| | | 74HCT | | | | | | | | V_{CC} (V) | MODE | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t_{PHL}/t_{PLH} | propagation delay C_n to C_{n+4} | | 25 | 42 | | 53 | | 63 | ns | 4.5 | sum diff | M = 0 V; Fig.9; Tables 1 and 2 |
| t_{PHL}/t_{PLH} | propagation delay C_n to \bar{F}_n | | 28 | 48 | | 60 | | 72 | ns | 4.5 | sum diff | M = 0 V; Fig.9; Tables 1 and 2 |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_n to \bar{G} | | 31 | 54 | | 68 | | 81 | ns | 4.5 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 |
| t_{PHL}/t_{PLH} | propagation delay \bar{B}_n to \bar{G} | | 32 | 54 | | 68 | | 81 | ns | 4.5 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_n to \bar{G} | | 31 | 54 | | 68 | | 81 | ns | 4.5 | diff | M = $S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig.8; Table 2 |
| t_{PHL}/t_{PLH} | propagation delay \bar{B}_n to \bar{G} | | 31 | 54 | | 68 | | 81 | ns | 4.5 | diff | M = $S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig.8; Table 2 |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_n to \bar{P} | | 23 | 41 | | 51 | | 62 | ns | 4.5 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 |
| t_{PHL}/t_{PLH} | propagation delay \bar{B}_n to \bar{P} | | 24 | 41 | | 51 | | 62 | ns | 4.5 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_n to \bar{P} | | 23 | 40 | | 50 | | 60 | ns | 4.5 | diff | M = $S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig.8; Table 2 |
| t_{PHL}/t_{PLH} | propagation delay \bar{B}_n to \bar{P} | | 23 | 40 | | 50 | | 60 | ns | 4.5 | diff | M = $S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig.8; Table 2 |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_i to \bar{F}_i | | 33 | 58 | | 73 | | 87 | ns | 4.5 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 |
| t_{PHL}/t_{PLH} | propagation delay \bar{B}_i to \bar{F}_i | | 34 | 58 | | 73 | | 87 | ns | 4.5 | sum | M = $S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig.7; Table 1 |

4-bit arithmetic logic unit

74HC/HCT181

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | | |
|-------------------|---|----------------|------|------|------------|------|-------------|------|-----------------|------|-------|---|
| | | 74HCT | | | | | | | V_{CC} (V) | MODE | OTHER | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | | max. |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_i to \bar{F}_i | | 33 | 57 | | 71 | | 86 | ns | 4.5 | diff | $M = S_0 = S_3 = 0\text{ V};$ $S_1 = S_2 = 4.5\text{ V};$ Fig.8; Table 2 |
| t_{PHL}/t_{PLH} | propagation delay \bar{B}_i to \bar{F}_i | | 33 | 57 | | 71 | | 86 | ns | 4.5 | diff | $M = S_0 = S_3 = 0\text{ V};$ $S_1 = S_2 = 4.5\text{ V};$ Fig.8; Table 2 |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_i to \bar{F}_i | | 29 | 54 | | 68 | | 81 | ns | 4.5 | logic | $M = 4.5\text{ V};$ Fig.8; Table 3 |
| t_{PHL}/t_{PLH} | propagation delay \bar{B}_i to \bar{F}_i | | 33 | 54 | | 68 | | 81 | ns | 4.5 | logic | $M = 4.5\text{ V};$ Fig.8; Table 3 |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_n to C_{n+4} | | 30 | 53 | | 66 | | 80 | ns | 4.5 | sum | $M = S_1 = S_2 = 0\text{ V};$ $S_0 = S_3 = 4.5\text{ V};$ Fig.8; Table 1 |
| t_{PHL}/t_{PLH} | propagation delay \bar{B}_n to C_{n+4} | | 31 | 53 | | 66 | | 80 | ns | 4.5 | sum | $M = S_1 = S_2 = 0\text{ V};$ $S_0 = S_3 = 4.5\text{ V};$ Fig.8; Table 1 |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_n to C_{n+4} | | 30 | 55 | | 69 | | 83 | ns | 4.5 | diff | $M = S_0 = S_3 = 0\text{ V};$ $S_1 = S_2 = 4.5\text{ V};$ Fig.10; Table 2 |
| t_{PHL}/t_{PLH} | propagation delay \bar{B}_n to C_{n+4} | | 34 | 55 | | 69 | | 83 | ns | 4.5 | diff | $M = S_0 = S_3 = 0\text{ V};$ $S_1 = S_2 = 4.5\text{ V};$ Fig.10; Table 2 |
| t_{PZL}/t_{PLZ} | propagation delay \bar{A}_n to $A=B$ | | 34 | 60 | | 75 | | 90 | ns | 4.5 | diff | $M = S_0 = S_3 = 0\text{ V};$ $S_1 = S_2 = 4.5\text{ V};$ Fig.11; Table 2 |
| t_{PZL}/t_{PLZ} | propagation delay \bar{B}_n to $A=B$ | | 35 | 60 | | 75 | | 90 | ns | 4.5 | diff | $M = S_0 = S_3 = 0\text{ V};$ $S_1 = S_2 = 4.5\text{ V};$ Fig.11; Table 2 |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_n to \bar{F}_n | | 33 | 56 | | 70 | | 84 | ns | 4.5 | sum | $M = S_1 = S_2 = 0\text{ V};$ $S_0 = S_3 = 4.5\text{ V};$ Fig.7; Table 1 |
| t_{PHL}/t_{PLH} | propagation delay \bar{B}_n to \bar{F}_n | | 33 | 56 | | 70 | | 84 | ns | 4.5 | sum | $M = S_1 = S_2 = 0\text{ V};$ $S_0 = S_3 = 4.5\text{ V};$ Fig.7; Table 1 |

4-bit arithmetic logic unit

74HC/HCT181

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------|---|----------------|------|------|------------|------|-------------|------|----|------|-----------------|--|-------|
| | | 74HCT | | | | | | | | | V_{CC} (V) | MODE | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | | |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_n to \bar{F}_n | | 32 | 56 | | 70 | | 84 | ns | 4.5 | diff | $M = S_0 = S_3 = 0 V$; $S_1 = S_2 = 4.5 V$; Fig.8; Table 2 | |
| t_{PHL}/t_{PLH} | propagation delay \bar{A}_n to \bar{F}_n | | 33 | 56 | | 70 | | 84 | ns | 4.5 | diff | $M = S_0 = S_3 = 0 V$; $S_1 = S_2 = 4.5 V$; Fig.8; Table 2 | |
| t_{THL}/t_{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | | Figs 7 and 11; note 1 | |

Note to the AC characteristics

1. For the open drain output (A=B) only t_{THL} is valid.

4-bit arithmetic logic unit

74HC/HCT181

AC WAVEFORMS

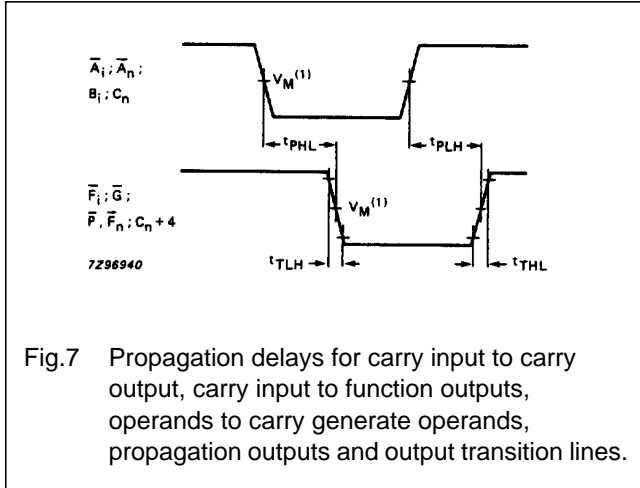


Fig.7 Propagation delays for carry input to carry output, carry input to function outputs, operands to carry generate operands, propagate outputs and function outputs.

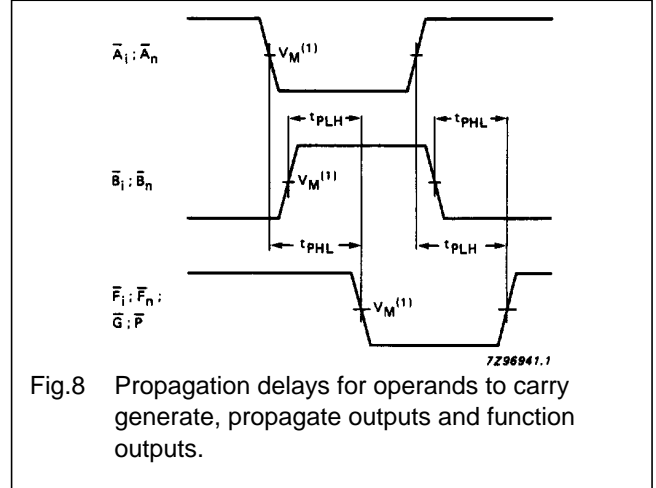


Fig.8 Propagation delays for operands to carry generate, propagate outputs and function outputs.

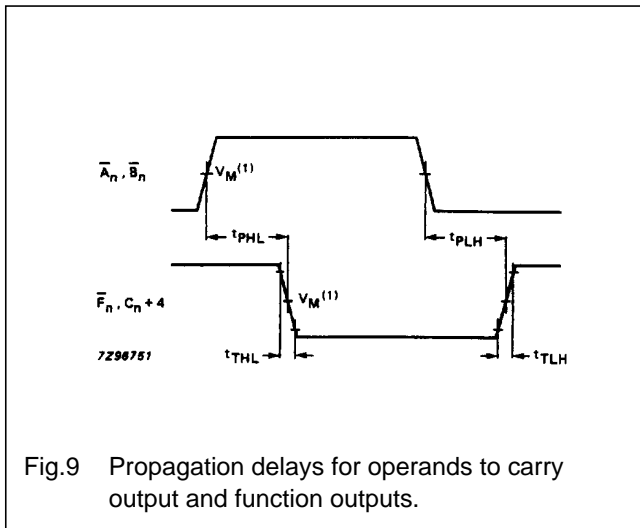


Fig.9 Propagation delays for operands to carry output and function outputs.

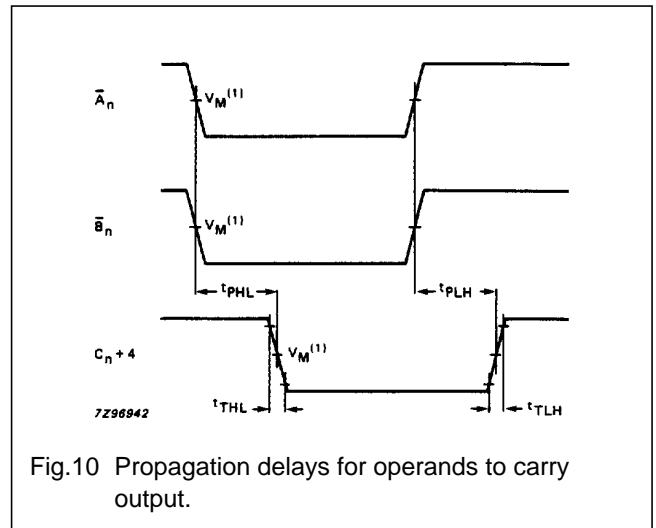


Fig.10 Propagation delays for operands to carry output.

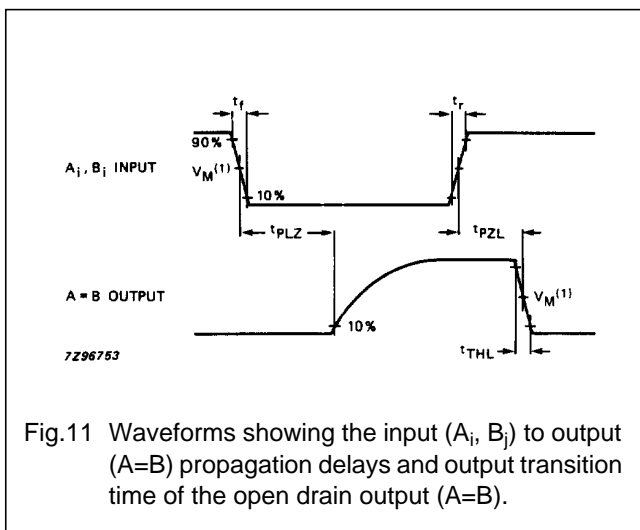


Fig.11 Waveforms showing the input (A_i, B_i) to output (A=B) propagation delays and output transition time of the open drain output (A=B).

Note to AC waveforms

- (1) HC: $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
- HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

APPLICATION INFORMATION

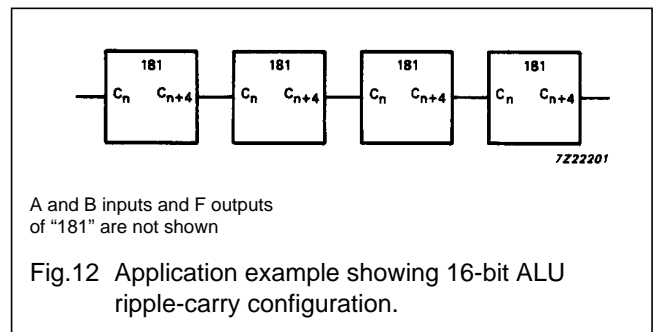


Fig.12 Application example showing 16-bit ALU ripple-carry configuration.

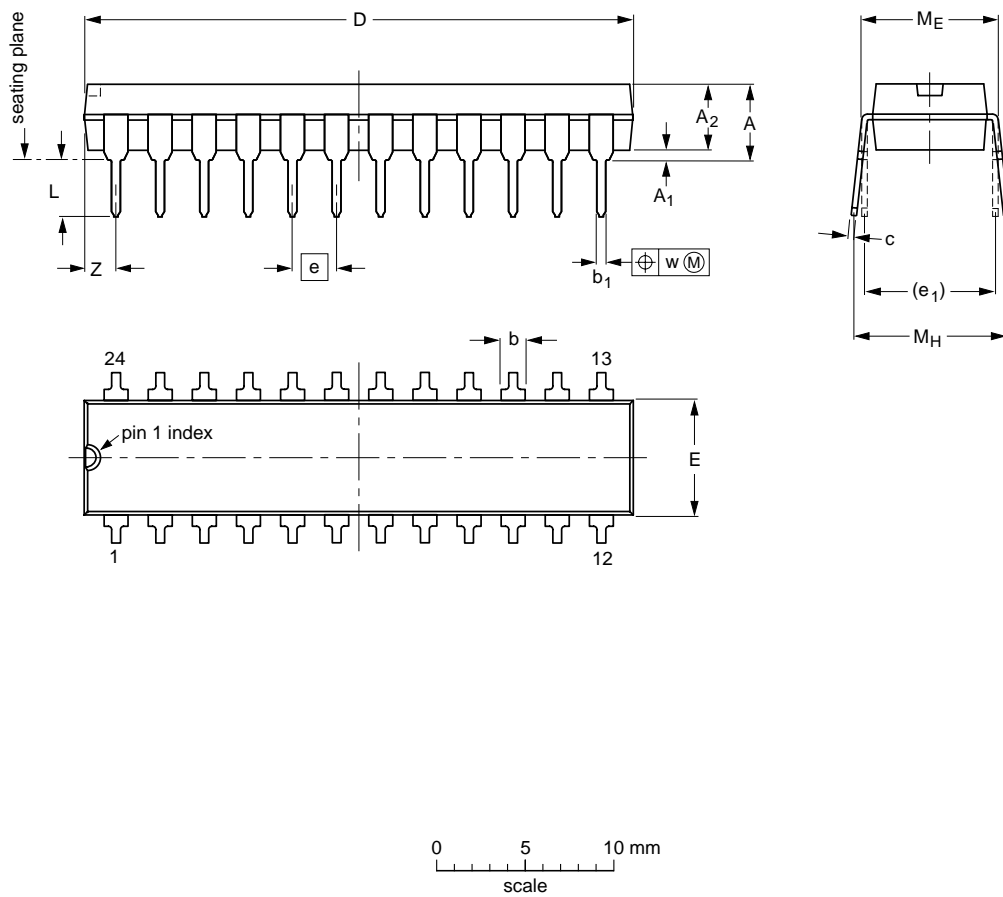
4-bit arithmetic logic unit

74HC/HCT181

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|----------------|----------------|----------------|------|-----------------------|
| mm | 4.70 | 0.38 | 3.94 | 1.63 1.14 | 0.56 0.43 | 0.36 0.25 | 31.9 31.5 | 6.73 6.48 | 2.54 | 7.62 | 3.51 3.05 | 8.13 7.62 | 10.03 7.62 | 0.25 | 2.05 |
| inches | 0.185 | 0.015 | 0.155 | 0.064 0.045 | 0.022 0.017 | 0.014 0.010 | 1.256 1.240 | 0.265 0.255 | 0.100 | 0.300 | 0.138 0.120 | 0.32 0.30 | 0.395 0.300 | 0.01 | 0.081 |

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

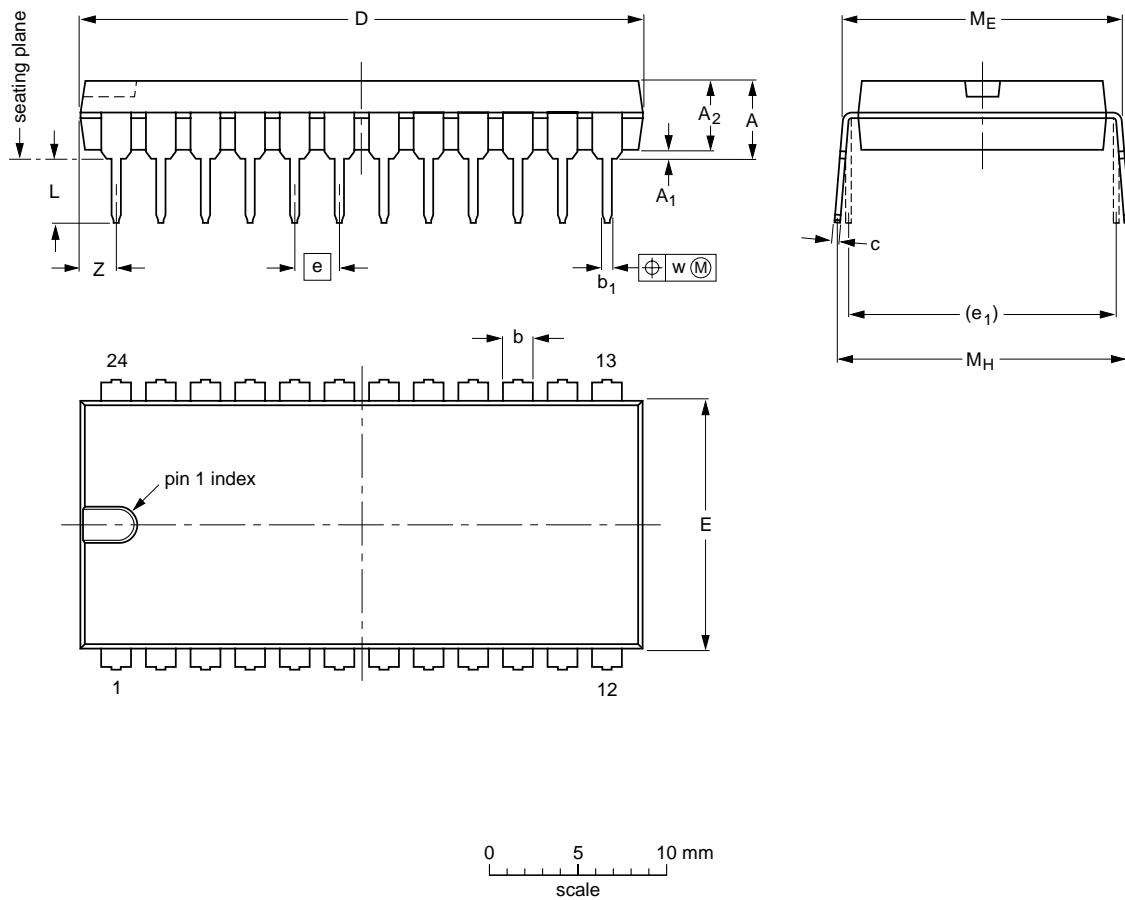
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT222-1 | | MS-001AF | | | | 95-03-11 |

4-bit arithmetic logic unit

74HC/HCT181

DIP24: plastic dual in-line package; 24 leads (600 mil)

SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|------|-----------------------|
| mm | 5.1 | 0.51 | 4.0 | 1.7 1.3 | 0.53 0.38 | 0.32 0.23 | 32.0 31.4 | 14.1 13.7 | 2.54 | 15.24 | 3.9 3.4 | 15.80 15.24 | 17.15 15.90 | 0.25 | 2.2 |
| inches | 0.20 | 0.020 | 0.16 | 0.066 0.051 | 0.021 0.015 | 0.013 0.009 | 1.26 1.24 | 0.56 0.54 | 0.10 | 0.60 | 0.15 0.13 | 0.62 0.60 | 0.68 0.63 | 0.01 | 0.087 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

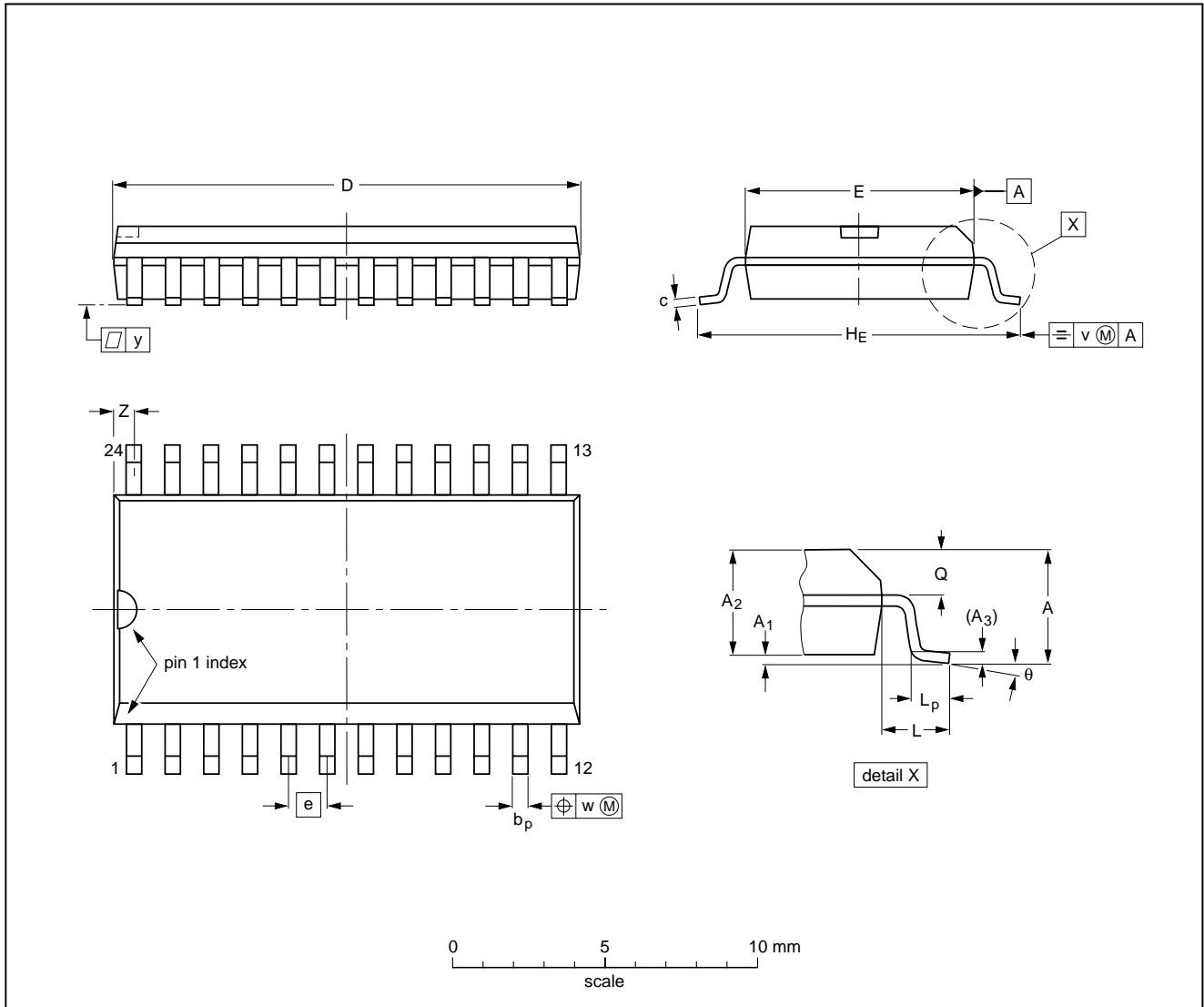
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT101-1 | 051G02 | MO-015AD | | | | 92-11-17 95-01-23 |

4-bit arithmetic logic unit

74HC/HCT181

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 2.65 | 0.30 0.10 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 15.6 15.2 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.4 | 1.1 0.4 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 0.9 0.4 | 8° 0° |
| inches | 0.10 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.61 0.60 | 0.30 0.29 | 0.050 | 0.419 0.394 | 0.055 | 0.043 0.016 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.035 0.016 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | |
| SOT137-1 | 075E05 | MS-013AD | | | 95-01-24 97-05-22 |

4-bit arithmetic logic unit

74HC/HCT181

SOLDERING**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

DIP**SOLDERING BY DIPPING OR BY WAVE**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO**REFLOW SOLDERING**

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

4-bit arithmetic logic unit

74HC/HCT181

DEFINITIONS

| | |
|---|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.