

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT237**

**3-to-8 line decoder/demultiplexer  
with address latches**

Product specification  
File under Integrated Circuits, IC06

December 1990

## 3-to-8 line decoder/demultiplexer with address latches

## 74HC/HCT237

### FEATURES

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active HIGH mutually exclusive outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT237 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT237 are 3-to-8 line decoder/demultiplexers with latches at the three address inputs (A<sub>n</sub>). The "237" essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled ( $\overline{LE} = \text{LOW}$ ), the "237" acts as a 3-to-8 active LOW decoder. When the latch enable ( $\overline{LE}$ ) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as  $\overline{LE}$  remains HIGH.

The output enable input ( $\overline{E}_1$  and E<sub>2</sub>) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless  $\overline{E}_1$  is LOW and E<sub>2</sub> is HIGH.

The "237" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub> $\overline{LE}$ to Y <sub>n</sub> $\overline{E}_1$ to Y <sub>n</sub> E <sub>2</sub> to Y <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	16 19 14 14	19 21 17 17	ns ns ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	60	63	pF

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION

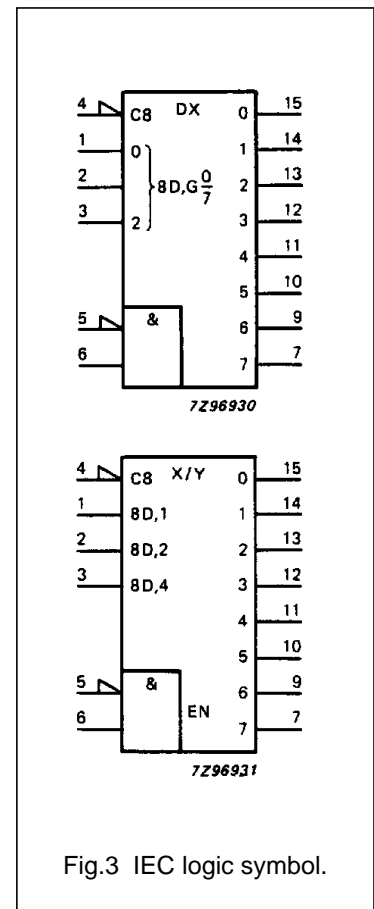
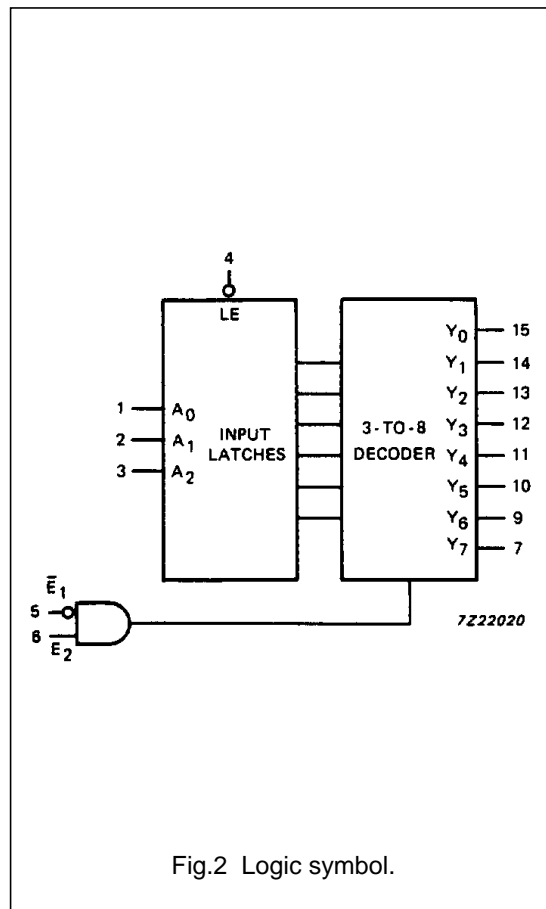
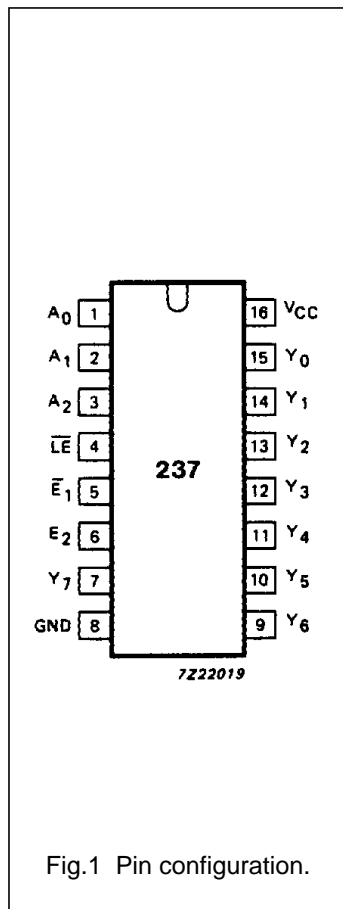
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# 3-to-8 line decoder/demultiplexer with address latches

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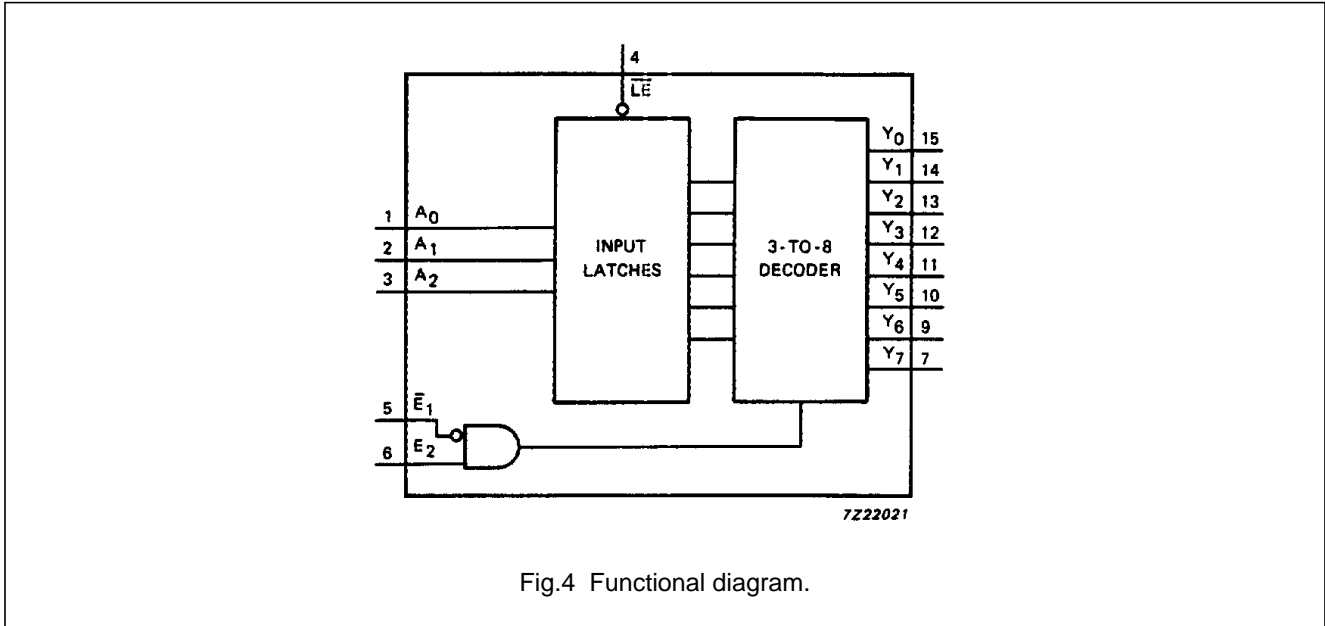
## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A <sub>0</sub> to A <sub>2</sub>	data inputs
4	$\overline{LE}$	latch enable input (active LOW)
5	$\overline{E}_1$	data enable input (active LOW)
6	E <sub>2</sub>	data enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	Y <sub>0</sub> to Y <sub>7</sub>	multiplexer outputs
16	V <sub>CC</sub>	positive supply voltage



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FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	$E_2$	$A_0$	$A_1$	$A_2$	$Y_0$	$Y_1$	$Y_2$	$Y_3$	$Y_4$	$Y_5$	$Y_6$	$Y_7$
H	L	H	X	X	X	stable							
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

Notes

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care

### 3-to-8 line decoder/demultiplexer with address latches

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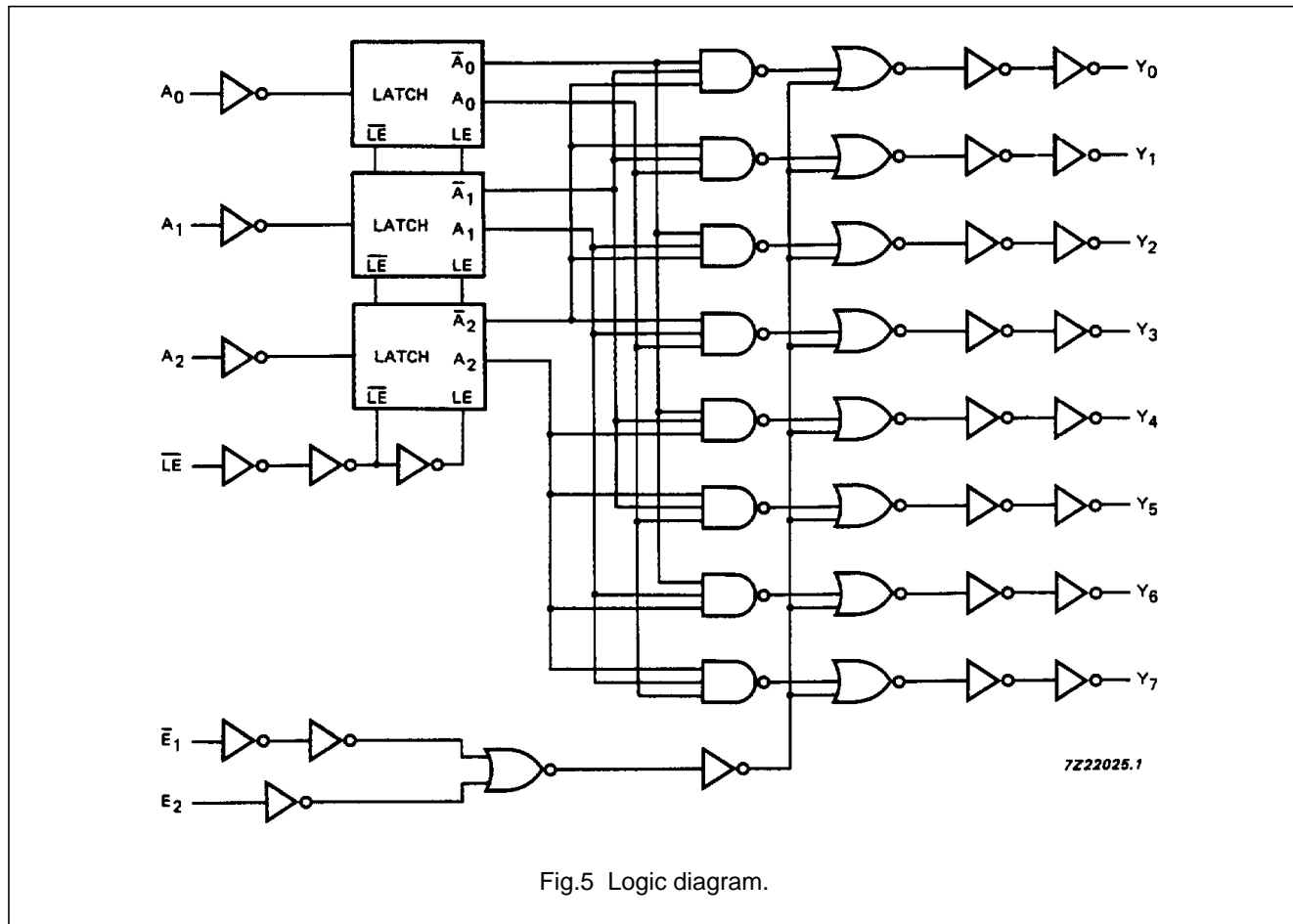


Fig.5 Logic diagram.

# 3-to-8 line decoder/demultiplexer with address latches

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Y <sub>n</sub>		61 22 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E <sub>1</sub> to Y <sub>n</sub>		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E <sub>2</sub> to Y <sub>n</sub>		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	LE pulse width LOW	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.8
t <sub>su</sub>	set-up time A <sub>n</sub> to LE	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.8
t <sub>h</sub>	hold time A <sub>n</sub> to LE	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig.8

## 3-to-8 line decoder/demultiplexer with address latches

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### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

#### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A <sub>n</sub>	1.50
$\overline{E}_1$	1.50
E <sub>2</sub>	1.50
$\overline{LE}$	1.50

### AC CHARACTERISTICS FOR 74HCT

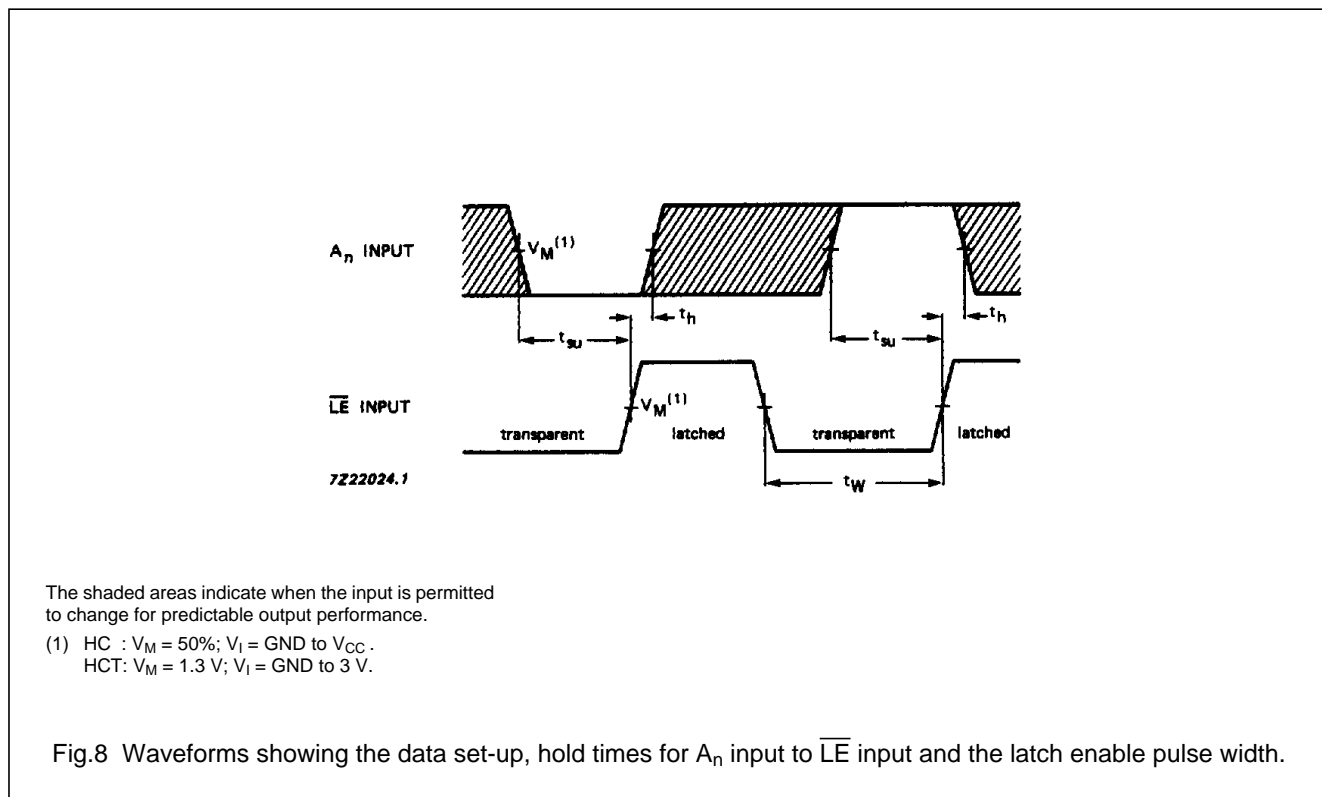
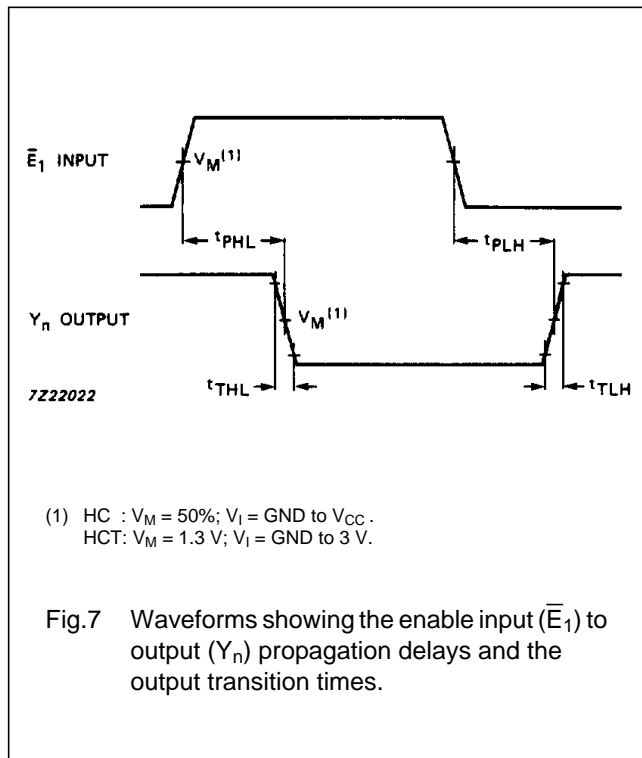
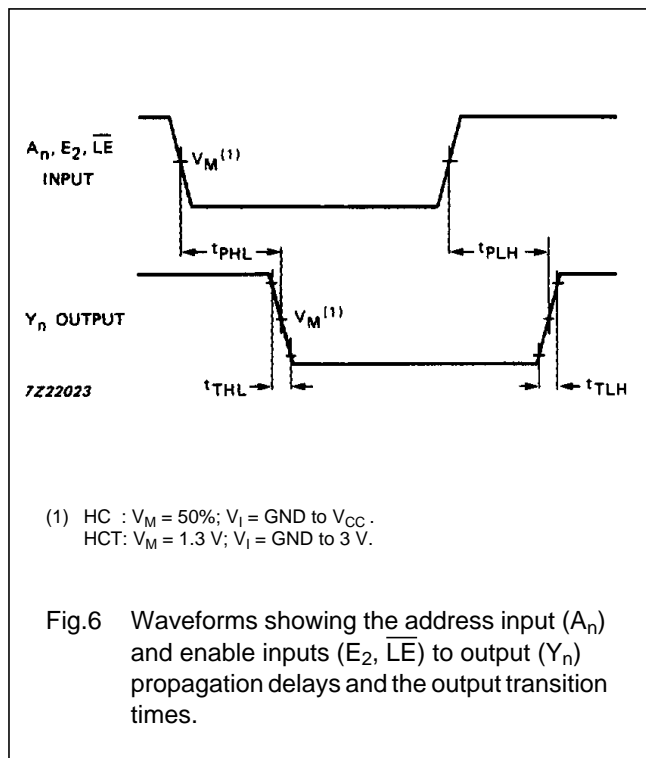
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>		22	38		48		57	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{LE}$ to Y <sub>n</sub>		25	42		53		63	ns	4.5	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{E}_1$ to Y <sub>n</sub>		20	35		44		53	ns	4.5	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E <sub>2</sub> to Y <sub>n</sub>		20	33		41		50	ns	4.5	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6
t <sub>w</sub>	$\overline{LE}$ pulse width HIGH	10	5		13		15		ns	4.5	Fig.8
t <sub>su</sub>	set-up time A <sub>n</sub> to $\overline{LE}$	10	2		13		15		ns	4.5	Fig.8
t <sub>h</sub>	hold time A <sub>n</sub> to $\overline{LE}$	5	0		5		5		ns	4.5	Fig.8

# 3-to-8 line decoder/demultiplexer with address latches

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## AC WAVEFORMS





# 3-to-8 line decoder/demultiplexer with address latches

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## APPLICATION INFORMATION

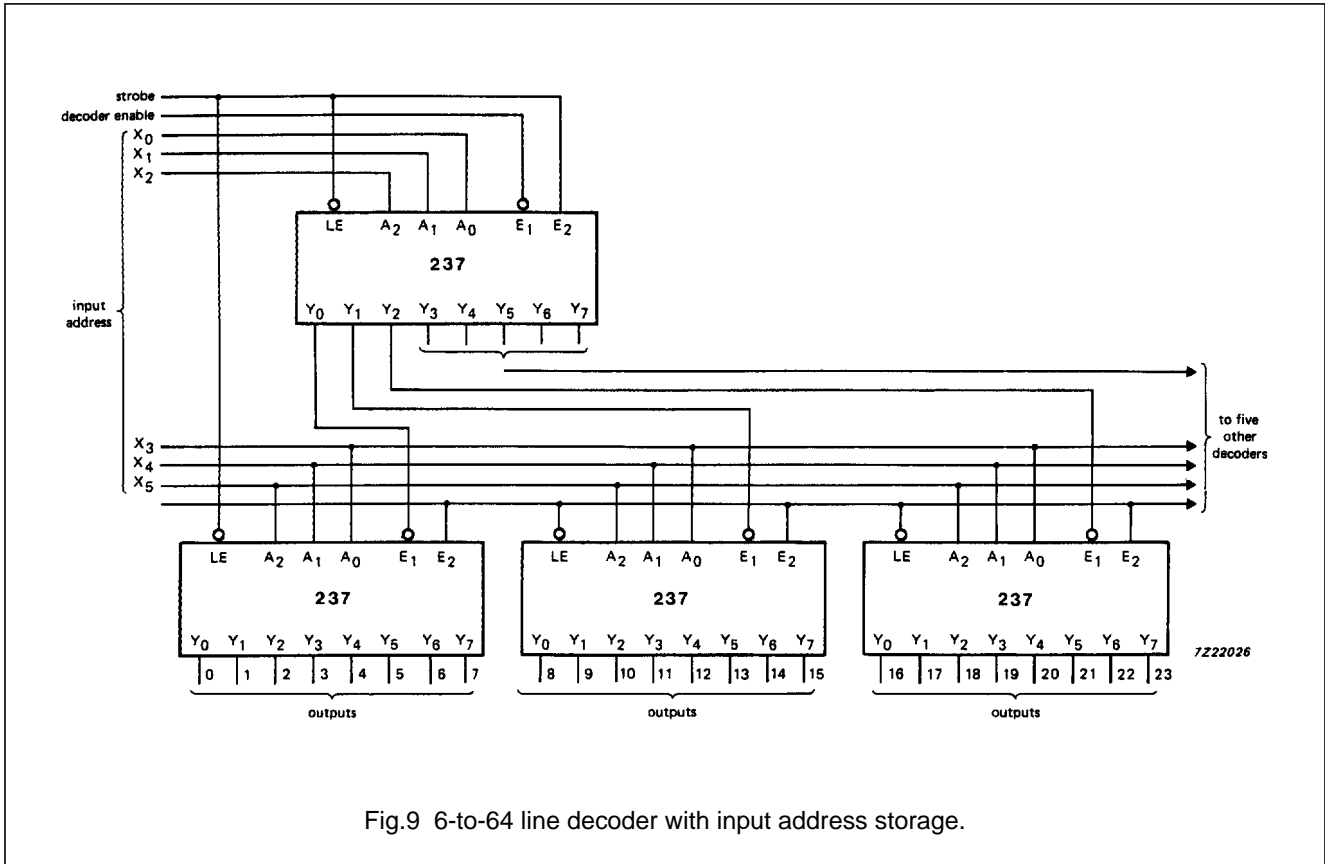


Fig.9 6-to-64 line decoder with input address storage.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".