

## 74LCX16841

### Low Voltage 20-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

#### General Description

The LCX16841 contains twenty non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH, the outputs are in a high impedance state.

The LCX16841 is designed for low voltage (2.5V or 3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

The LCX16841 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V  $V_{CC}$  specifications provided
- 5.5 ns  $t_{PD}$  max ( $V_{CC} = 3.3V$ ), 20  $\mu A$   $I_{CC}$  max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- $\pm 24$  mA output drive ( $V_{CC} = 3.0V$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

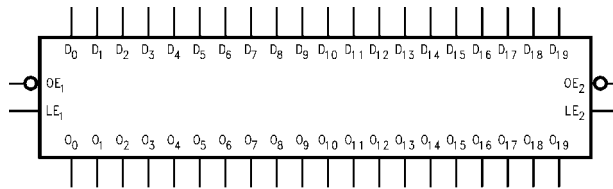
**Note 1:** To ensure the high-impedance state during power up or down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value or the resistor is determined by the current-sourcing capability of the driver.

#### Ordering Code:

Order Number	Package Number	Package Description
74LCX16841MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
74LCX16841MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

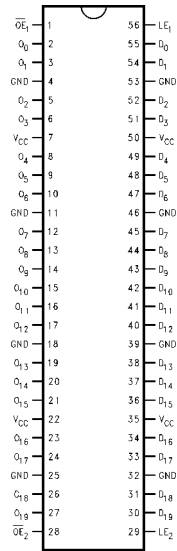
#### Logic Symbol



#### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$LE_n$	Latch Enable Input
$D_0$ – $D_{19}$	Inputs
$O_0$ – $O_{19}$	Outputs

Connection Diagram



Truth Tables

Inputs			Outputs
LE <sub>1</sub>	OE <sub>1</sub>	D <sub>0</sub> -D <sub>9</sub>	O <sub>0</sub> -O <sub>9</sub>
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O <sub>0</sub>

Inputs			Outputs
LE <sub>2</sub>	OE <sub>2</sub>	D <sub>10</sub> -D <sub>19</sub>	O <sub>10</sub> -O <sub>19</sub>
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O <sub>0</sub>

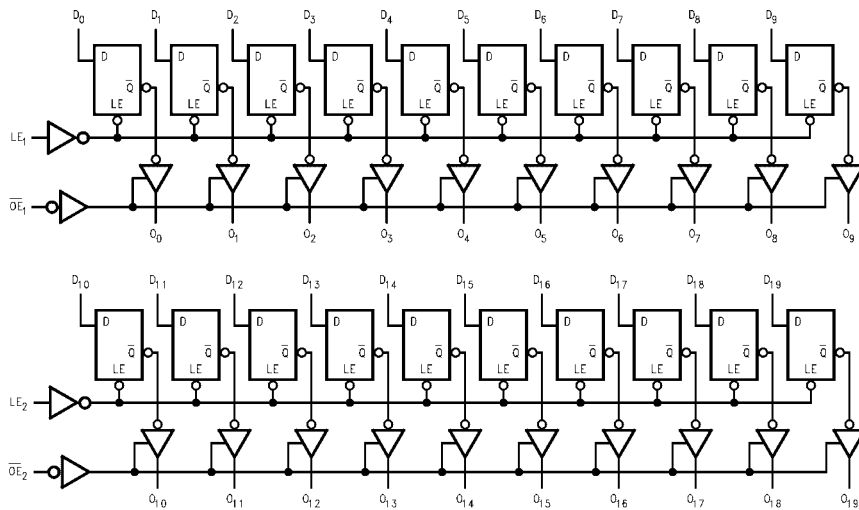
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 O<sub>0</sub> = Previous O<sub>0</sub> before HIGH-to-LOW transition of Latch Enable

Functional Description

The LCX16841 contains twenty D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 20-bit operation. The following description applies to each byte. When the Latch Enable (LE<sub>n</sub>) input is HIGH, data on the D<sub>n</sub> enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time

its D input changes. When LE<sub>n</sub> is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE<sub>n</sub>. The 3-STATE standard outputs are controlled by the Output Enable (OE<sub>n</sub>) input. When OE<sub>n</sub> is LOW, the standard outputs are in the 2-state mode. When OE<sub>n</sub> is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)				
Symbol	Parameter	Value	Conditions	Units
V <sub>CC</sub>	Supply Voltage	-0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0		V
V <sub>O</sub>	DC Output Voltage	-0.5 to +7.0 -0.5 to V <sub>CC</sub> + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 3)	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature	-65 to +150		°C

Recommended Operating Conditions (Note 4)					
Symbol	Parameter	Min	Max	Units	
V <sub>CC</sub>	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V <sub>I</sub>	Input Voltage	0	5.5	V	
V <sub>O</sub>	Output Voltage	HIGH or LOW State	0	V <sub>CC</sub>	V
		3-STATE	0	5.5	
I <sub>OH</sub> /I <sub>OL</sub>	Output Current	V <sub>CC</sub> = 3.0V – 3.6V		±24	mA
		V <sub>CC</sub> = 2.7V – 3.0V		±12	
		V <sub>CC</sub> = 2.3V – 2.7V		±8	
T <sub>A</sub>	Free-Air Operating Temperature	-40	85	°C	
Δt/ΔV	Input Edge Rate, V <sub>IN</sub> = 0.8V – 2.0V, V <sub>CC</sub> = 3.0V	0	10	ns/V	

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** I<sub>O</sub> Absolute Maximum Rating must be observed.

**Note 4:** Unused inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units
				Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V <sub>IL</sub>	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA	2.3 – 3.6	V <sub>CC</sub> - 0.2		V
			2.3	1.8		
			2.7	2.2		
			3.0	2.4		
			3.0	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.3 – 3.6		0.2	V
			2.3		0.6	
			2.7		0.4	
			3.0		0.4	
			3.0		0.55	
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 5.5V	2.3 – 3.6		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 5.5V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.3 – 3.6		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 5.5V	0		10	μA

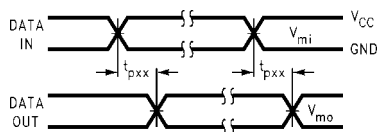
DC Electrical Characteristics (Continued)								
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units		
				Min	Max			
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 – 3.6		20	μA		
		3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V (Note 5)	2.3 – 3.6		±20			
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.3 – 3.6		500	μA		
<b>Note 5:</b> Outputs disabled or 3-STATE only.								
AC Electrical Characteristics								
Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
		Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	1.5	5.5	1.5	6.0	1.5	6.6	ns
t <sub>PLH</sub>	D <sub>n</sub> to O <sub>n</sub>	1.5	5.5	1.5	6.0	1.5	6.6	
t <sub>PHL</sub>	Propagation Delay	1.5	5.5	1.5	6.5	1.5	6.6	ns
t <sub>PLH</sub>	LE to O <sub>n</sub>	1.5	5.5	1.5	6.5	1.5	6.6	
t <sub>PZL</sub>	Output Enable Time	1.5	6.5	1.5	7.0	1.5	8.5	ns
t <sub>PZH</sub>		1.5	6.5	1.5	7.0	1.5	8.5	
t <sub>PLZ</sub>	Output Disable Time	1.5	6.5	1.5	7.0	1.5	7.8	ns
t <sub>PHZ</sub>		1.5	6.5	1.5	7.0	1.5	7.8	
t <sub>OSSL</sub>	Output to Output Skew (Note 6)		1.0					ns
t <sub>OSLH</sub>			1.0					
t <sub>S</sub>	Setup Time, D <sub>n</sub> to LE	2.5		2.5		3.0		ns
t <sub>H</sub>	Hold Time, D <sub>n</sub> to LE	1.5		1.5		2.0		ns
t <sub>W</sub>	LE Pulse Width	3.3		3.3		3.8		ns
<b>Note 6:</b> Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t <sub>OSSL</sub> ) or LOW-to-HIGH (t <sub>OSLH</sub> ).								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		Units		
				Typical				
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8	V			
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	0.6				
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	-0.8	V			
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	-0.6				
Capacitance								
Symbol	Parameter	Conditions	Typical	Units				
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF				
C <sub>O</sub>	Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF				
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz	20	pF				

**AC LOADING and WAVEFORMS** Generic for LCX Family

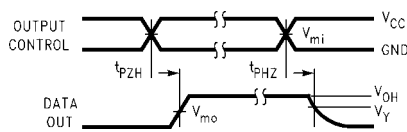


**FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)**

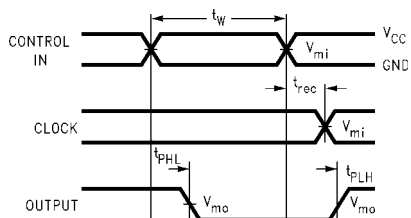
Test	Switch
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}, t_{PHZ}$	GND



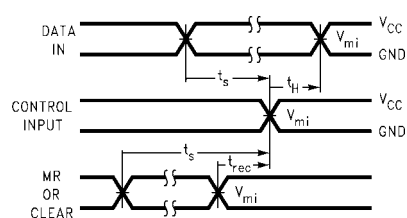
**Waveform for Inverting and Non-Inverting Functions**



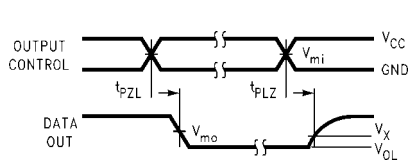
**3-STATE Output High Enable and Disable Times for Logic**



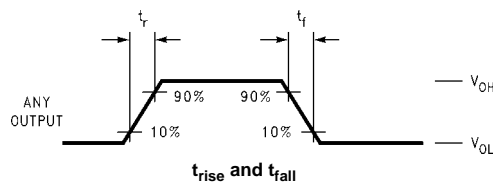
**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



**Setup Time, Hold Time and Recovery Time for Logic**



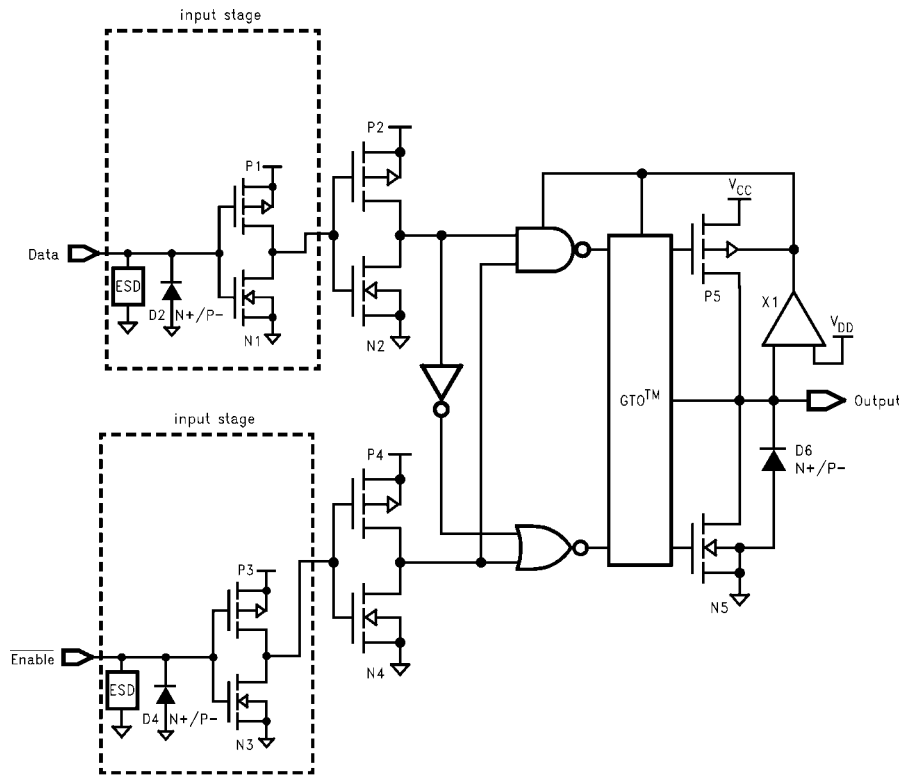
**3-STATE Output Low Enable and Disable Times for Logic**



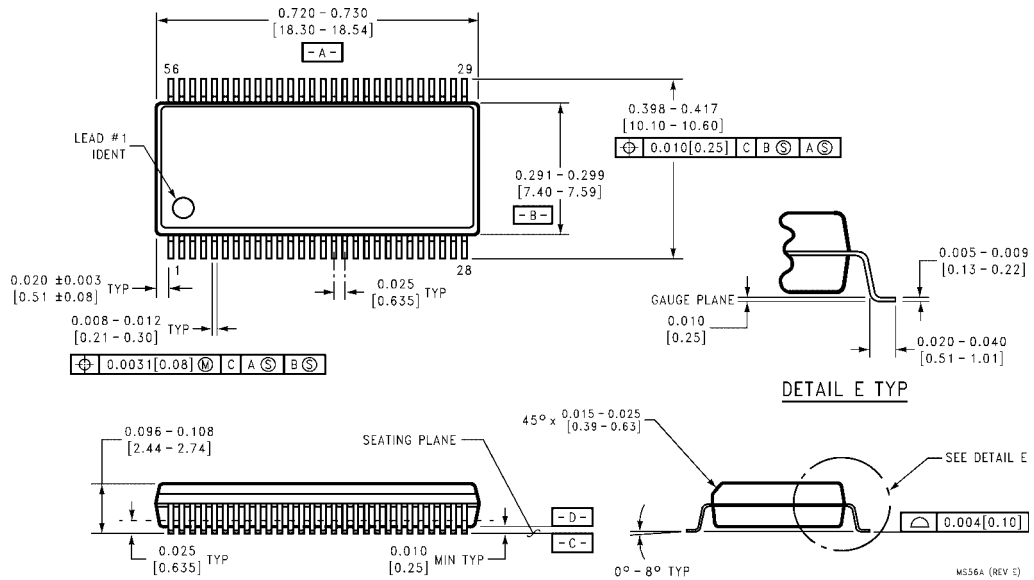
**FIGURE 2. Waveforms**  
(Input Characteristics;  $f = 1MHz, t_r = t_f = 3ns$ )

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

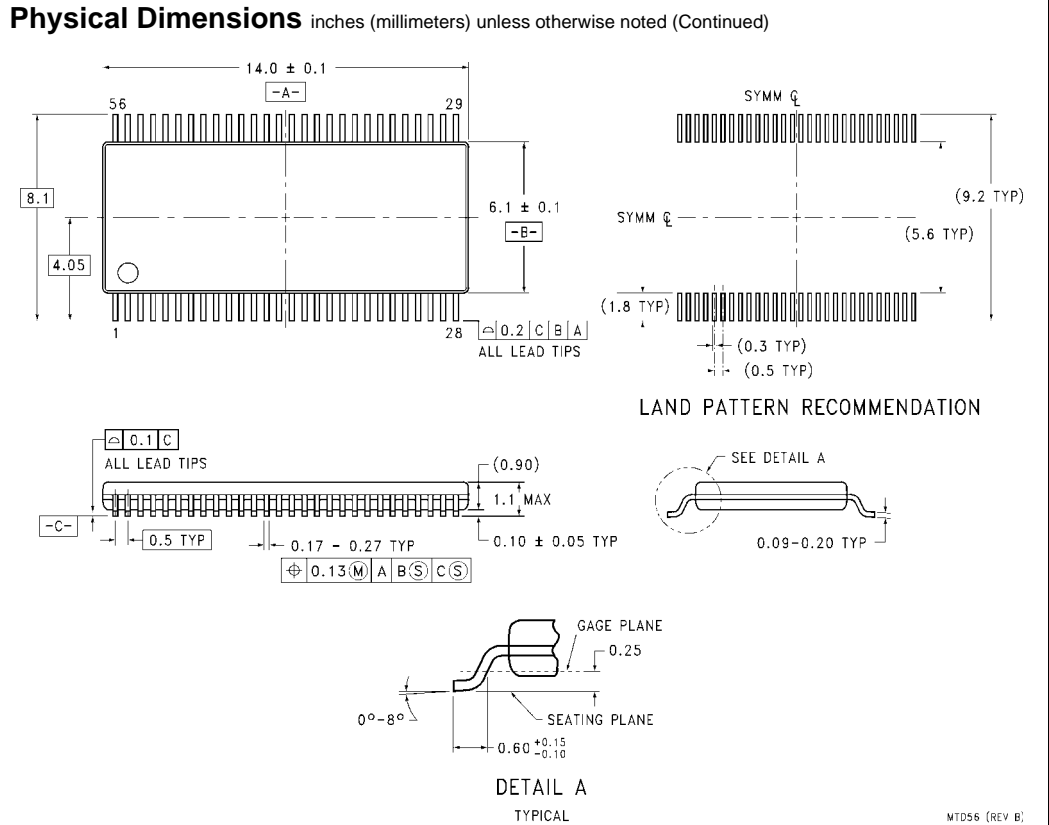
### Schematic Diagram Generic for LCX Family



**Physical Dimensions** inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide  
Package Number MS56A**



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD56

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