

74LCXP16245

Low Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs/Outputs and Pull-Down Resistors

General Description

The LCXP16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The T/R inputs determine the direction of data flow through the device. The \overline{OE} inputs disable both the A and B ports by placing them in a high impedance state.

In addition, A and B port datapath pins have built-in resistors to GND allowing the pins to float without any increase in I_{CC} current. This feature is intended to address modular and space constrained applications where additional space consumed by external resistors is not available.

The LCXP16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- I/O pull-down resistors terminate inactive busses ensuring a stable bus state
- 5.5 ns t_{PD} max ($V_{CC} = 3.3V$), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Pinout compatible with 74 series 16245
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

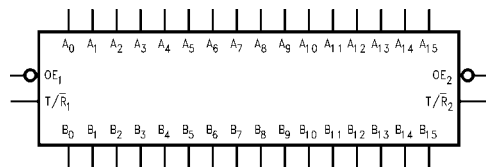
Note 1: To ensure the high-impedance state during power up or down \overline{OE} should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCXP16245MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCXP16245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

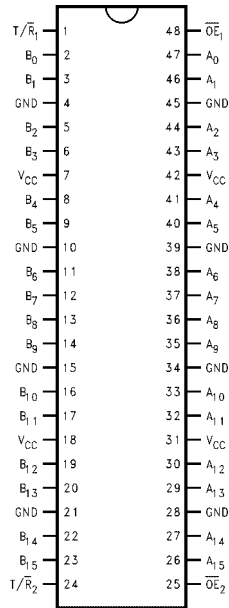
Logic Symbol



Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input
T/R_n	Transmit/Receive Input
A ₀ –A ₁₅	Side A Inputs or 3-STATE Outputs
B ₀ –B ₁₅	Side B Inputs or 3-STATE Outputs

Connection Diagram



Truth Tables

Inputs		Outputs
\overline{OE}_1	T/\overline{R}_1	
L	L	Bus B ₀ -B ₇ Data to Bus A ₀ -A ₇
L	H	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇
H	X	HIGH Z State on A ₀ -A ₇ , B ₀ -B ₇ (Note 2)

Inputs		Outputs
\overline{OE}_2	T/\overline{R}_2	
L	L	Bus B ₈ -B ₁₅ Data to Bus A ₈ -A ₁₅
L	H	Bus A ₈ -A ₁₅ Data to Bus B ₈ -B ₁₅
H	X	HIGH Z State on A ₈ -A ₁₅ , B ₈ -B ₁₅ (Note 2)

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

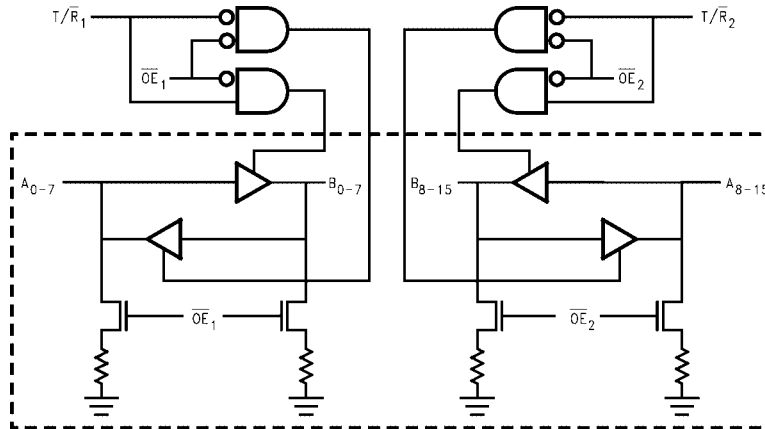
Note 2: A and B port inputs are still active.

Functional Descriptions

The LCXP16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The T/\overline{R} inputs determine the direction of data flow through the device.

The \overline{OE} inputs disable both the A and B ports by placing them in a high impedance state. The pulldown resistor (30K Ω normal) to GND is active only when the outputs are 3-STATE (\overline{OE} = HIGH). When the outputs become active (\overline{OE} = LOW) the resistor is removed from the circuit.

Logic Diagram



Absolute Maximum Ratings (Note 3)					
Symbol	Parameter	Value	Conditions	Units	
V_{CC}	Supply Voltage	-0.5 to +7.0		V	
V_I	DC Input Voltage	-0.5 to +7.0		V	
V_O	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V	
		-0.5 to $V_{CC} + 0.5$	Output in HIGH or LOW State (Note 4)		
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA	
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA	
		+50	$V_O > V_{CC}$		
I_O	DC Output Source/Sink Current	± 50		mA	
I_{CC}	DC Supply Current per Supply Pin	± 100		mA	
I_{GND}	DC Ground Current per Ground Pin	± 100		mA	
T_{STG}	Storage Temperature	-65 to +150		°C	

Recommended Operating Conditions					
Symbol	Parameter	Min	Max	Units	
V_{CC}	Supply Voltage				
	Operating	2.0	3.6	V	
	Data Retention	1.5	3.6		
V_I	Input Voltage	0	5.5	V	
V_O	Output Voltage				
	HIGH or LOW State	0	V_{CC}	V	
	3-STATE	0	5.5		
I_{OH}/I_{OL}	Output Current				
	$V_{CC} = 3.0V - 3.6V$		± 24	mA	
	$V_{CC} = 2.7V - 3.0V$		± 12		
	$V_{CC} = 2.3V - 2.7V$		± 8		
T_A	Free-Air Operating Temperature	-40	85	°C	
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$, $V_{CC} = 3.0V$	0	10	ns/V	

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics						
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^\circ C$ to $+85^\circ C$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -8 mA$	2.3	1.8		
		$I_{OH} = -12 mA$	2.7	2.2		
		$I_{OH} = -18 mA$	3.0	2.4		
		$I_{OH} = -24 mA$	3.0	2.2		
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 3.6		0.2	V
		$I_{OL} = 8 mA$	2.3		0.6	
		$I_{OL} = 12 mA$	2.7		0.4	
		$I_{OL} = 16 mA$	3.0		0.4	
		$I_{OL} = 24 mA$	3.0		0.55	
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 - 3.6		± 5.0	μA
$I_{OZ(L)}$	3-STATE I/O Leakage	V_I or $V_O = 0.0V$	2.3 - 3.6		± 5.0	μA
$I_{OZ(H)}$	3-STATE I/O Leakage	V_I or $V_O = 5.5V$	2.3 - 3.6	50	500	μA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 - 3.6		20	μA
		$3.6V \leq V_I, V_O \leq 5.5V$ (Note 5)	2.3 - 3.6		± 20	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.3 - 3.6		500	μA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L = 50 pF		C _L = 50 pF		C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.5	5.5	1.5	6.0	1.5	6.6	ns
t _{PLH}	A _n to B _n or B _n to A _n	1.5	5.5	1.5	6.0	1.5	6.6	
t _{PZL}	Output Enable Time	1.5	7.0	1.5	8.0	1.5	9.1	ns
t _{PZH}		1.5	7.0	1.5	8.0	1.5	9.1	
t _{PLZ}	Output Disable Time	1.5	7.0	1.5	7.5	1.5	8.4	ns
t _{PHZ}		1.5	7.0	1.5	7.5	1.5	8.4	
t _{OSHL}	Output to Output Skew (Note 6)		1.0					ns
t _{OSLH}			1.0					

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	0.6	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	-0.8	V
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	-0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF
C _{I/O}	Input/Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

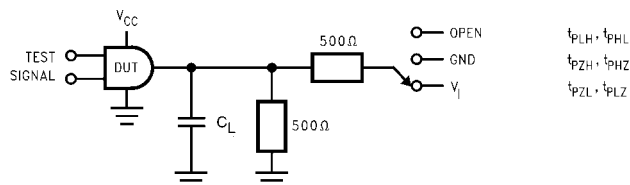
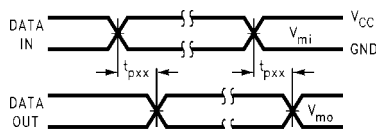
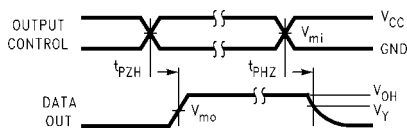


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

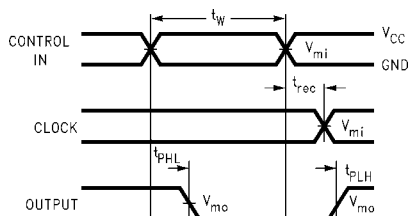
Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH} , t_{PHZ}	GND



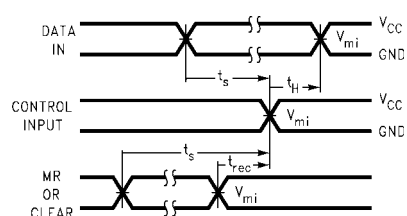
Waveform for Inverting and Non-Inverting Functions



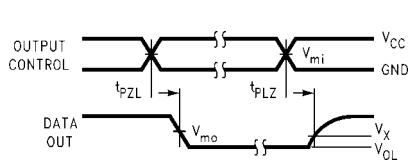
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

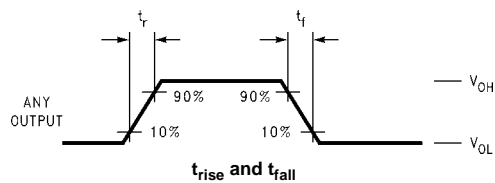
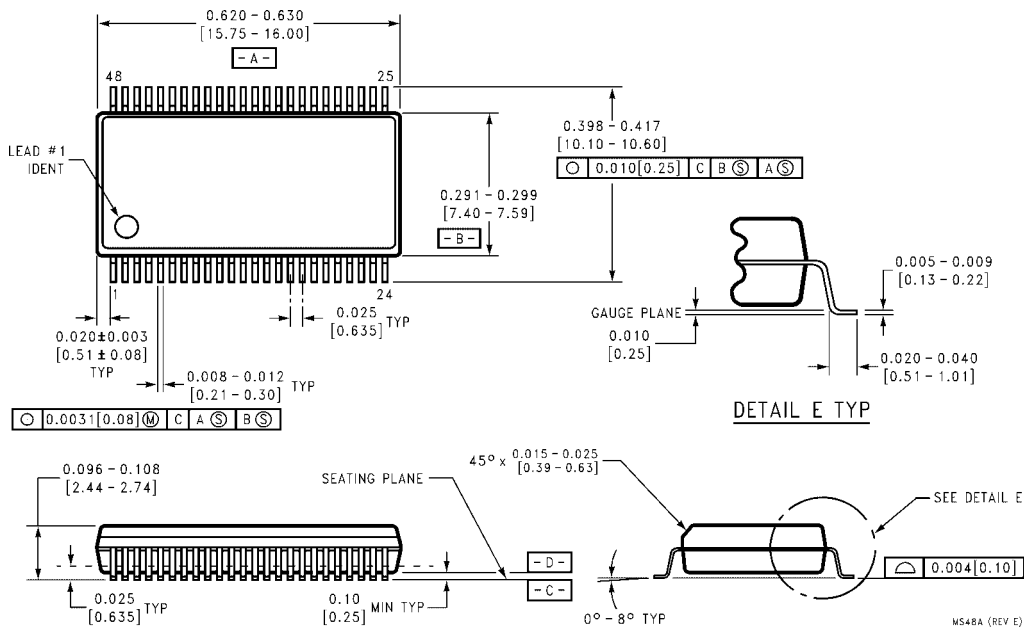


FIGURE 2. Waveforms
(Input Characteristics; $f = 1MHz$, $t_r = t_f = 3ns$)

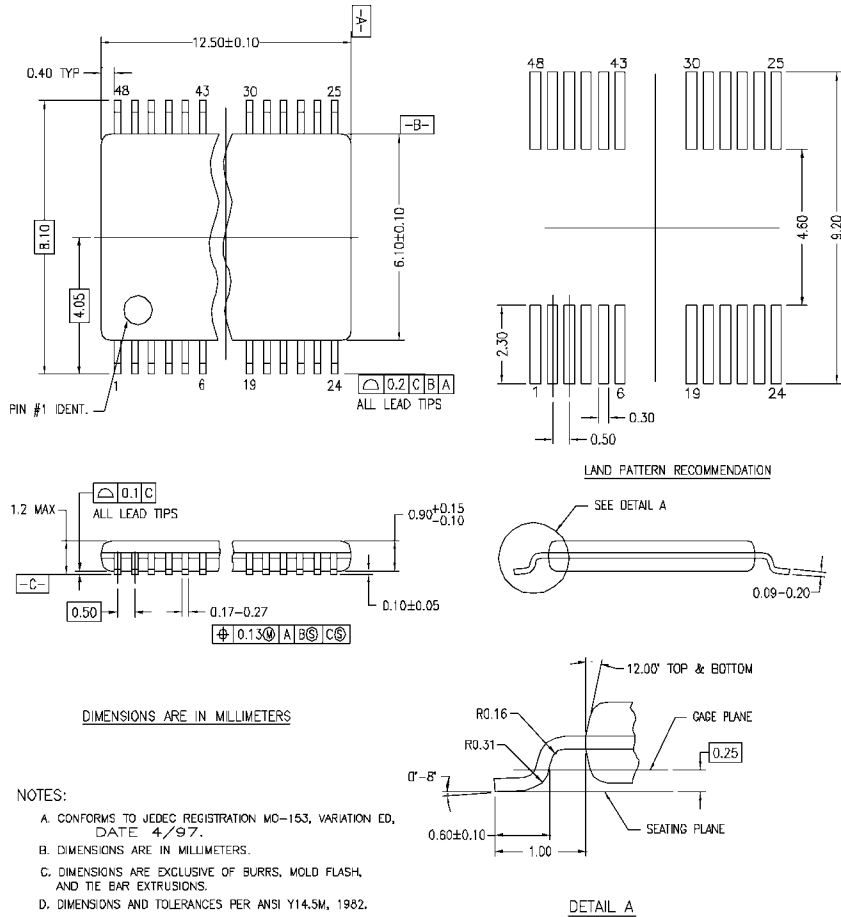
Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Physical Dimensions inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTD48REV C

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com