

## 74LVQ174 Low Voltage Hex D-Type Flip-Flop with Master Reset

### General Description

The LVQ174 is a high-speed hex D-type flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

### Features

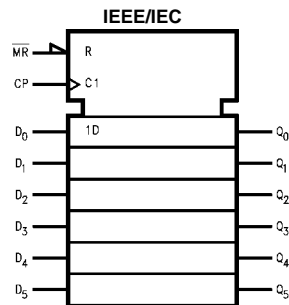
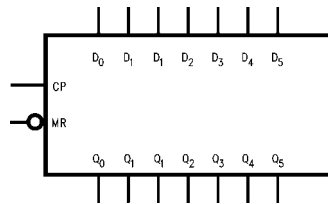
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

### Ordering Code:

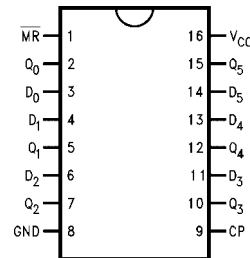
Order Number	Package Number	Package Description
74LVQ174SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVQ174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Pin Descriptions

Pin Names	Description
D <sub>0</sub> -D <sub>5</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{\text{MR}}$	Master Reset Input
Q <sub>0</sub> -Q <sub>5</sub>	Outputs

### Functional Description

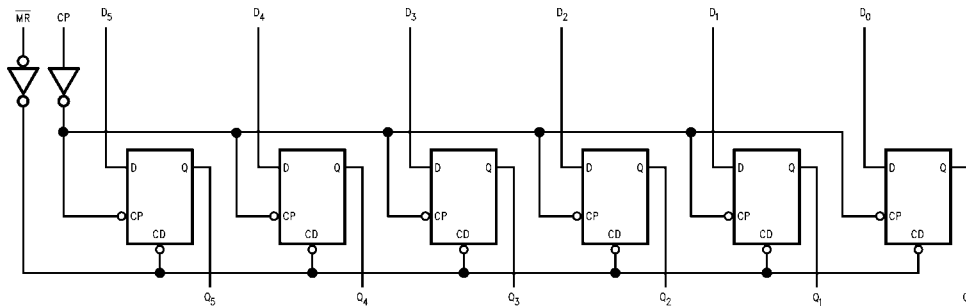
The LVQ174 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ( $\overline{MR}$ ) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ( $\overline{MR}$ ) will force all outputs LOW independent of Clock or Data inputs. The LVQ174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### Truth Table

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H	↗	H	H
H	↗	L	L
H	L	X	Q

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Transition

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)			Recommended Operating Conditions (Note 2)			
Supply Voltage ( $V_{CC}$ )		-0.5V to +7.0V	Supply Voltage ( $V_{CC}$ )			2.0V to 3.6V
DC Input Diode Current ( $I_{IK}$ )			Input Voltage ( $V_I$ )			0V to $V_{CC}$
$V_I = -0.5V$		-20 mA	Output Voltage ( $V_O$ )			0V to $V_{CC}$
$V_I = V_{CC} + 0.5V$		+20 mA	Operating Temperature ( $T_A$ )			-40°C to +85°C
DC Input Voltage ( $V_I$ )		-0.5V to $V_{CC} + 0.5V$	Minimum Input Edge Rate ( $\Delta V/\Delta t$ )			
DC Output Diode Current ( $I_{OK}$ )			$V_{IN}$ from 0.8V to 2.0V			
$V_O = -0.5V$		-20 mA	$V_{CC}$ @ 3.0V			125 mV/ns
$V_O = V_{CC} + 0.5V$		+20 mA				
DC Output Voltage ( $V_O$ )		-0.5V to $V_{CC} + 0.5V$				
DC Output Source						
or Sink Current ( $I_O$ )		$\pm 50$ mA				
DC $V_{CC}$ or Ground Current						
( $I_{CC}$ or $I_{GND}$ )		$\pm 200$ mA				
Storage Temperature ( $T_{STG}$ )		-65°C to +150°C				
DC Latch-Up Source or						
Sink Current		$\pm 100$ mA				
<b>DC Electrical Characteristics</b>						
Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits		
$V_{IH}$	Minimum High Level Input Voltage	3.0	1.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
$V_{IL}$	Maximum Low Level Input Voltage	3.0	1.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.99	2.9	V	$I_{OUT} = -50 \mu\text{A}$
		3.0		2.58	V	$V_{IN} = V_{IL}$ or $V_{IH}$ (Note 3) $I_{OH} = -12 \text{ mA}$
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.002	0.1	V	$I_{OUT} = 50 \mu\text{A}$
		3.0		0.36	V	$V_{IN} = V_{IL}$ or $V_{IH}$ (Note 3) $I_{OL} = 12 \text{ mA}$
$I_{IN}$	Maximum Input Leakage Current	3.6		$\pm 0.1$	$\mu\text{A}$	$V_I = V_{CC}$ , GND
$I_{OLD}$	Minimum Dynamic (Note 4)	3.6			mA	$V_{OLD} = 0.8V$ Max (Note 5)
$I_{OHD}$	Output Current	3.6			mA	$V_{OHD} = 2.0V$ Min (Note 5)
$I_{CC}$	Maximum Quiescent Supply Current	3.6		4.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	3.3	0.7	0.8	V	(Note 6)(Note 7)
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	3.3	-0.6	-0.8	V	(Note 6)(Note 7)
$V_{IHD}$	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0	V	(Note 6)(Note 8)
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	V	(Note 6)(Note 8)
<p><b>Note 3:</b> All outputs loaded; thresholds on input associated with output under test.</p> <p><b>Note 4:</b> Maximum test duration 2.0 ms, one output loaded at a time.</p> <p><b>Note 5:</b> Incident wave switching on transmission lines with impedances as low as 75<math>\Omega</math> for commercial temperature range is guaranteed.</p> <p><b>Note 6:</b> Worst case package.</p> <p><b>Note 7:</b> Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.</p> <p><b>Note 8:</b> Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (<math>V_{ILD}</math>), 0V to threshold (<math>V_{IHD}</math>), <math>f = 1 \text{ MHz}</math>.</p>						

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units	
			Min	Typ	Max	Min	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	2.7 3.3 ± 0.3	60 90	90 100		50 70		MHz	
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7 3.3 ± 0.3	2.0 2.0	10.8 9.0	16.2 11.5	1.5 1.5	18.0 12.5		ns
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7 3.3 ± 0.3	2.0 2.0	10.2 8.5	15.5 11.0	1.5 1.5	17.0 12.0		ns
t <sub>PHL</sub>	Propagation Delay $\overline{MR}$ to Q <sub>n</sub>	2.7 3.3 ± 0.3	2.5 2.5	10.8 9.0	16.2 11.5	2.0 2.0	18.0 12.5		ns
t <sub>OSHL</sub>	Output to	2.7		1.0	1.5		1.5		ns
t <sub>OSLH</sub>	Output Skew (Note 9)	3.3 ± 0.3		1.0	1.5		1.5		ns

**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## AC Operating Requirements

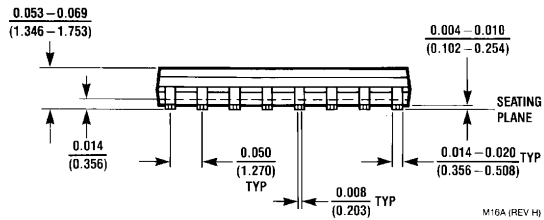
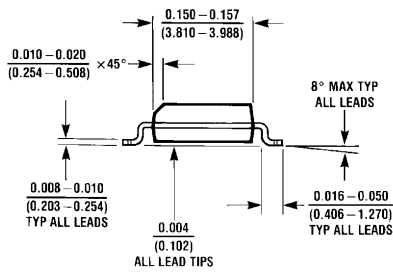
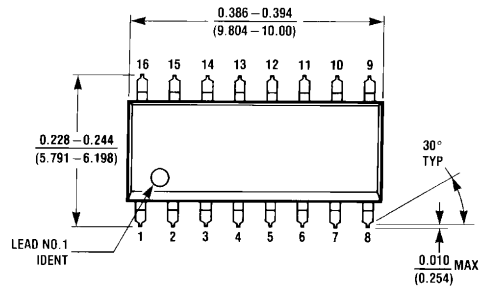
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Typ	Guaranteed Minimum			
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	2.7 3.3 ± 0.3	3.0 2.5	8.0 6.5	10.0 7.0		ns
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	2.7 3.3 ± 0.3	1.2 1.0	4.0 3.0	4.5 3.0		ns
t <sub>W</sub>	$\overline{MR}$ Pulse Width, LOW	2.7 3.3 ± 0.3	1.2 1.0	7.0 5.5	10.0 7.0		ns
t <sub>W</sub>	CP Pulse Width	2.7 3.3 ± 0.3	1.2 1.0	7.0 5.5	10.0 7.0		ns
t <sub>REC</sub>	Recovery Time MR to CP	2.7 3.3 ± 0.3	0 0	3.5 2.5	3.5 2.5		ns

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 10)	Power Dissipation Capacitance	23	pF	V <sub>CC</sub> = 3.3V

**Note 10:** C<sub>PD</sub> is measured at 10 MHz.

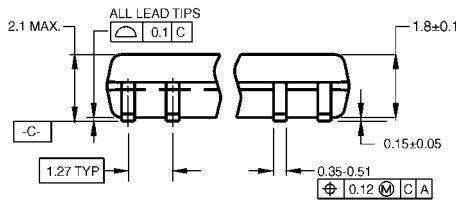
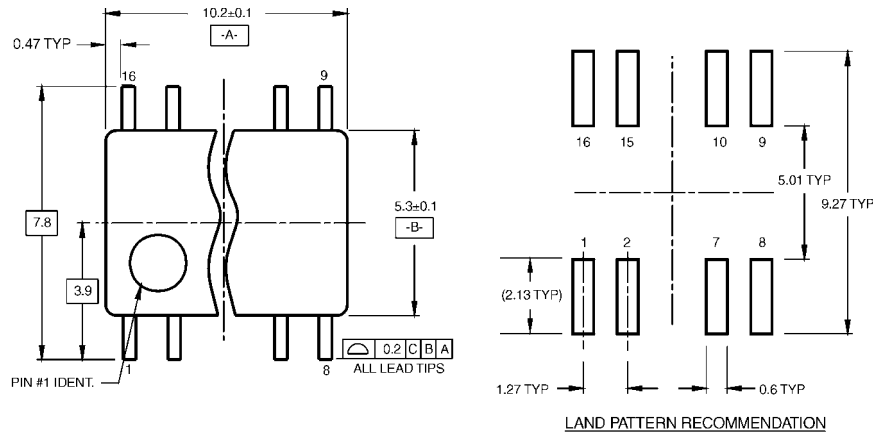
**Physical Dimensions** inches (millimeters) unless otherwise noted



M16A (REV H)

**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

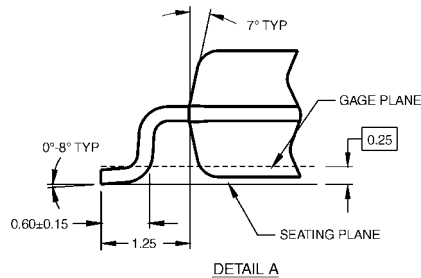
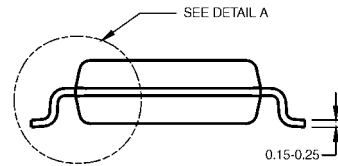


DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

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