

ADVANCE INFORMATION

March 1996

74LVXC164245 16-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs

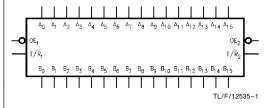
General Description

The LVXC164245 is a 48-pin dual-supply, 16-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The V $_{\rm CCB}$ pin accepts a 5V supply level. The "B" port is a dedicated 5V port. The V $_{\rm CCA}$ pin accepts a 3V-to-5V supply level. The "A" port is configured to track the V $_{\rm CCA}$ supply level respectively. A 5V level on the V $_{\rm CC}$ pin will configure the I/O pins at a 5V level and a 3V V $_{\rm CC}$ will configure the I/O pins at a 3V level. This device will allow the V $_{\rm CCA}$ voltage source pin and I/O pins on the "A" port to float when $\overline{\rm OE}$ is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

Features

- Power up/down high impedance provides glitch-free bus loading
- Allows A port and V_{CCA} to float simultaneously when OE is HIGH
- Bidirectional interface between 5V and 3V-to-5V buses
- Inputs compatible with TTL level
- Allow dual V_{CC} supplies power up/down easily when OE is HIGH
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SSOP and TSSOP packages
- Implements patented Quiet Series™ EMI reduction circuitry
- Flexible V_{CCA} operating range
- Functionally compatible with the 74 series 16245

Logic Symbol

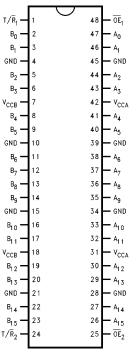


Pin Names	Description
ŌĒn	Output Enable Input (Active Low)
T/R _n	Transmit/Receive Input
A ₀ -A ₁₅	Side A Inputs/TRI-STATE Outputs
B ₀ -B ₁₅	Side B Inputs/TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVXC164245MEA	74LVXC164245MTD
	74LVXC164245MEAX	74LVXC164245MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



Functional Description

The LVXC164245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

Inputs		Outputs
ŌE ₁	T/R ₁	Juipuis
L	L	Bus B ₀ -B ₇ Data to Bus A ₀ -A ₇
L	Н	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇
Н	X	HIGH-Z State on A ₀ -A ₇ , B ₀ -B ₇

H =	: Hiah	Voltage	I eve

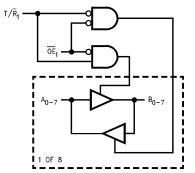
L = Low Voltage Level

Inp	Inputs Outputs	
\overline{OE}_2	T/\overline{R}_2	Outputs
L	L	Bus B ₈ -B ₁₅ Data to Bus A ₈ -A ₁₅
L	Н	Bus A ₈ -A ₁₅ Data to Bus B ₈ -B ₁₅
Н	Χ	HIGH-Z State on A_8-A_{15} , B_8-B_{15}

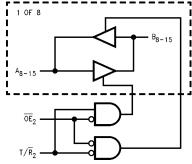
X = Immaterial

Z = High Impedance

Logic Diagrams

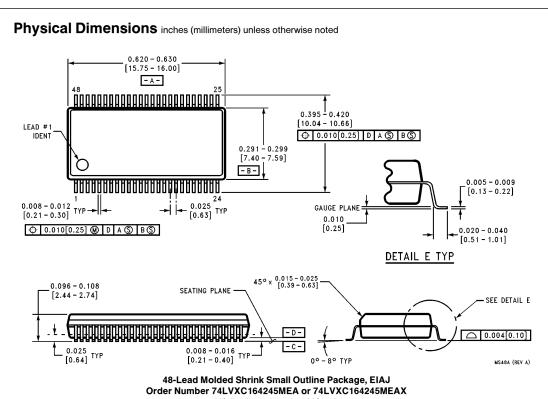






TL/F/12535-4

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.



NS Package Number MS48A

Physical Dimensions millimeters (Continued) 12.5 ± 0.1 -A-GAGE PLANE 0.25 8.1 6.1 ± 0.1 -B-SEATING PLANE 4.05 00-80 $0.60 \, \substack{+0.15 \\ -0.10}$ DETAIL A △ 0.2 C B A TYPICAL ALL LEAD TIPS SEE DETAIL A ____O.1 C - (0.90) ALL LEAD TIPS 1.1 MAX 0.09-0.20 TYP 0.10 ± 0.05 TYP ⊕ | 0.13 M | A | B S | C S |

48-Lead Molded Thin Shrink Small Outline Package, JEDEC, 6.1 mm Body Width Order Number 74LVXC164245MTD or 74LVXC164245MTDX **NS Package Number MTD48**

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MTD48 (REV A)

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