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74VCX32373 Low Voltage 32-Bit Transparent Latch with 3.6V Tolerant Inputs and Outputs (Preliminary)

## 74VCX32373 Low Voltage 32-Bit Transparent Latch with 3.6V Tolerant Inputs and Outputs (Preliminary)

### General Description

The VCX32373 contains thirty-two non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear to be transparent to the data when the Latch enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in a high impedance state.

The 74VCX32373 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The 74VCX32373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

### Features

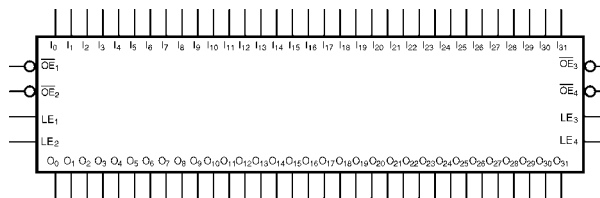
- 1.65V–3.6V  $V_{CC}$  supply operation
  - 3.6V tolerant inputs and outputs
  - $t_{PD}$  ( $I_n$  to  $O_n$ )
    - 3.0 ns max for 3.0V to 3.6V  $V_{CC}$
    - 3.4 ns max for 2.3V to 2.7V  $V_{CC}$
    - 6.8 ns max for 1.65V to 1.95V  $V_{CC}$
  - Power-off high impedance inputs and outputs
  - Support live insertion and withdrawal (Note 1)
  - Static Drive ( $I_{OH}/I_{OL}$ )
    - $\pm 24$  mA @ 3.0V  $V_{CC}$
    - $\pm 18$  mA @ 2.3V  $V_{CC}$
    - $\pm 6$  mA @ 1.65V  $V_{CC}$
  - Uses patented noise/EMI reduction circuitry
  - Latch-up performance exceeds 300 mA
  - ESD performance:
    - Human body model > 2000V
    - Machine model > 200V
  - Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)
- Note 1:** To ensure the high-impedance state during power up or power down, OE should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### Ordering Code:

Ordering Number	Package Number	Package Description
74VCX32373GX (Note 2)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]

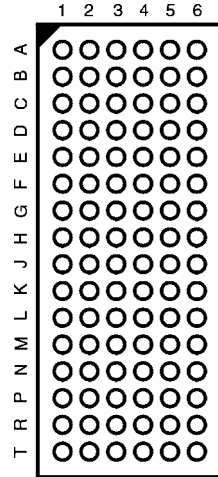
**Note 2:** BGA package available in Tape and Reel only.

### Logic Symbol



**Connection Diagram**

Pin Assignment for FBGA



(Top Thru View)

**Pin Descriptions**

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$LE_n$	Latch Enable Input
$I_0-I_{31}$	Inputs
$O_0-O_{31}$	Outputs

**FBGA Pin Assignments**

	1	2	3	4	5	6
<b>A</b>	$O_1$	$O_0$	$\overline{OE}_1$	$LE_1$	$I_0$	$I_1$
<b>B</b>	$O_3$	$O_2$	GND	GND	$I_2$	$I_3$
<b>C</b>	$O_5$	$O_4$	$V_{CC}$	$V_{CC}$	$I_4$	$I_5$
<b>D</b>	$O_7$	$O_6$	GND	GND	$I_6$	$I_7$
<b>E</b>	$O_9$	$O_8$	GND	GND	$I_8$	$I_9$
<b>F</b>	$O_{11}$	$O_{10}$	$V_{CC}$	$V_{CC}$	$I_{10}$	$I_{11}$
<b>G</b>	$O_{13}$	$O_{12}$	GND	GND	$I_{12}$	$I_{13}$
<b>H</b>	$O_{14}$	$O_{15}$	$\overline{OE}_2$	$LE_2$	$I_{15}$	$I_{14}$
<b>J</b>	$O_{17}$	$O_{16}$	$\overline{OE}_3$	$LE_3$	$I_{16}$	$I_{17}$
<b>K</b>	$O_{19}$	$O_{18}$	GND	GND	$I_{18}$	$I_{19}$
<b>L</b>	$O_{21}$	$O_{20}$	$V_{CC}$	$V_{CC}$	$I_{20}$	$I_{21}$
<b>M</b>	$O_{23}$	$O_{22}$	GND	GND	$I_{22}$	$I_{23}$
<b>N</b>	$O_{25}$	$O_{24}$	GND	GND	$I_{24}$	$I_{25}$
<b>P</b>	$O_{27}$	$O_{26}$	$V_{CC}$	$V_{CC}$	$I_{26}$	$I_{27}$
<b>R</b>	$O_{29}$	$O_{28}$	GND	GND	$I_{28}$	$I_{29}$
<b>T</b>	$O_{30}$	$O_{31}$	$\overline{OE}_4$	$LE_4$	$I_{31}$	$I_{30}$

**Truth Tables**

Inputs			Outputs
$LE_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

Inputs			Outputs
$LE_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, inputs may not float)

Inputs			Outputs
$LE_3$	$\overline{OE}_3$	$I_{16}-I_{23}$	$O_{16}-O_{23}$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

Inputs			Outputs
$LE_4$	$\overline{OE}_4$	$I_{24}-I_{31}$	$O_{24}-O_{31}$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

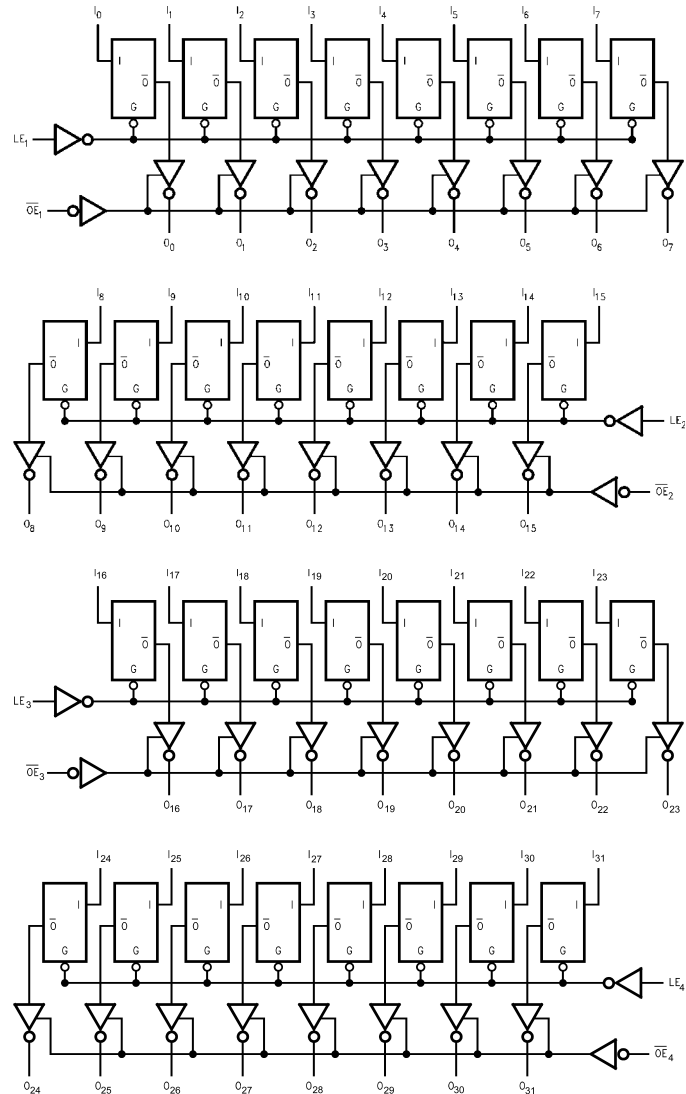
Z = High Impedance  
 $O_0$  = Previous  $O_0$  before HIGH-to-LOW of Latch Enable

### Functional Description

The 74VCX32373 contains thirty-two edge D-type latches with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 32-bit operation. The following description applies to each byte. When the Latch Enable ( $LE_n$ ) input is HIGH, data on the  $I_n$  enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time

its I input changes. When  $LE_n$  is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition on  $LE_n$ . The 3-STATE outputs are controlled by the Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW the standard outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

### Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

74VCX32373

**Absolute Maximum Ratings** (Note 3)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V
Output Voltage ( $V_O$ )	
Outputs 3-STATED	-0.5V to +4.6V
Outputs Active (Note 4)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 5)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage ( $V_O$ )	
Output in Active States	0V to $V_{CC}$
Output in "OFF" State	0.0V to 3.6V
Output Current in $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to $3.6V$	$\pm 24$ mA
$V_{CC} = 2.3V$ to $2.7V$	$\pm 18$ mA
$V_{CC} = 1.65V$ to $2.3V$	$\pm 6$ mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V

**Note 3:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 4:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 5:** Floating or unused inputs must be held HIGH or LOW.

**DC Electrical Characteristics (2.7V <  $V_{CC}$  ≤ 3.6V)**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7-3.6	2.0		V
$V_{IL}$	LOW Level Input Voltage		2.7-3.6		0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7-3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12 \text{ mA}$	2.7	2.2		V
		$I_{OH} = -18 \text{ mA}$	3.0	2.4		V
		$I_{OH} = -24 \text{ mA}$	3.0	2.2		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7-3.6		0.2	V
		$I_{OL} = 12 \text{ mA}$	2.7		0.4	V
		$I_{OL} = 18 \text{ mA}$	3.0		0.4	V
		$I_{OL} = 24 \text{ mA}$	3.0		0.55	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.7-3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	2.7-3.6		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7-3.6		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 6)	2.7-3.6		$\pm 20$	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		750	$\mu A$

**Note 6:** Outputs disabled or 3-STATE only.

DC Electrical Characteristics ( $2.3V \leq V_{CC} \leq 2.7V$ )						
Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.3 – 2.7	1.6		V
$V_{IL}$	LOW Level Input Voltage		2.3 – 2.7		0.7	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 – 2.7	$V_{CC} - 0.2$		V
		$I_{OH} = -6 \text{ mA}$	2.3	2.0		V
		$I_{OH} = -12 \text{ mA}$	2.3	1.8		V
		$I_{OH} = -18 \text{ mA}$	2.3	1.7		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 – 2.7		0.2	V
		$I_{OL} = 12 \text{ mA}$	2.3		0.4	V
		$I_{OL} = 18 \text{ mA}$	2.3		0.6	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.3 – 2.7		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	2.3 – 2.7		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 2.7		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 7)	2.3 – 2.7		$\pm 20$	$\mu A$
<b>Note 7:</b> Outputs disabled or 3-STATE only.						
DC Electrical Characteristics ( $1.65V \leq V_{CC} < 2.3V$ )						
Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		1.65 - 2.3	$0.65 \times V_{CC}$		V
$V_{IL}$	LOW Level Input Voltage		1.65 - 2.3		$0.35 \times V_{CC}$	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 2.3	$V_{CC} - 0.2$		V
		$I_{OH} = -6 \text{ mA}$	1.65	1.25		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 - 2.3		0.2	V
		$I_{OL} = 6 \text{ mA}$	1.65		0.3	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.65 - 2.3		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	1.65 - 2.3		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	1.65 - 2.3		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 8)	1.65 – 2.3		$\pm 20$	$\mu A$
<b>Note 8:</b> Outputs disabled or 3-STATE only.						

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**AC Electrical Characteristics** (Note 9)

Symbol	Parameter	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, C_L = 30 \text{ pF}, R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	
$t_{PHL}, t_{PLH}$	Propagation Delay $I_n$ to $O_n$	0.8	3.0	1.0	3.4	1.5	6.8	ns
$t_{PHL}, t_{PLH}$	Propagation Delay LE to $O_n$	0.8	3.0	1.0	3.9	1.5	7.8	ns
$t_{PZL}, t_{PZH}$	Output Enable Time	0.8	3.5	1.0	4.6	1.5	9.2	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time	0.8	3.5	1.0	3.8	1.5	6.8	ns
$t_S$	Setup Time	1.5		1.5		2.5		ns
$t_H$	Hold Time	1.0		1.0		1.0		ns
$t_W$	Pulse Width	1.5		1.5		4.0		ns

Note 9: For  $C_L = 50\text{pF}$ , add approximately 300 ps to the AC maximum specification.

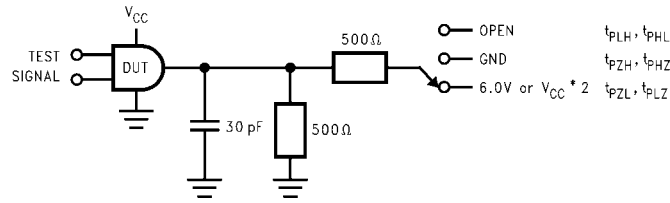
**Dynamic Switching Characteristics**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = +25^{\circ}\text{C}$	Units
				Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8 2.5 3.3	0.25 0.6 0.8	V
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8 2.5 3.3	-0.25 -0.6 -0.8	V
$V_{OHV}$	Quiet Output Dynamic Valley $V_{OH}$	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8 2.5 3.3	1.5 1.9 2.2	V

**Capacitance**

Symbol	Parameter	Conditions	$T_A = +25^{\circ}\text{C}$	Units
			Typical	
$C_{IN}$	Input Capacitance	$V_{CC} = 1.8V, 2.5V \text{ or } 3.3V, V_I = 0V \text{ or } V_{CC}$	6	pF
$C_{OUT}$	Output Capacitance	$V_I = 0V \text{ or } V_{CC}, V_{CC} = 1.8V, 2.5V \text{ or } 3.3V$	7	pF
$C_{PD}$	Power Dissipation Capacitance	$V_I = 0V \text{ or } V_{CC}, f = 10 \text{ MHz}, V_{CC} = 1.8V, 2.5V \text{ or } 3.3V$	20	pF

AC Loading and Waveforms



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V, 1.8V \pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

FIGURE 1. AC Test Circuit

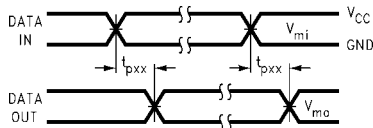


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

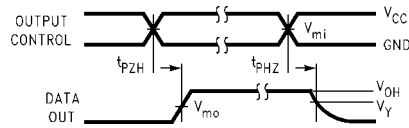


FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

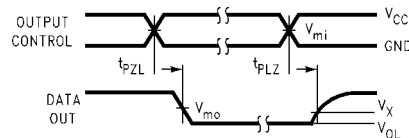


FIGURE 4. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

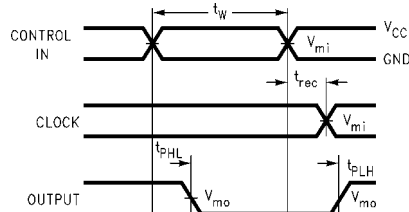


FIGURE 5. Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms

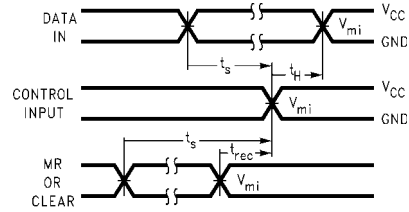


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

