

## 74VHCT138A 3-to-8 Decoder/Demultiplexer

### General Description

The VHCT138A is an advanced high speed CMOS 3-to-8 DECODER fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs ( $A_0$ ,  $A_1$  and  $A_2$ ) determine which one of the outputs ( $\overline{O}_0$ – $\overline{O}_7$ ) will go LOW. When enable input  $E_3$  is held LOW or either  $\overline{E}_1$  or  $\overline{E}_2$  is held HIGH, decoding function is inhibited and all outputs go HIGH.  $E_3$ ,  $\overline{E}_1$  and  $\overline{E}_2$  inputs are provided to ease cascade connection and for use as an address decoder for memory systems. Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the sup-

ply voltage and to the output pins with  $V_{CC} = 0V$ . These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

### Features

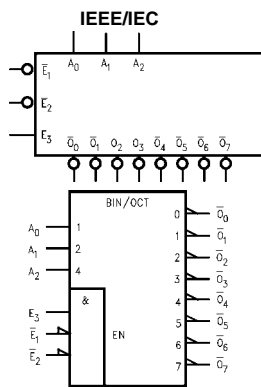
- High Speed:  $t_{PD} = 7.6$  ns (typ) at  $V_{CC} = 5V$
- Low power dissipation:  $I_{CC} = 4$   $\mu A$  (max.) at  $T_A = 25^\circ C$
- Power down protection is provided on all inputs and outputs
- Pin and function compatible with 74HCT138

### Ordering Code:

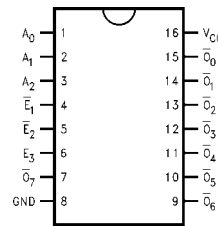
Order Number	Package Number	Package Description
74VHCT138AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74VHCT138ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT138AMTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT138AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Pin Descriptions

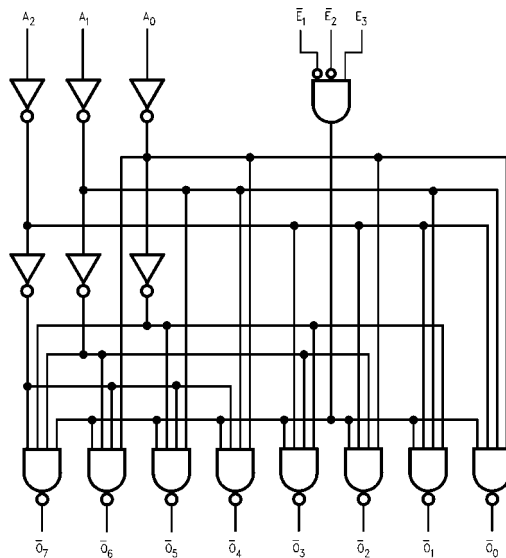
Pin Names	Description
$A_0$ – $A_2$	Address Inputs
$\overline{E}_1$ – $\overline{E}_2$	Enable Inputs
$E_3$	Enable Input
$\overline{O}_0$ – $\overline{O}_7$	Outputs

**Truth Table**

Inputs						Outputs							
$\bar{E}_1$	$\bar{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

**Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions (Note 5)	
Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V	Supply Voltage ( $V_{CC}$ )	4.5V to +5.5V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V	Input Voltage ( $V_{IN}$ )	0V to +5.5V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to 7.0V	Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
(Note 2)	-0.5V to $V_{CC} + 0.5V$	(Note 3)	0V to 5.5V
(Note 3)	-20 mA	(Note 2)	0V to 5.5V
Input Diode Current ( $I_{IK}$ )	-20 mA	Operating Temperature ( $T_{OPR}$ )	-40°C to +85°C
Output Diode Current ( $I_{OK}$ )	±20 mA	Input Rise and Fall Time ( $t_r, t_f$ )	0 – 20 ns/V
(Note 4)	±25 mA	$V_{CC} = 5.0V \pm 0.5V$	
DC Output Current ( $I_{OUT}$ )	±75 mA		
DC $V_{CC}/GND$ Current ( $I_{CC}$ )	-65°C to +150°C		
Storage Temperature ( $T_{STG}$ )	260°C		
Lead Temperature ( $T_L$ )			
(Soldering, 10 seconds)			

**Note 1:** Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

**Note 2:**  $V_{CC} = 0V$ .

**Note 3:** HIGH or LOW state.  $I_{OUT}$  absolute maximum rating must be observed.

**Note 4:**  $V_{OUT} < GND, V_{OUT} > V_{CC}$  (Outputs Active).

**Note 5:** Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

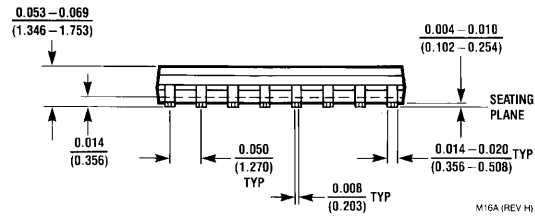
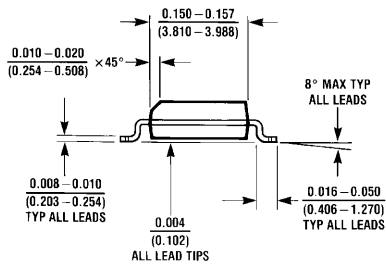
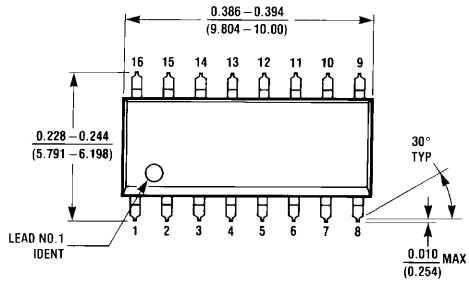
Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
$V_{IH}$	HIGH Level Input Voltage	4.5 – 5.5	2.0			2.0		V		
$V_{IL}$	LOW Level Input Voltage	4.5 – 5.5			0.8		0.8	V		
$V_{OH}$	HIGH Level	4.5	4.4	4.5		4.4		V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$ $I_{OH} = -8 \text{ mA}$
	Output Voltage	4.5	3.94			3.80				
$V_{OL}$	LOW Level	4.5		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$ $I_{OL} = 8 \text{ mA}$
	Output Voltage	4.5			0.36		0.44			
$I_{IN}$	Input Leakage Current	0 – 5.5			±0.1		±1.0	$\mu A$	$V_{IN} = 5.5V$ or GND	
$I_{CC}$	Quiescent Supply Current	5.5			4.0		20.0	$\mu A$	$V_{IN} = V_{CC}$ or GND	
$I_{CCT}$	Maximum $I_{CC}/Input$	5.5			1.35		1.50	mA	$V_{in} = 3.4V$ other inputs = $V_{CC}$ or GND	
$I_{OFF}$	Output Leakage Current	0			0.5		5.0	$\mu A$	$V_{OUT} = 5.5V$	

## AC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Typ	Max	Min	Max		
$t_{PLH}$	Propagation Delay	$5.0 \pm 0.5$		7.6	10.4	1.0	12.0	ns	$C_L = 15 \text{ pF}$
$t_{PHL}$	$A_n$ to $\bar{O}_n$			8.1	11.4	1.0	13.0		$C_L = 50 \text{ pF}$
$t_{PLH}$	Propagation Delay	$5.0 \pm 0.5$		6.6	9.1	1.0	10.5	ns	$C_L = 15 \text{ pF}$
$t_{PHL}$	$E_3$ to $\bar{O}_n$			7.1	10.1	1.0	11.5		$C_L = 50 \text{ pF}$
$t_{PLH}$	Propagation Delay	$5.0 \pm 0.5$		7.0	9.6	1.0	11.0	ns	$C_L = 15 \text{ pF}$
$t_{PHL}$	$\bar{E}_1$ or $\bar{E}_2$ to $\bar{O}_n$			7.5	10.6	1.0	12.0		$C_L = 50 \text{ pF}$
$C_{IN}$	Input Capacitance			4	10		10	pF	$V_{CC} = \text{Open}$
$C_{PD}$	Power Dissipation Capacitance			49				pF	(Note 6)

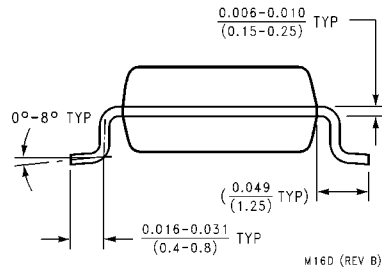
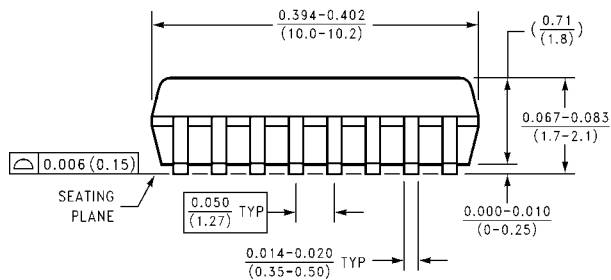
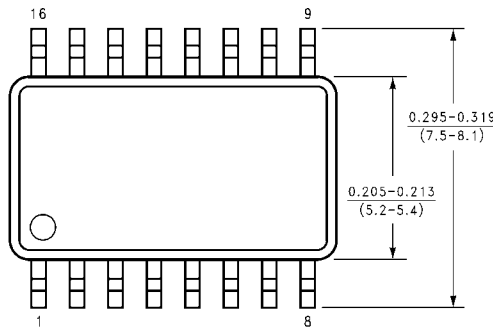
**Note 6:**  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC}(\text{opr}) = C_{PD} * V_{CC} * f_{IN} + I_{CC}$ .

**Physical Dimensions** inches (millimeters) unless otherwise noted



M16A (REV H)

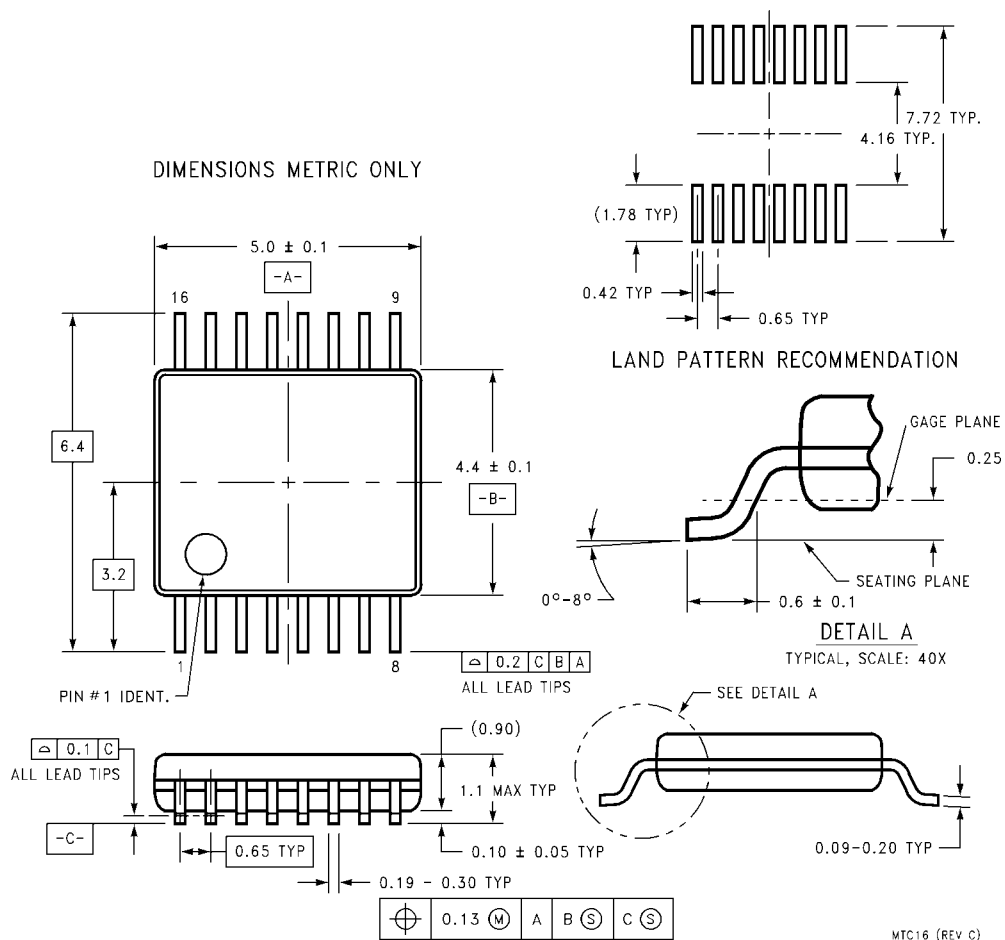
**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow  
Package Number M16A**



M16D (REV B)

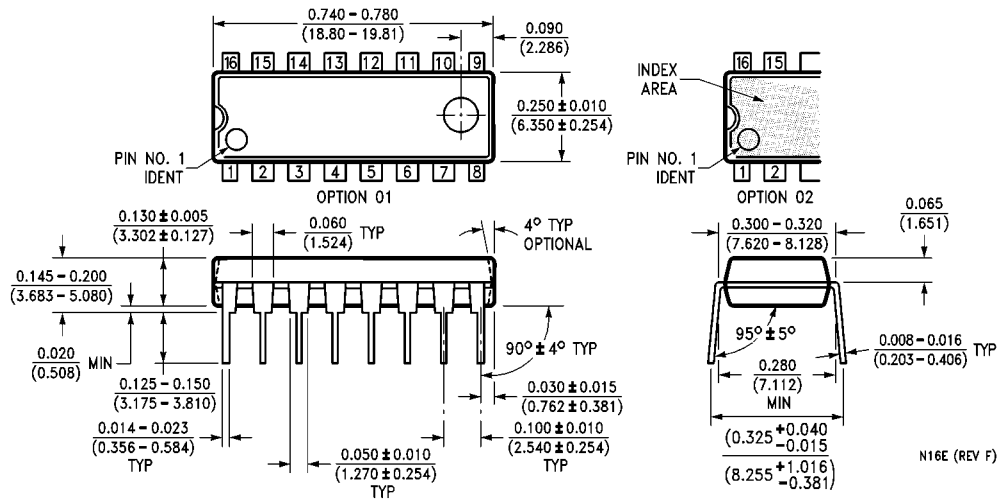
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

N16E (REV F)

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