CY7C374i

UltraLogic™ 128-Macrocell Flash CPLD

Features

- **128 macrocells in eight logic blocks**
- **64 I/O pins**
- **5 dedicated inputs including 4 clock pins**
- **In-System Reprogrammable (ISR™) Flash technology**
  - **JTAG interface**
- **Bus Hold capabilities on all I/Os and dedicated inputs**
- **No hidden delays**
- **High speed**
  - **f_{MAX} = 125 MHz**
  - **t_{PD} = 10 ns**
  - **t_S = 5.5 ns**
  - **t_{CO} = 6.5 ns**
- **Fully PCI compliant**
- **3.3V or 5.0V I/O operation**
- **Available in 84-pin PLCC, 84-pin CLCC, and 100-pin TQFP packages**
- **Pin compatible with the CY7C373i**

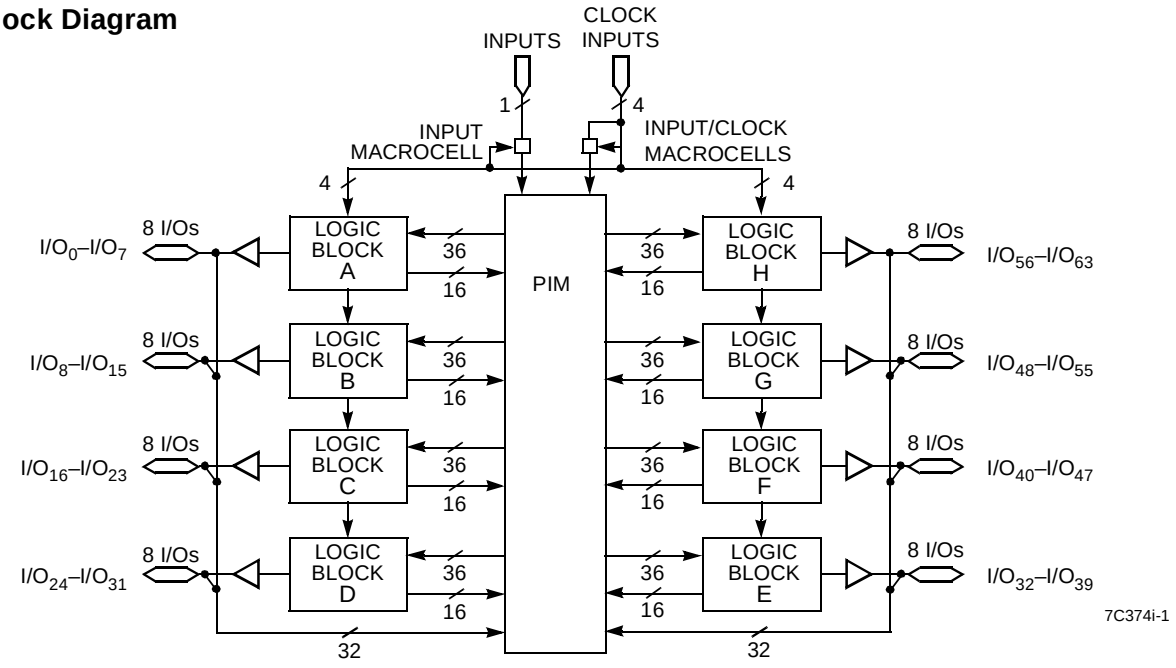
Functional Description

The CY7C374i is an In-System Reprogrammable Complex Programmable Logic Device (CPLD) and is part of the FLASH370i™ family of high-density, high-speed CPLDs. Like all members of the FLASH370i family, the CY7C374i is designed to bring the ease of use as well as PCI Local Bus Specification support and high performance of the 22V10 to high-density CPLDs.

Like all of the UltraLogic™ FLASH370i devices, the CY7C374i is electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows thereby reducing costs. The Cypress ISR function is implemented through a JTAG serial interface. Data is shifted in and out through the SDI and SDO pin. The ISR interface is enabled using the programming voltage pin (ISR_{EN}). Additionally, because of the superior routability of the FLASH370i devices, ISR often allows users to change existing logic designs while simultaneously fixing pinout assignments.

The 128 macrocells in the CY7C374i are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

Logic Block Diagram



Selection Guide

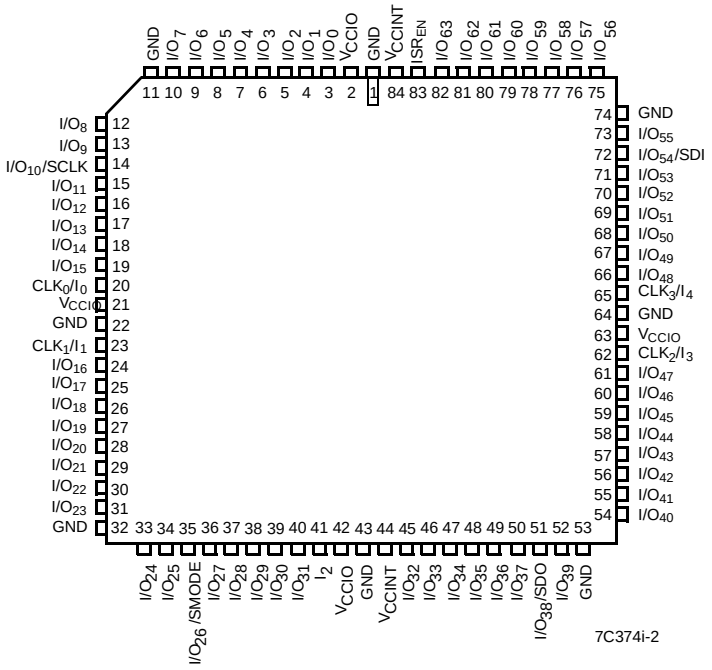
	7C374i–125	7C374i–100	7C374i–83	7C374i–66	7C374iL–66
Maximum Propagation Delay[1], t_{PD} (ns)	10	12	15	20	20
Minimum Set-Up, t_S (ns)	5.5	6	8	10	10
Maximum Clock to Output[1], t_{CO} (ns)	6.5	7	8	10	10
Typical Supply Current, I_{CC} (mA)	125	125	125	125	75

Note:

1. The 3.3V I/O mode timing adder, $t_{3.3IO}$, must be added to this specification when V_{CCIO} = 3.3V.

Pin Configurations

PLCC
Top View



7C374i-2

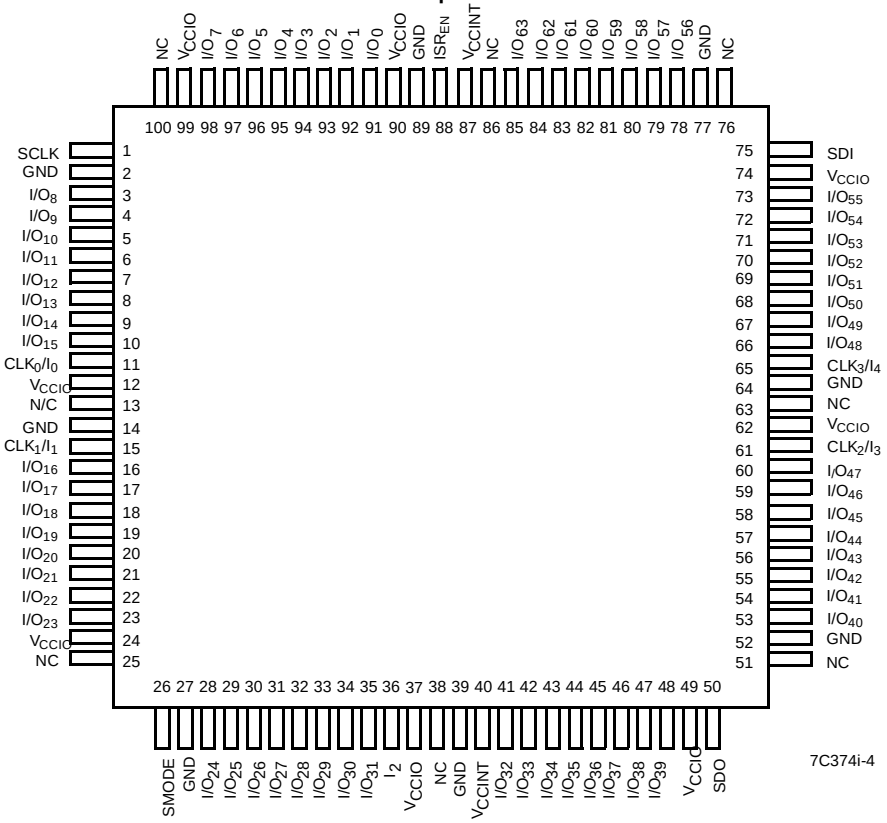
PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L	I/O_{23}	I/O_{25}	I/O_{26} SMODE	I/O_{28}	I/O_{31}	I/O_{33}	V_{CC}	I/O_{34}	I/O_{36}	I/O_{37}	I/O_{39}
K	I/O_{21}	GND	I/O_{24}	I/O_{27}	I/O_{30}	I_2	I/O_{32}	I/O_{35}	I/O_{38} SDO	GND	I/O_{41}
J	I/O_{20}	I/O_{22}			I/O_{29}	V_{CC}	GND			I/O_{40}	I/O_{42}
H	I/O_{18}	I/O_{19}								I/O_{43}	I/O_{44}
G	CLK1 /I_1	I/O_{16}	GND						CLK2 /I_3	I/O_{46}	I/O_{47}
F	I/O_{17}	CLK0 /I_0	V_{CC}						V_{CC}	I/O_{45}	GND
E	I/O_{15}	I/O_{14}	I/O_{13}						I/O_{49}	I/O_{48}	CLK3 /I_4
D	I/O_{12}	I/O_{11}								I/O_{51}	I/O_{50}
C	I/O_{10} SCLK	I/O_8	■		I/O_1	V_{CC}	ISR_{EN}			I/O_{54} SDI	I/O_{52}
B	I/O_9	GND	I/O_6	I/O_3	I/O_0	I/O_{61}	I/O_{62}	I/O_{59}	I/O_{56}	GND	I/O_{53}
A	I/O_7	I/O_5	I/O_4	I/O_2	V_{CC}	GND	I/O_{63}	I/O_{60}	I/O_{58}	I/O_{57}	I/O_{55}

7C374i–3

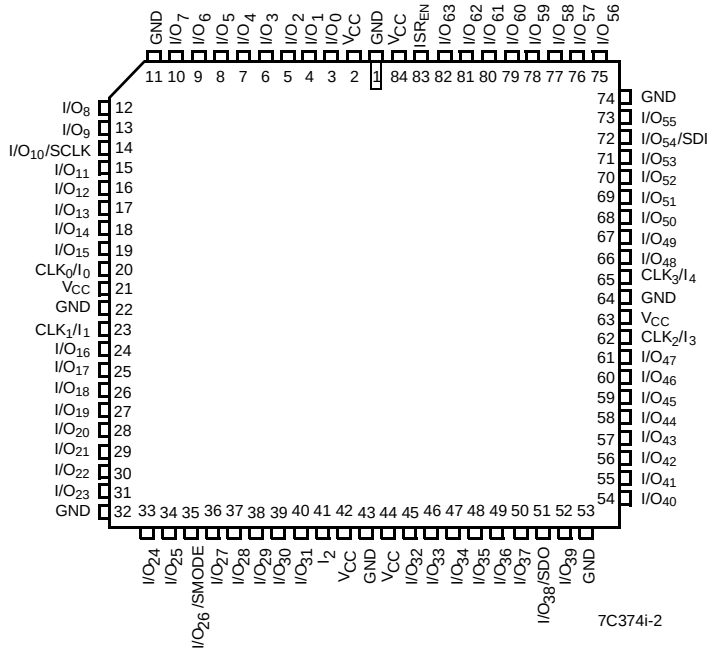
Pin Configurations (continued)

TQFP
Top View



7C374i-4

CLCC
Top View



7C374i-2

Functional Description (continued)

The logic blocks in the FLASH370i architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370i family, the CY7C374i is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 64 I/O pins on the CY7C374i. In addition, there is one dedicated input and four input/clock pins.

Finally, the CY7C374i features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C374i remain the same.

Logic Block

The number of logic blocks distinguishes the members of the FLASH370i family. The CY7C374i includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370i logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370i CPLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Half of the macrocells on the CY7C374i have I/O pins associated with them. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The I/O macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C374i to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Programming

For an overview of ISR programming, refer to the FLASH370i Family data sheet and for ISR cable and software specifications, refer to ISR data sheets. For a detailed description of ISR capabilities, refer to the Cypress application note, “An Introduction to In System Reprogramming with FLASH370i.”

PCI Compliance

The FLASH370i family of CMOS CPLDs are fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The simple and predictable timing model of FLASH370i ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without simple and predictable timing, PCI compliance is dependent upon routing and product term distribution.

3.3V or 5.0V I/O Operation

The FLASH370i family can be configured to operate in both 3.3V and 5.0V systems. All devices have two sets of VCC pins: one set, VCCINT, for internal operation and input buffers, and another set, VCCIO, for I/O output drivers. VCCINT pins must always be connected to a 5.0V power supply. However, the VCCIO pins may be connected to either a 3.3V or 5.0V power supply, depending on the output requirements. When VCCIO pins are connected to a 5.0V source, the I/O voltage levels are compatible with 5.0V systems. When VCCIO pins are connected to a 3.3V source, the input voltage levels are compatible with both 5.0V and 3.3V systems, while the output voltage levels are compatible with 3.3V systems. There will be an additional timing delay on all output buffers when operating in 3.3V I/O mode. The added flexibility of 3.3V I/O capability is available in commercial and industrial temperature ranges.

Bus Hold Capabilities on all I/Os and Dedicated Inputs

In addition to ISR capability, a new feature called bus-hold has been added to all FLASH370i I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device’s performance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND.

Design Tools

Development software for the CY7C371i is available from Cypress’s *Warp2*®, *Warp2*Sim™, and *Warp3*® software packages. All of these products are based on the IEEE-standard VHDL language. Cypress also actively supports third-party design tools from companies such as Synopsys, Mentor Graphics, Cadence, and Synario. Please refer to third-party tool support for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC} V_{CCINT}	V_{CCIO}
Commercial	0°C to +70°C	5V ± .25V	5V ± .25V OR 3.3V ± .3V
Industrial	–40°C to +85°C	5V ± .5V	5V ± .5V OR 3.3V ± .3V
Military[2]	–55°C to +125°C	5V ± .5V	

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[5]	2.4			V
			I_{OH} = –2.0 mA (Mil)				V
V_{OHZ}	Output HIGH Voltage with Output Disabled[9]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l/Ind)[5, 6]			4.0	V
			I_{OH} = –50 µA (Com'l/Ind)[5, 6]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[5]			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs[7]		2.0		7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs[7]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = Internal GND, V_I = V_{CC}		–10		+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_O = GND or V_O = V_{CC}, Output Disabled		–50		+50	µA
		V_{CC} = Max., V_O = 3.3V, Output Disabled[6]		0	–70	–125	µA
I_{OS}	Output Short Circuit Current[8, 9]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = 1 MHz, V_{IN} = GND, V_{CC}[10]	Com'l/Ind.		125	200	mA
			Com'l "L" –66		75	125	mA
			Military		125	250	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Notes:

2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. If V_{CCIO} is not specified, the device can be operating in either 3.3V or 5V I/O mode; V_{CC}=V_{CCINT}.
5. I_{OH} = –2 mA, I_{OL} = 2 mA for SDO.
6. When the I/O is three-stated, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are three-stated during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
9. Tested initially and after any design or process changes that may affect these parameters.
10. Measured with 16-bit counter programmed into each logic block.

Capacitance[9]

Parameter	Description	Test Conditions	Min.	Max.	Unit
$C_{I/O}$[11, 12]	Input Capacitance	V_{IN} = 5.0V at f=1 MHz		8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz	5	12	pF

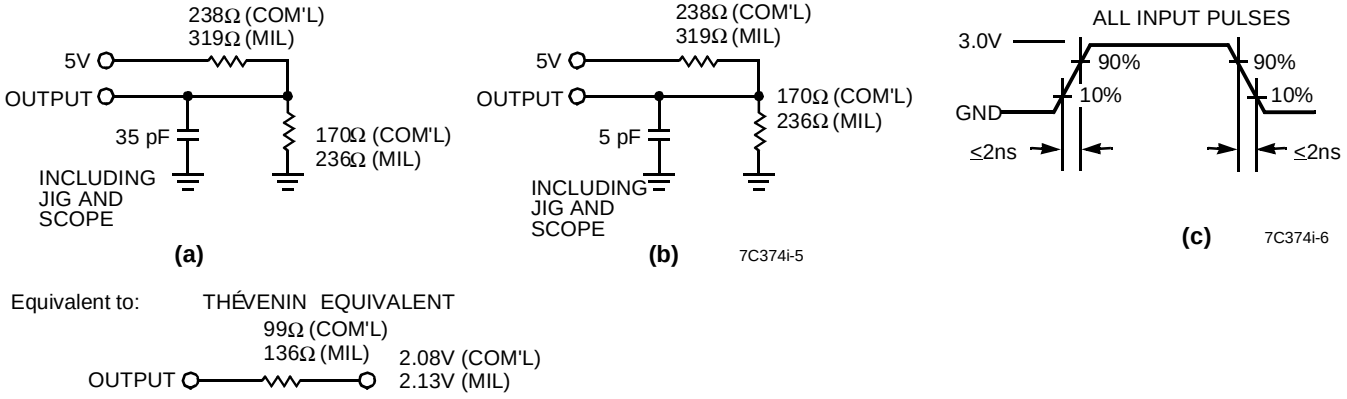
Inductance[9]

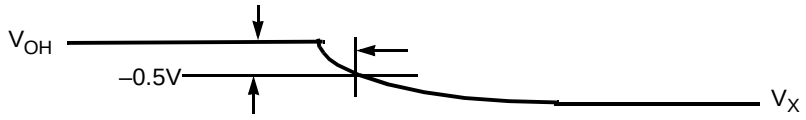
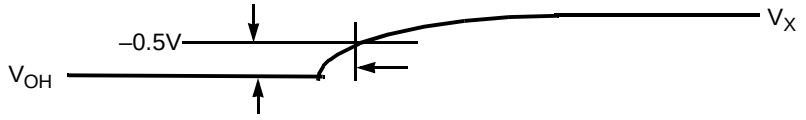
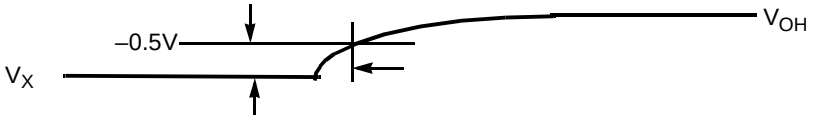
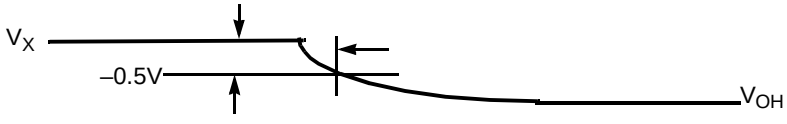
Parameter	Description	Test Conditions	100-PinTQFP	84-Lead PLCC	84-Lead CLCC	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	8	8	5	nH

Endurance Characteristics[9]

Parameter	Description	Test Conditions	Max.	Unit
N	Maximum Reprogramming Cycles	Normal Programming Conditions	100	Cycles

AC Test Loads and Waveforms



Parameter[13]	V_X	Output Waveform Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{thc}	

Notes:
11. $C_{I/O}$ for the CLCC package are 12 pF Max
12. $C_{I/O}$ for dedicated Inputs, and for I/O pins with JTAG functionality is 12 pF Max., and for ISR_{EN} is 15 pF Max.
13. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[14]

Parameter	Description	7C374i–125		7C374i–100		7C374i–83		7C374i–66 7C374iL–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Combinatorial Output[1]		10		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch[1]		13		15		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches[1]		15		16		19		24	ns
t_{EA}	Input to Output Enable[1]		14		16		19		24	ns
t_{ER}	Input to Output Disable		14		16		19		24	ns
Input Registered/Latched Mode Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time[9]	3		3		4		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[9]	3		3		4		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output[1]		14		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch[1]		16		18		21		26	ns
Output Registered/Latched Mode Parameters										
t_{CO}	Clock or Latch Enable to Output[1]		6.5		7		8		10	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	5.5		6		8		10		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)[1]		14		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	8		10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	10		12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[9]	125		100		83		66		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	158.3		143		125		100		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	83.3		76.9		67.5		50		MHz
t_{OH}–t_{IH} 37x	Output Data Stable from Output Clock Minus Input Register Hold Time for 7C37x[9, 15]	0		0		0		0		ns
Pipelined Mode Parameters										
t_{ICS}	Input Register Clock to Output Register Clock	8		10		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	125		100		83.3		66.6		MHz

Notes:

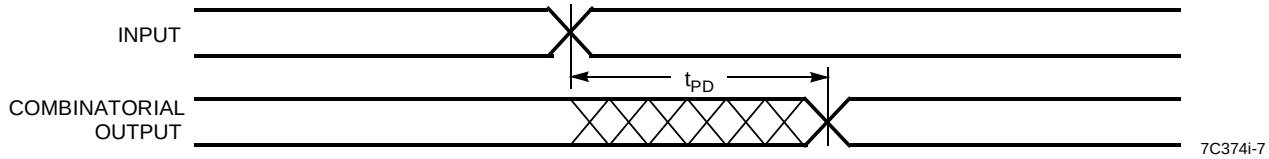
14. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
15. This specification is intended to guarantee interface compatibility of the other members of the CY7C370i family with the CY7C374i. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

Switching Characteristics Over the Operating Range[14] (continued)

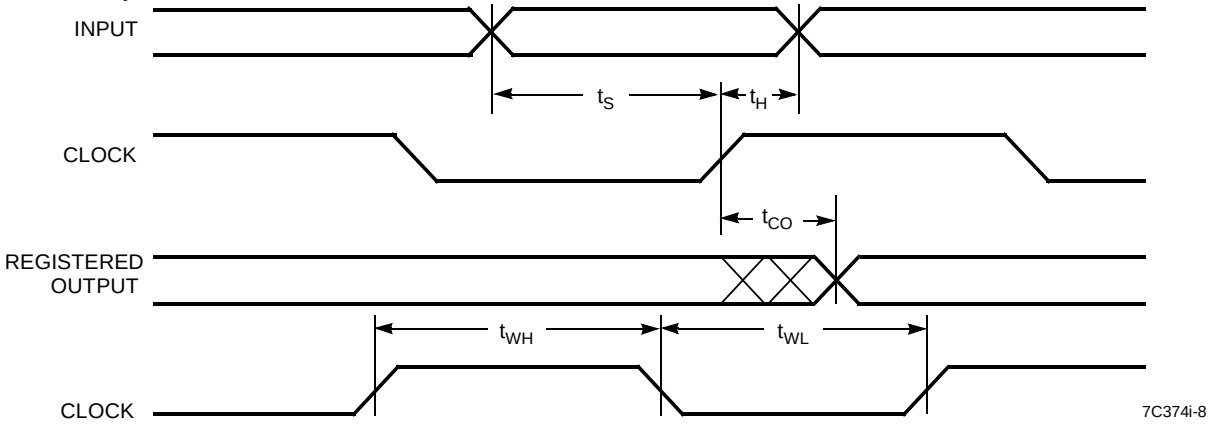
Parameter	Description	7C374i–125		7C374i–100		7C374i–83		7C374i–66 7C374iL–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width[9]	10		12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[9]	12		14		17		22		ns
t_{RO}	Asynchronous Reset to Output[1]		16		18		21		26	ns
t_{PW}	Asynchronous Preset Width[9]	10		12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[9]	12		14		17		22		ns
t_{PO}	Asynchronous Preset to Output[1]		16		18		21		26	ns
Tap Controller Parameter										
f_{TAP}	Tap Controller Frequency	500		500		500		500		kHz
3.3V I/O Mode Parameters										
$t_{3.3IO}$	3.3V I/O mode timing adder		1		1		1		1	ns

Switching Waveforms

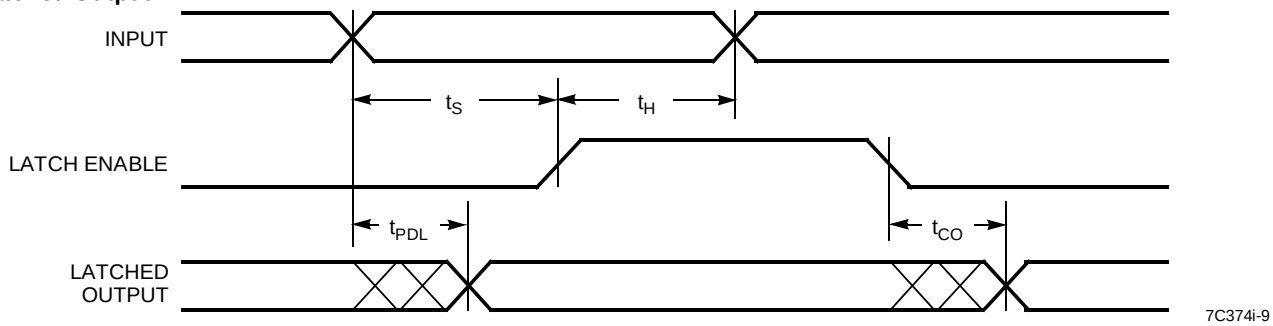
Combinatorial Output



Registered Output

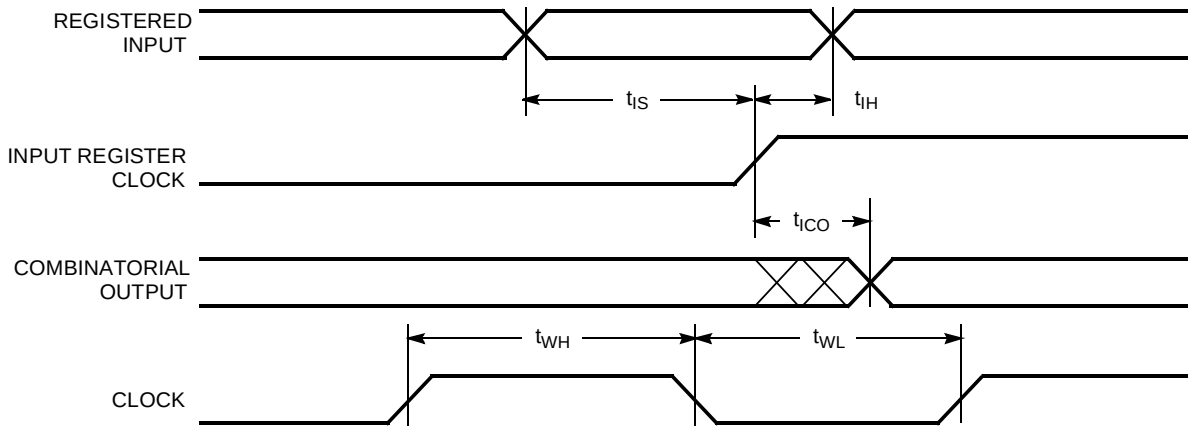


Latched Output

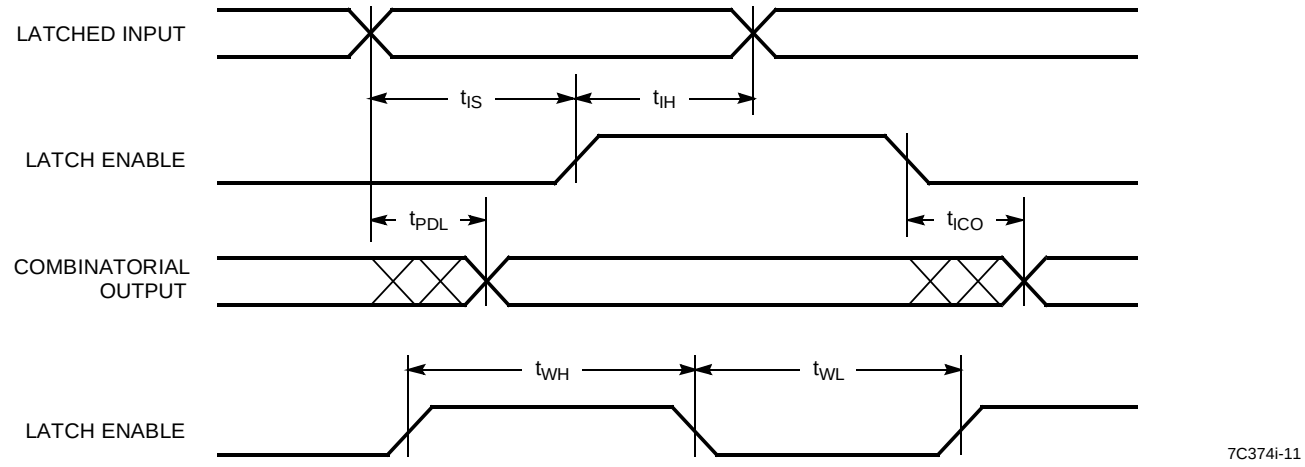


Switching Waveforms (continued)

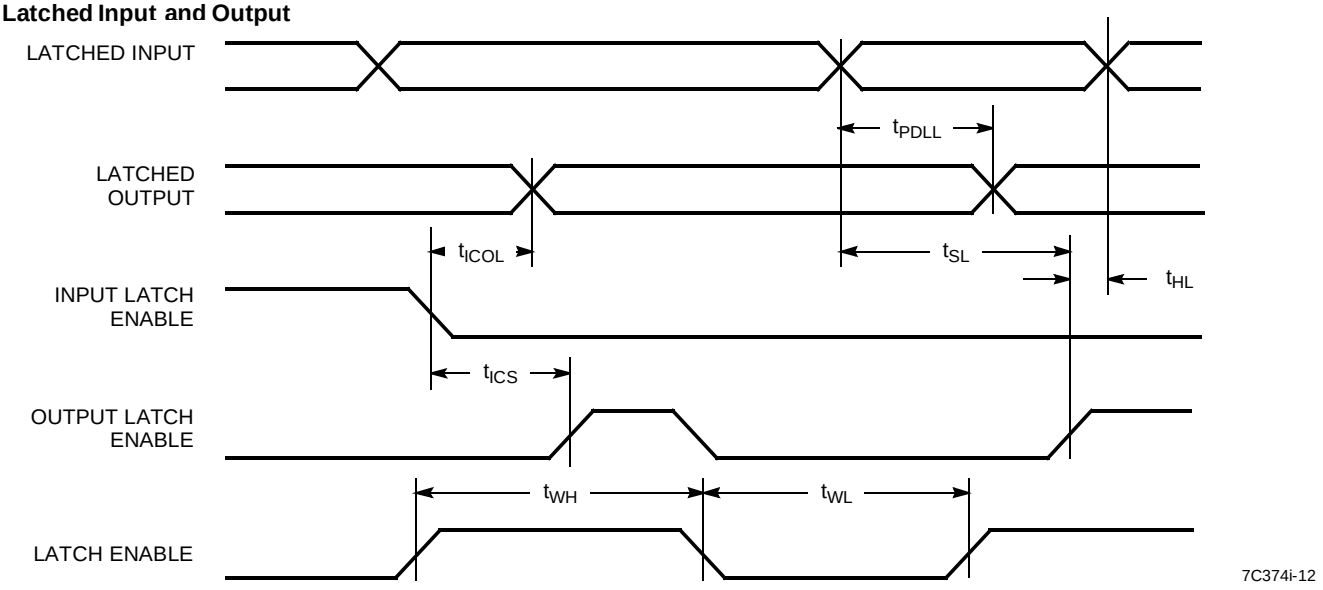
Registered Input



Latched Input

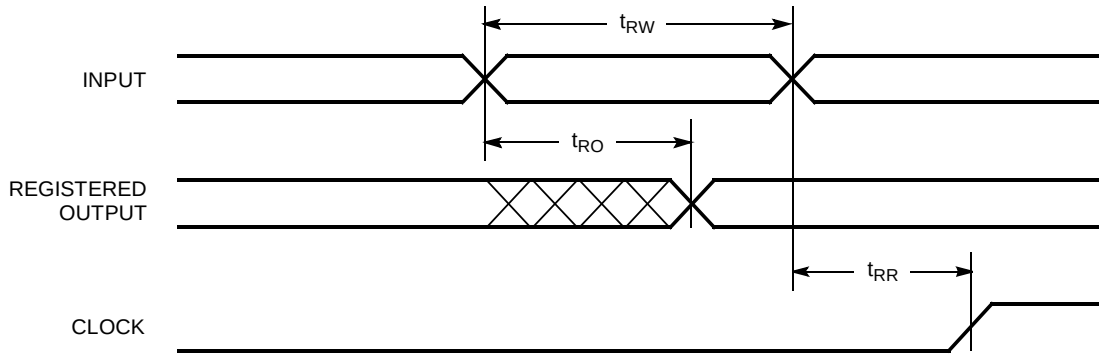


Latched Input and Output

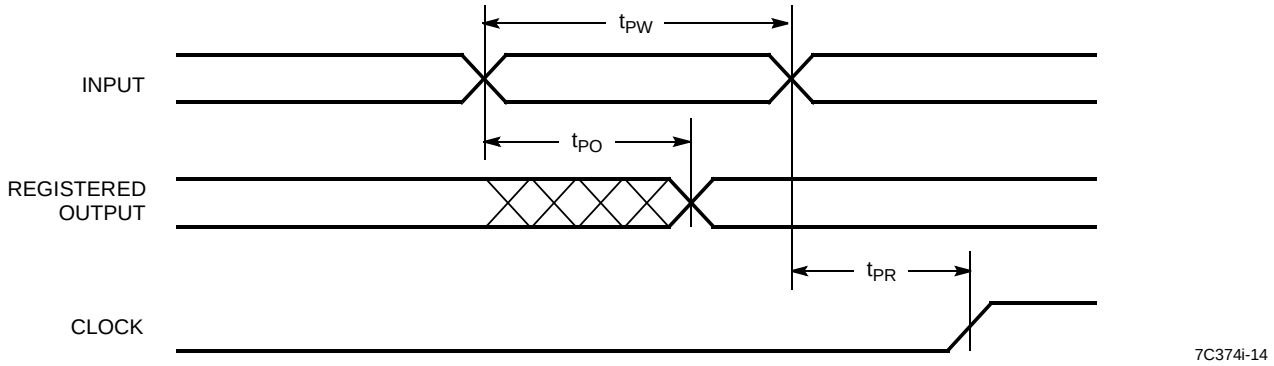


Switching Waveforms (continued)

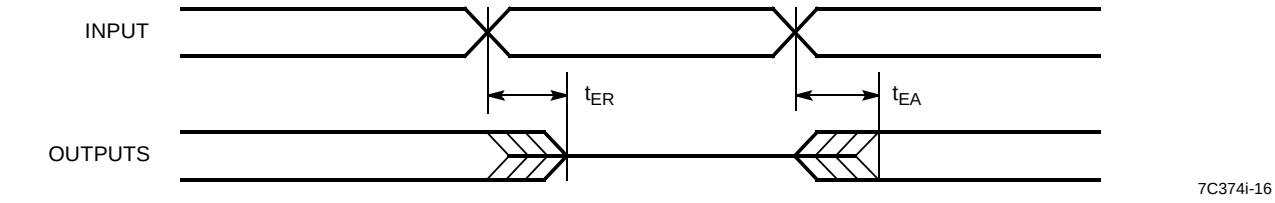
Asynchronous Reset



Asynchronous Preset



Output Enable/Disable



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
125	CY7C374i–125AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i–125JC	J83	84-Lead Plastic Leaded Chip Carrier	
100	CY7C374i–100AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i–100JC	J83	84-Lead Plastic Leaded Chip Carrier	
83	CY7C374i–83AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i–83JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i–83AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C374i–83JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i-83GMB	G84	84-Pin Ceramic Pin Grid Array	Military
	CY7C374i–83YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	
66	CY7C374i–66AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i–66JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i–66AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C374i–66JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i-66GMB	G84	84-Pin Ceramic Pin Grid Array	Military
	CY7C374i–66YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	
	CY7C374iL–66AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374iL–66JC	J83	84-Lead Plastic Leaded Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

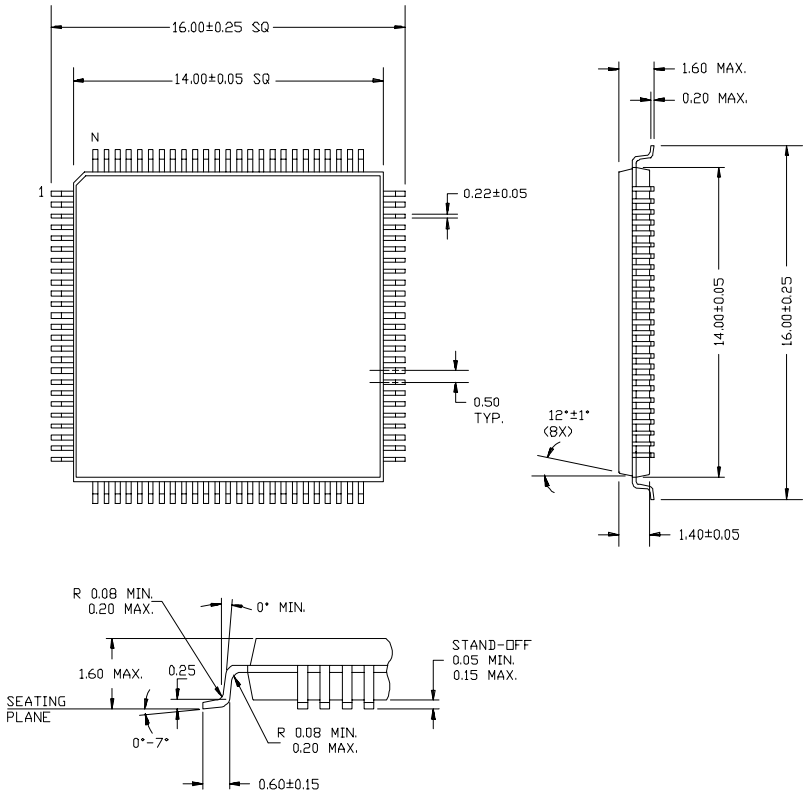
Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PDL}	9, 10, 11
t_{PDLL}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_{ICOL}	9, 10, 11
t_{S}	9, 10, 11
t_{SL}	9, 10, 11
t_{H}	9, 10, 11
t_{HL}	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11
t_{EA}	9, 10, 11
t_{ER}	9, 10, 11

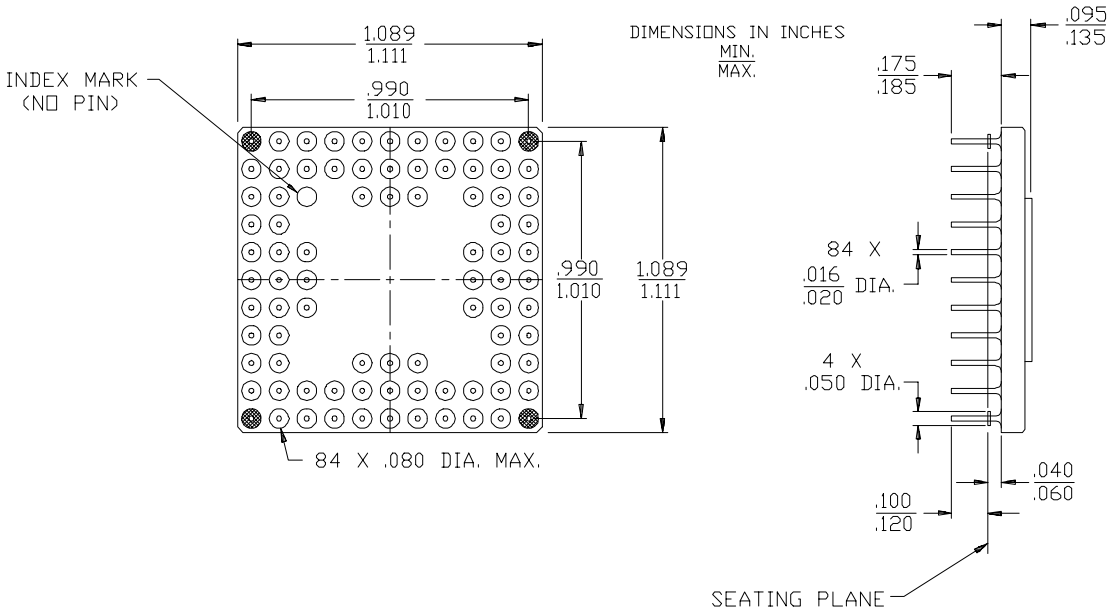
Document #: 38-00496-C

Package Diagrams

100-Pin Thin Quad Flat Pack A100

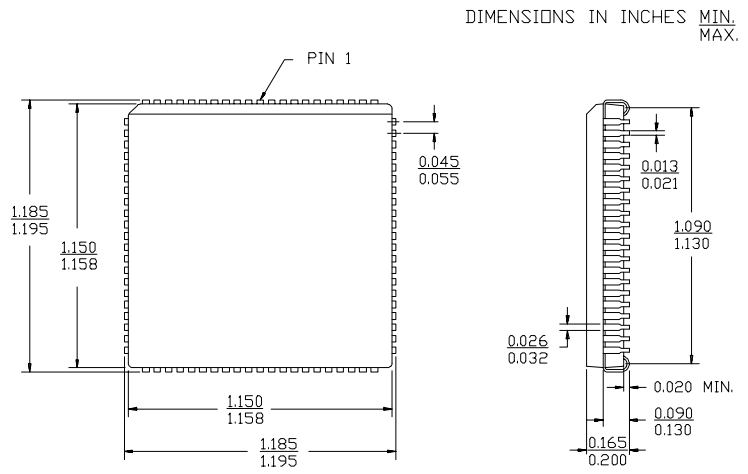


84-Pin Grid Array (Cavity Up) G84



Package Diagrams (continued)

84-Lead Plastic Leaded Chip Carrier J83



84-Pin Ceramic Leaded Chip Carrier Y84