

# DATA SHEET

## **74LVC544A**

Octal D-type registered transceiver,  
inverting (3-State)

Product specification

1998 Jul 29

# Octal D-type registered transceiver, inverting (3-State)

## 74LVC544A

### FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- Combines 74LVC640 and 74LVC533 type functions in one chip
- Octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State inverting outputs for bus oriented applications
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

### DESCRIPTION

The 74LVC544A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC544A is an octal registered inverting transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable ( $\overline{\text{LEAB}}$ ,  $\overline{\text{LEBA}}$ ) and output enable ( $\overline{\text{OEAB}}$ ,  $\overline{\text{OEBA}}$ ) inputs are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The '544A' contains eight D-type latches with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ( $\overline{\text{EAB}}$ ) input must be LOW in order to enter data from  $\overline{\text{A0}}\text{--}\overline{\text{A7}}$  or take data from  $\overline{\text{B0}}\text{--}\overline{\text{B7}}$ , as indicated in the function table.

With  $\overline{\text{EAB}}$  LOW, a LOW signal on the A-to-B latch enable ( $\overline{\text{LEAB}}$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{\text{LEAB}}$  signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With  $\overline{\text{EAB}}$  and  $\overline{\text{OEAB}}$  both LOW, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

### QUICK REFERENCE DATA

GND = 0V;  $T_{\text{amb}} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{\text{PHL}}/t_{\text{PLH}}$	Propagation delay $\overline{\text{An}}$ to $\overline{\text{Bn}}$	$C_L = 50\text{pF}$ $V_{\text{CC}} = 3.3\text{V}$	4	ns
$C_I$	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
$C_{\text{PD}}$	Power dissipation capacitance per latch	Notes 1, 2	30	pF

#### NOTES:

1.  $C_{\text{PD}}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i + \sum (C_L \times V_{\text{CC}}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{\text{CC}}$  = supply voltage in V;  
 $\sum (C_L \times V_{\text{CC}}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_I = \text{GND}$  to  $V_{\text{CC}}$ .

### ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVC544A D	74LVC544A D	SOT137-1
24-Pin Plastic SSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVC544A DB	74LVC544A DB	SOT340-1
24-Pin Plastic TSSOP Type I	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVC544A PW	74LVC544APW DH	SOT355-1

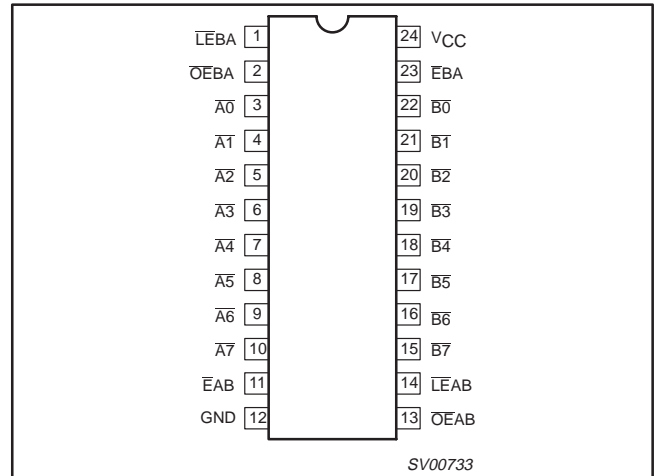
# Octal D-type registered transceiver, inverting (3-State)

74LVC544A

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{LEBA}$	'B' to 'A' latch enable input (active LOW)
2	$\overline{OEBA}$	'B' to 'A' output enable input (active LOW)
3, 4, 5, 6, 7, 8, 9, 10	$\overline{A0}-\overline{A7}$	'A' data inputs/outputs
11	$\overline{EBA}$	'B' to 'A' enable input (active LOW)
12	GND	Ground (0V)
22, 21, 20, 19, 18, 17, 16, 15	$\overline{B0}-\overline{B7}$	'B' data inputs/outputs
13	$\overline{OEAB}$	'A' to 'B' output enable input (active LOW)
14	$\overline{LEAB}$	'A' to 'B' latch enable input (active LOW)
23	$\overline{EAB}$	'A' to 'B' enable input (active LOW)
24	VCC	Positive supply voltage

## PIN CONFIGURATION



## FUNCTION TABLE

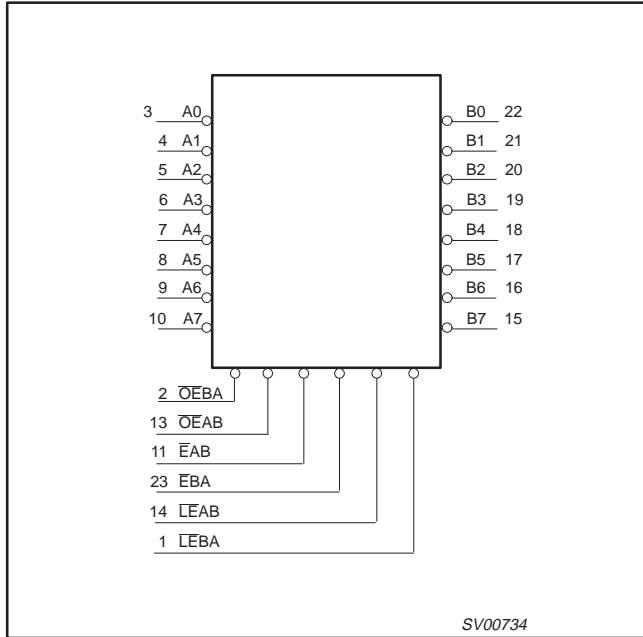
INPUTS				DATA	OUTPUTS	STATUS
$\overline{OE_{XX}}$	$\overline{E_{XX}}$	$\overline{LE_{XX}}$				
H	X	X	X		Z	Disabled
X	H	X	X		Z	Disabled
L	↑	L	h		Z	Disabled + Latch
L	↑	L	l		Z	
L	L	↑	h		L	Latch + Display
L	L	↑	l		H	
L	L	L	H		L	Transparent
L	L	L	L		H	
L	L	H	X		NC	Hold

- XX = AB for A-to-B direction, BA for B-to-A direction
- H = HIGH voltage level
- L = LOW voltage level
- h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of  $\overline{LEAB}$ ,  $\overline{LEBA}$ ,  $\overline{EAB}$ ,  $\overline{EBA}$
- l = LOW state must be present one set-up time before the LOW-to-HIGH transition of  $\overline{LEAB}$ ,  $\overline{LEBA}$ ,  $\overline{EAB}$ ,  $\overline{EBA}$
- X = Don't care
- ↑ = LOW-to-HIGH level transition
- NC = No change
- Z = High impedance OFF-state

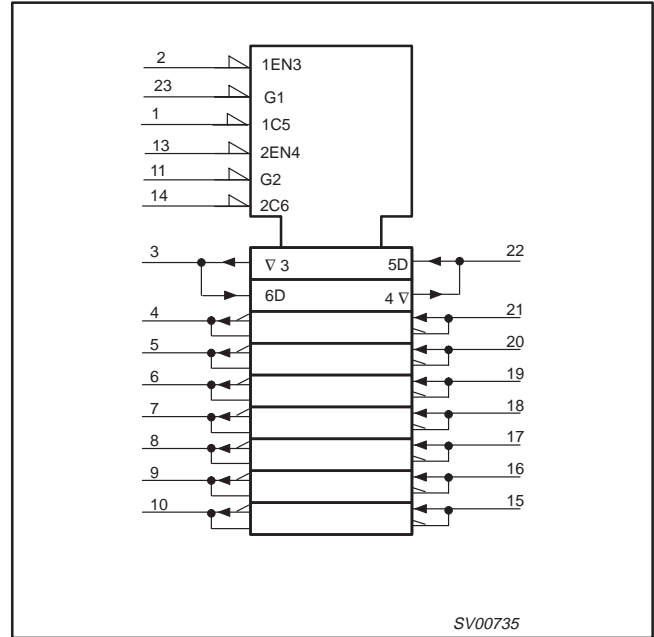
# Octal D-type registered transceiver, inverting (3-State)

74LVC544A

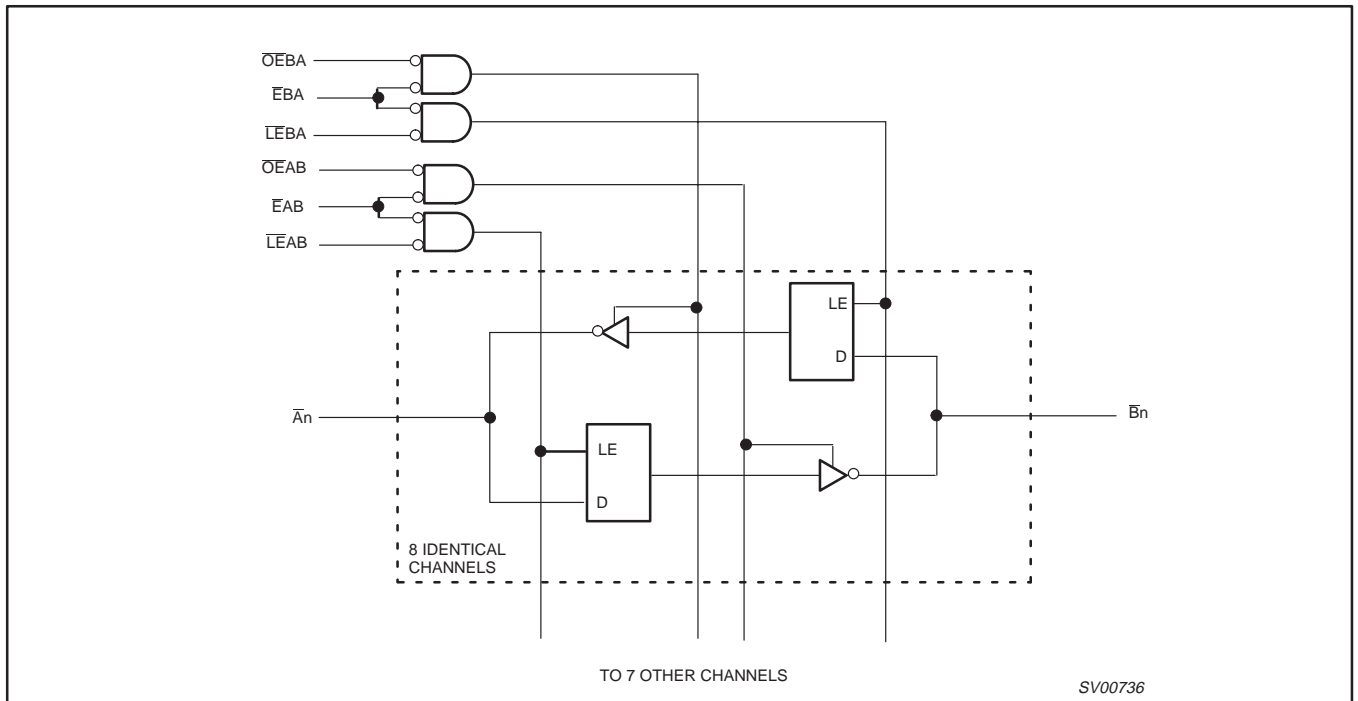
## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM



# Octal D-type registered transceiver, inverting (3-State)

74LVC544A

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V <sub>I</sub>	DC input voltage range		0	5.5	V
V <sub>O</sub>	DC output voltage range; output HIGH or LOW state		0	V <sub>CC</sub>	V
	DC output voltage range; output 3-State		0	5.5	
T <sub>amb</sub>	Operating free-air temperature range		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7V V <sub>CC</sub> = 2.7 to 3.6V	0	20 10	ns/V

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +6.5	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage	Note 2	-0.5 to +6.5	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	± 50	mA
V <sub>O</sub>	DC output voltage; output HIGH or LOW	Note 2	-0.5 to V <sub>CC</sub> +0.5	V
	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	V
I <sub>O</sub>	DC output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	± 50	mA
I <sub>GND</sub> , I <sub>CC</sub>	DC V <sub>CC</sub> or GND current		± 100	mA
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C
P <sub>TOT</sub>	Power dissipation per package			
	– plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# Octal D-type registered transceiver, inverting (3-State)

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA	V <sub>CC</sub> - 0.6			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 0.8			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND		±0.1	±5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5V or GND		0.1	±5	μA
I <sub>OFF</sub>	Power off leakage current	V <sub>CC</sub> = 0.0V; V <sub>I</sub> = 5.5V; V <sub>O</sub> = 5.5V		0.1	±10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	10	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	μA

### NOTES:

1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

## AC CHARACTERISTICS

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V <sub>CC</sub> = 3.3V ±0.3V			V <sub>CC</sub> = 2.7V		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay Ā <sub>n</sub> to B <sub>n</sub> , B <sub>n</sub> to Ā <sub>n</sub>	Figures 1, 5	1.5	4	6.5	1.5	7.5	ns
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay ĒEBA to Ā <sub>n</sub> , ĒEAB to B <sub>n</sub>	Figures 2, 5	1.5	4.3	7.5	1.5	8.5	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-State output enable time ĒEBA to Ā <sub>n</sub> , ĒEAB to B <sub>n</sub>	Figures 3, 5	1.5	4.5	8.5	1.5	9.5	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-State output disable time ĒEBA to Ā <sub>n</sub> , ĒEAB to B <sub>n</sub>	Figures 3, 5	1.5	3.9	6.5	1.5	7.5	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-State output enable time ĒEBA to Ā <sub>n</sub> , ĒEAB to B <sub>n</sub>	Figures 3, 5	1.5	4.7	8.9	1.5	9.9	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-State output disable time ĒEBA to Ā <sub>n</sub> , ĒEAB to B <sub>n</sub>	Figures 3, 5	1.5	3.9	6.9	1.5	7.9	ns
t <sub>W</sub>	LEXX pulse width HIGH	Figure 2	2.0	–	–	2.0	–	ns
t <sub>su</sub>	Set-up time Ā <sub>n</sub> /B <sub>n</sub> to LEXX, Ā <sub>n</sub> /B <sub>n</sub> to EXX	Figure 4	2.0	–	–	2.0	–	ns
t <sub>h</sub>	Hold time Ā <sub>n</sub> /B <sub>n</sub> to LEXX, Ā <sub>n</sub> /B <sub>n</sub> to EXX	Figure 4	4.0	–	–	1.0	–	ns

### NOTE:

1. These typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

# Octal D-type registered transceiver, inverting (3-State)

74LVC544A

## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$   
 $V_M = 0.5V \cdot V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$   
 $V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$   
 $V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7V$

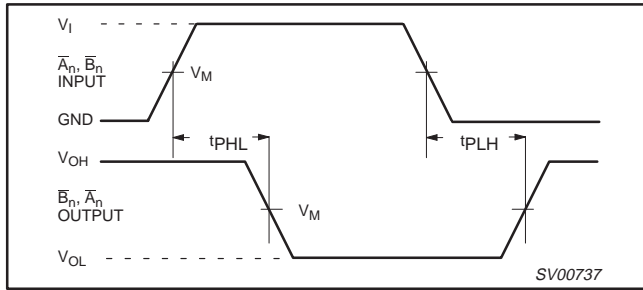


Figure 1. Input ( $\bar{A}_n, \bar{B}_n$ ) to output ( $\bar{B}_n, \bar{A}_n$ ) propagation delays.

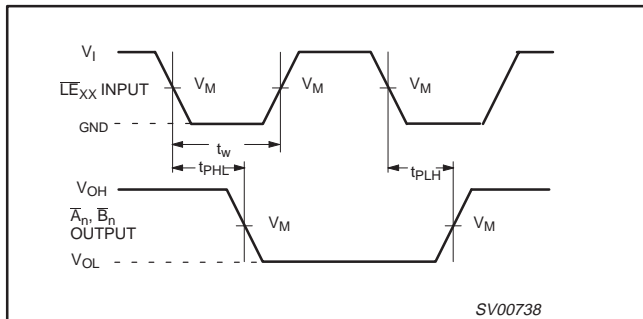


Figure 2. Latch enable input ( $\bar{L}_{EXX}$ ) pulse width, the latch enable input to output ( $\bar{A}_n, \bar{B}_n$ ) propagation delays.

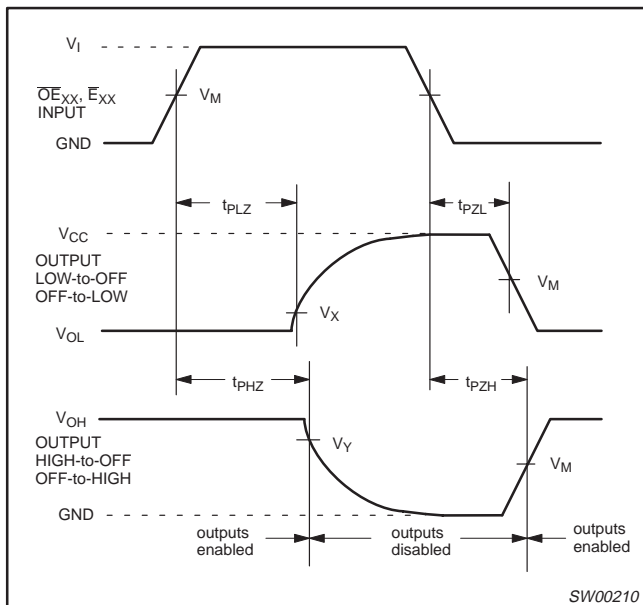


Figure 3. 3-State enable and disable times

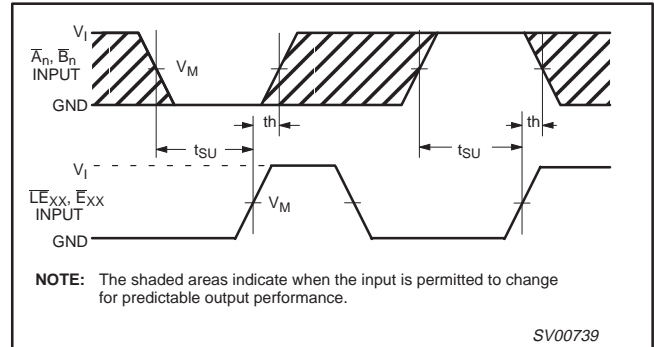


Figure 4. Data set-up and hold times for the ( $\bar{A}_n, \bar{B}_n$ ) input to the  $\bar{L}_{EXX}$  and  $E_{XX}$  inputs

## TEST CIRCUIT

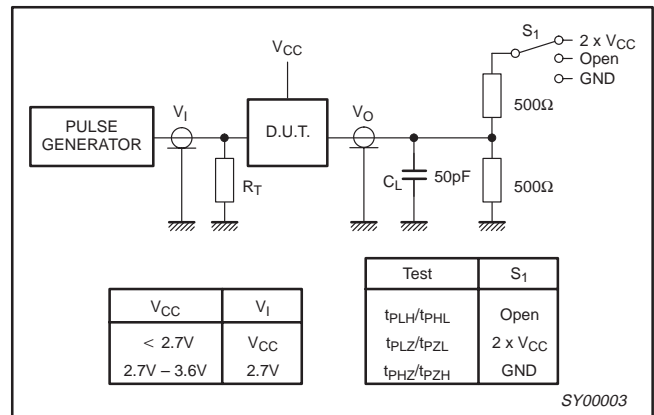


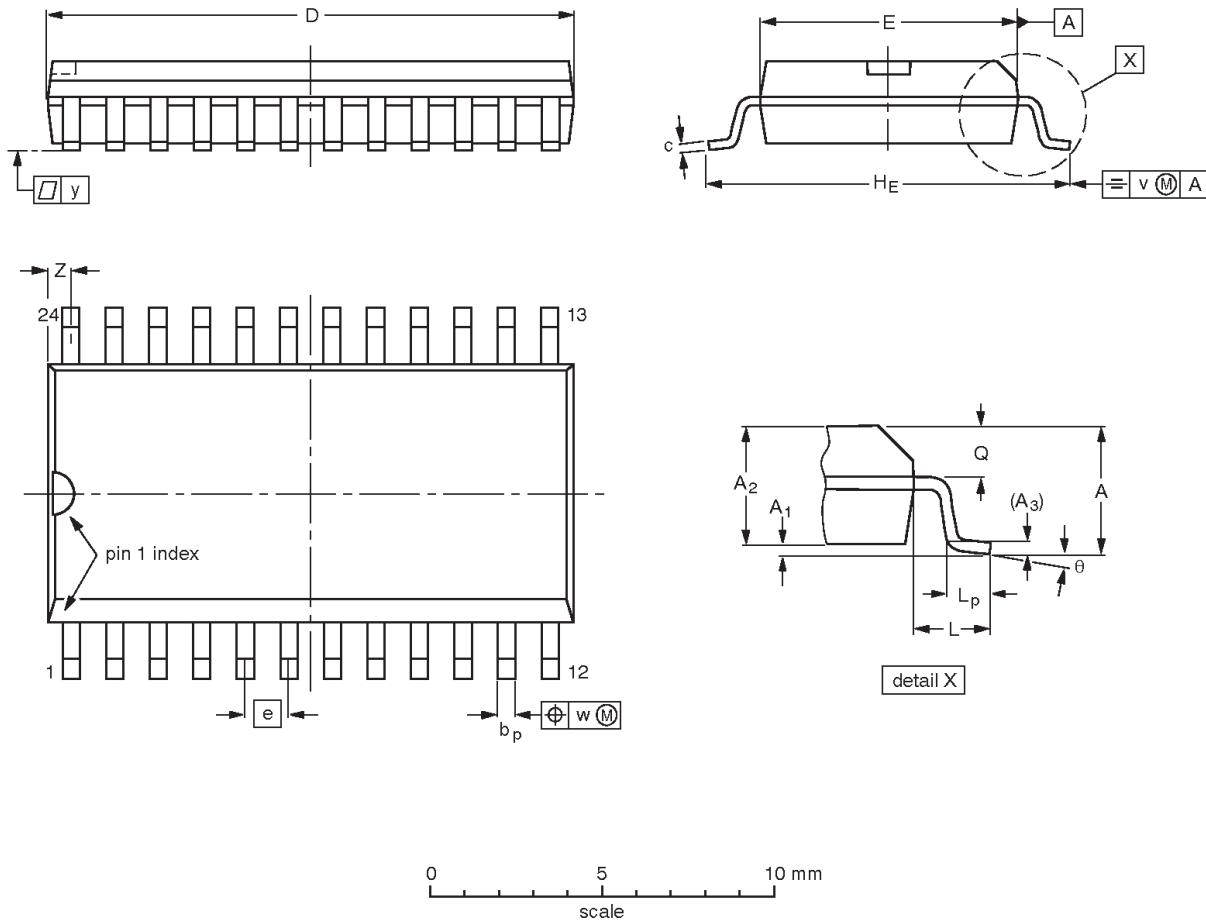
Figure 5. Load circuitry for switching times

# Octal D-type registered transceiver, inverting (3-State)

## 74LVC544A

**SO24:** plastic small outline package; 24 leads; body width 7.5 mm

**SOT137-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

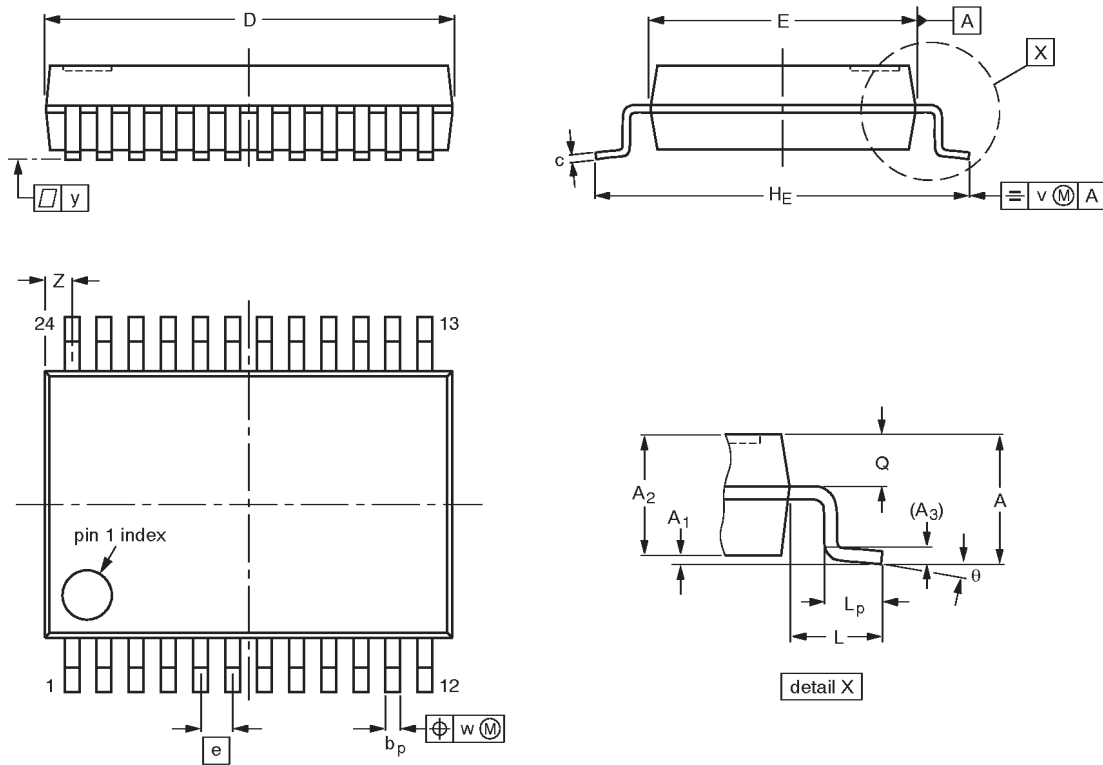


# Octal D-type registered transceiver, inverting (3-State)

74LVC544A

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

# Octal D-type registered transceiver, inverting (3-State)

74LVC544A

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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print code

Date of release: 08-98

Document order number:

9397-750-04512

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