

DATA SHEET

80C652/83C652

CMOS single-chip 8-bit microcontrollers

Product specification
Supersedes data of 1996 Aug 15
IC20 Data Handbook

1997 Dec 05

CMOS single-chip 8-bit microcontrollers

80C652/83C652

DESCRIPTION

The P80C652/83C652 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 80C652/83C652 has the same instruction set as the 80C51. Three versions of the derivative exist:

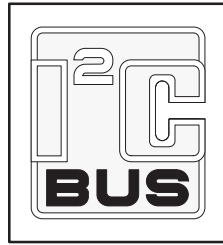
83C652 — 8k bytes mask programmable ROM

80C652 — ROMless version

87C652 — EPROM version (described in a separate chapter)

This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XC652 contains a non-volatile 8k × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I²C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC652 can be expanded using standard TTL compatible memories and logic.

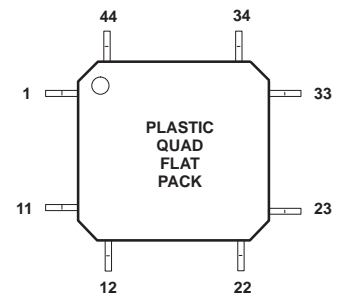
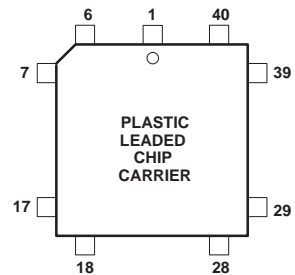
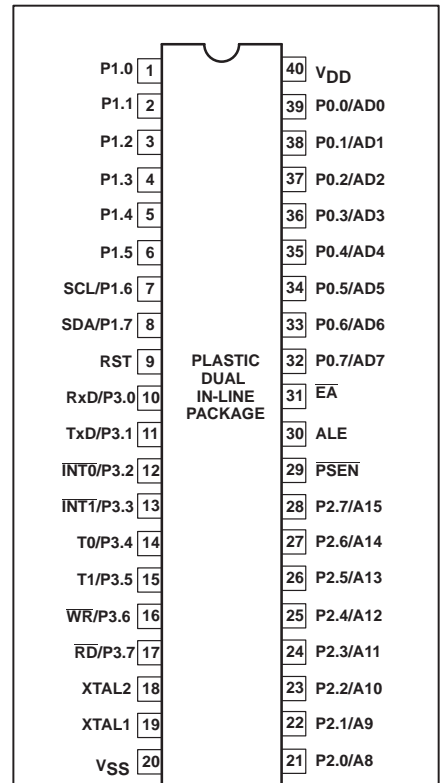
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16(24)MHz crystal, 58% of the instructions are executed in 0.75(0.5)μs and 40% in 1.5(1)μs. Multiply and divide instructions require 3(2)μs.



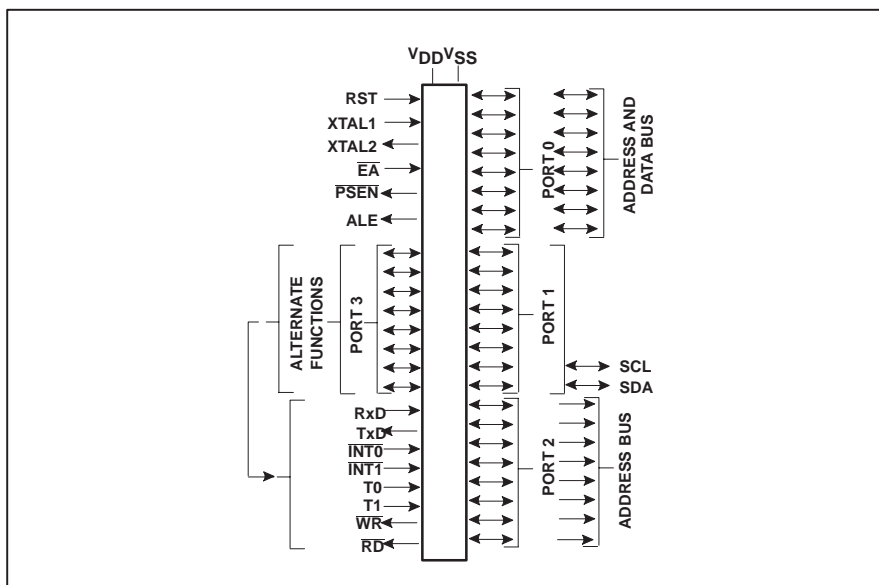
FEATURES

- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
 - Idle mode
 - Power-down mode
- ROM code protection
- Extended frequency range: 3.5 to 24 MHz
 - 0 to +70°C
 - 40 to +85°C
 - 40 to +125°C
- Three operating ambient temperature ranges:

PIN CONFIGURATIONS



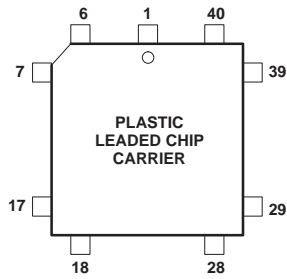
LOGIC SYMBOL



CMOS single-chip 8-bit microcontrollers

80C652/83C652

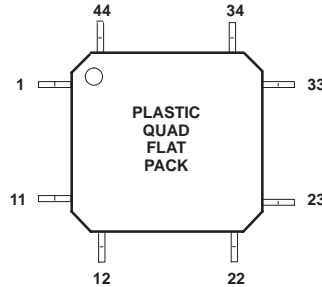
PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



| Pin | Function | Pin | Function |
|-----|-----------|-----|----------|
| 1 | NC* | 23 | NC* |
| 2 | P1.0 | 24 | P2.0/A8 |
| 3 | P1.1 | 25 | P2.1/A9 |
| 4 | P1.2 | 26 | P2.2/A10 |
| 5 | P1.3 | 27 | P2.3/A11 |
| 6 | P1.4 | 28 | P2.4/A12 |
| 7 | P1.5 | 29 | P2.5/A13 |
| 8 | P1.6/SCL | 30 | P2.6/A14 |
| 9 | P1.7/SDA | 31 | P2.7/A15 |
| 10 | RST | 32 | PSEN |
| 11 | P3.0/RxD | 33 | ALE |
| 12 | NC* | 34 | NC* |
| 13 | P3.1/TxD | 35 | EA |
| 14 | P3.2/INT0 | 36 | P0.7/AD7 |
| 15 | P3.3/INT1 | 37 | P0.6/AD6 |
| 16 | P3.4/T0 | 38 | P0.5/AD5 |
| 17 | P3.5/T1 | 39 | P0.4/AD4 |
| 18 | P3.6/WR | 40 | P0.3/AD3 |
| 19 | P3.7/RD | 41 | P0.2/AD2 |
| 20 | XTAL2 | 42 | P0.1/AD1 |
| 21 | XTAL1 | 43 | P0.0/AD0 |
| 22 | VSS | 44 | VDD |

*DO NOT CONNECT

PLASTIC QUAD FLAT PACK PIN FUNCTIONS



| Pin | Function | Pin | Function |
|-----|-----------|-----|----------|
| 1 | P1.5 | 23 | P2.5/A13 |
| 2 | P1.6/SCL | 24 | P2.6/A14 |
| 3 | P1.7/SDA | 25 | P2.7/A15 |
| 4 | RST | 26 | PSEN |
| 5 | P3.0/RxD | 27 | ALE |
| 6 | VSS4 | 28 | VSS2 |
| 7 | P3.1/TxD | 29 | EA/VPP |
| 8 | P3.2/INT0 | 30 | P0.7/AD7 |
| 9 | P3.3/INT1 | 31 | P0.6/AD6 |
| 10 | P3.4/T0 | 32 | P0.5/AD5 |
| 11 | P3.5/T1 | 33 | P0.4/AD4 |
| 12 | P3.6/WR | 34 | P0.3/AD3 |
| 13 | P3.7/RD | 35 | P0.2/AD2 |
| 14 | XTAL2 | 36 | P0.1/AD1 |
| 15 | XTAL1 | 37 | P0.0/AD0 |
| 16 | VSS1 | 38 | VDD |
| 17 | NC* | 39 | VSS3 |
| 18 | P2.0/A8 | 40 | P1.0 |
| 19 | P2.1/A9 | 41 | P1.1 |
| 20 | P2.2/A10 | 42 | P1.2 |
| 21 | P2.3/A11 | 43 | P1.3 |
| 22 | P2.4/A12 | 44 | P1.4 |

*DO NOT CONNECT

NOTES TO QFP ONLY:

1. Due to EMC improvements, all VSS pins (6, 16, 28, 39) must be connected to VSS on the 80C652/83C652.

CMOS single-chip 8-bit microcontrollers

80C652/83C652

ORDER INFORMATION

| PHILIPS PART ORDER NUMBER PART MARKING | | | PHILIPS NORTH AMERICA PART ORDER NUMBER | | | TEMPERATURE RANGE (°C) AND PACKAGE | FREQ MHz ^{1,2} |
|--|------------------|-------------------|--|-------------|--------------------|--|----------------------------|
| ROMless | ROM ³ | Drawing Number | ROMless | ROM | EPROM ² | | |
| P80C652EBP | P83C652EBP/xxx | SOT129-1 | P80C652EBPN | P83C652EBPN | S87C652-4N40 | 0 to +70, Plastic Dual In-line Package | 16 |
| P80C652EBA | P83C652EBA/xxx | SOT187-2 | P80C652EBAA | P83C652EBAA | S87C652-4A44 | 0 to +70, Plastic Leaded Chip Carrier | 16 |
| P80C652EBB | P83C652EBB/xxx | SOT307-2 | P80C652EBBB | P83C652EBBB | S87C652-4B44 | 0 to +70, Plastic Quad Flat Pack | 16 |
| P80C652EFP | P83C652EFP/xxx | SOT129-1 | P80C652EFPN | P83C652EFPN | S87C652-5N40 | -40 to +85, Plastic Dual In-line Package | 16 |
| P80C652EFA | P83C652EFA/xxx | SOT187-2 | P80C652EFAA | P83C652EFAA | S87C652-5A44 | -40 to +85, Plastic Leaded Chip Carrier | 16 |
| P80C652EFB | P83C652EFB/xxx | SOT307-2 | P80C652EFBB | P83C652EFBB | S87C652-5B44 | -40 to +85, Plastic Quad Flat Pack | 16 |
| P80C652EHP | P83C652EHP/xxx | SOT129-1 | P80C652EHPN | P83C652EHPN | | -40 to +125, Plastic Dual In-line Package | 16 |
| P80C652EHA | P83C652EHA/xxx | SOT187-2 | P80C652EHAA | P83C652EHAA | | -40 to +125, Plastic Leaded Chip Carrier | 16 |
| P80C652EHB | P83C652EHB/xxx | SOT307-2 | P80C652EHBB | P83C652EHBB | | -40 to +125, Plastic Quad Flat Pack | 16 |
| P80C652IBP | P83C652IBP/xxx | SOT129-1 | P80C652IBPN | P83C652IBPN | | 0 to +70, Plastic Dual In-line Package | 24 |
| P80C652IBA | P83C652IBA/xxx | SOT187-2 | P80C652IBAA | P83C652IBAA | | 0 to +70, Plastic Leaded Chip Carrier | 24 |
| P80C652IBB | P83C652IBB/xxx | SOT307-2 | P80C652IBBB | P83C652IBBB | | 0 to +70, Plastic Quad Flat Pack | 24 |
| P80C652IFP | P83C652IFP/xxx | SOT129-1 | P80C652IFPN | P83C652IFPN | | -40 to +85, Plastic Dual In-line Package | 24 |
| P80C652IFA | P83C652IFA/xxx | SOT187-2 | P80C652IFAA | P83C652IFAA | | -40 to +85, Plastic Leaded Chip Carrier | 24 |
| P80C652IFB | P83C652IFB/xxx | SOT307-2 | P80C652IFBB | P83C652IFBB | | -40 to +85, Plastic Quad Flat Pack | 24 |

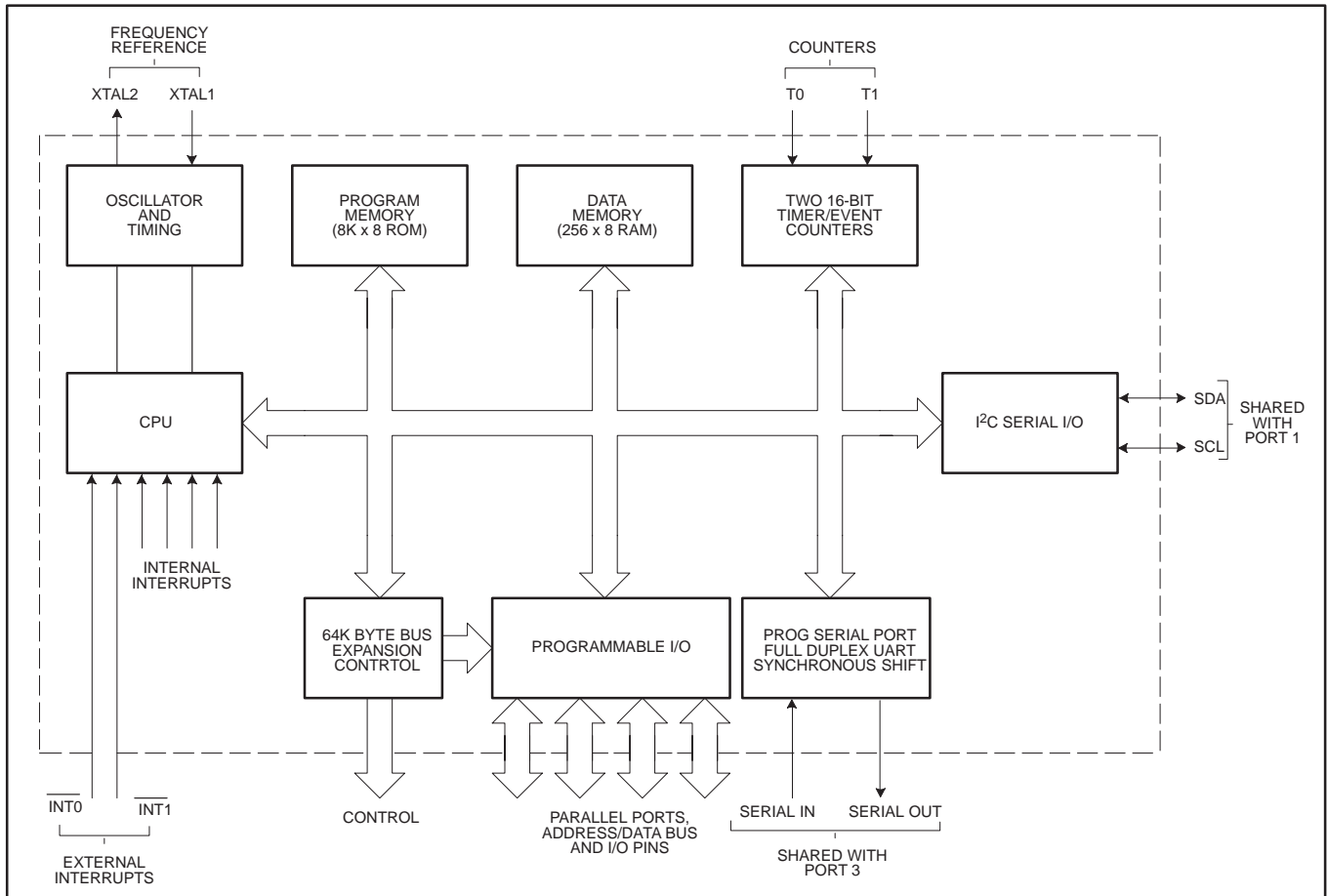
NOTES:

1. 80C652 and 83C652 frequency range is 3.5MHz–16MHz or 3.5MHz–24MHz.
2. For specification of the EPROM version, see the 87C652 data sheet.
3. xxx denotes the ROM code number.

CMOS single-chip 8-bit microcontrollers

80C652/83C652

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontrollers

80C652/83C652

PIN DESCRIPTIONS

| MNEMONIC | PIN NUMBER | | | TYPE | NAME AND FUNCTION |
|-----------------|------------|-----------|---------------|------|--|
| | DIP | PLCC | QFP | | |
| V _{SS} | 20 | 22 | 6, 16, 28, 39 | I | Ground: 0V reference. With the QFP package all V _{SS} pins (V _{SS1} to V _{SS4}) must be connected. |
| V _{DD} | 40 | 44 | 38 | I | Power Supply: This is the power supply voltage for normal, idle, and power-down operation. |
| P0.0–P0.7 | 39–32 | 43–36 | 37–30 | I/O | Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. |
| P1.0–P1.7 | 1–8 | 2–9 | 40–44, 1–3 | I/O | Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Alternate functions include: |
| P1.6 | 7 | 8 | 2 | I/O | SCL: I ² C-bus serial port clock line. |
| P1.7 | 8 | 9 | 3 | I/O | SDA: I ² C-bus serial port data line. |
| P2.0–P2.7 | 21–28 | 24–31 | 18–25 | I/O | Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. |
| P3.0–P3.7 | 10–17 | 11, 13–19 | 5, 7–13 | I/O | Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 80C51 family, as listed below: |
| | 10 | 11 | 5 | I | RxD (P3.0): Serial input port |
| | 11 | 13 | 7 | O | TxD (P3.1): Serial output port |
| | 12 | 14 | 8 | I | INT0 (P3.2): External interrupt |
| | 13 | 15 | 9 | I | INT1 (P3.3): External interrupt |
| | 14 | 16 | 10 | I | T0 (P3.4): Timer 0 external input |
| | 15 | 17 | 11 | I | T1 (P3.5): Timer 1 external input |
| | 16 | 18 | 12 | O | WR (P3.6): External data memory write strobe |
| | 17 | 19 | 13 | O | RD (P3.7): External data memory read strobe |
| RST | 9 | 10 | 4 | I | Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{DD} . |
| ALE | 30 | 33 | 27 | I/O | Address Latch Enable: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency. Note that one ALE pulse is skipped during each access to external data memory. |
| PSEN | 29 | 32 | 26 | O | Program Store Enable: Read strobe to external program memory via Port 0 and Port 2. It is activated twice each machine cycle during fetches from the external program memory. When executing out of external program memory two activations of PSEN are skipped during each access to external data memory. PSEN is not activated (remains HIGH) during no fetches from external program memory. PSEN can sink/source 8 LSTTL inputs and can drive CMOS inputs without external pull-ups. |
| E _A | 31 | 35 | 29 | I | External Access: If during a RESET, E _A is held at TTL, level HIGH, the CPU executes out of the internal program memory ROM provided the Program Counter is less than 8192. If during a RESET, E _A is held a TTL LOW level, the CPU executes out of external program memory. E _A is not allowed to float. |
| XTAL1 | 19 | 21 | 15 | I | Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| XTAL2 | 18 | 20 | 14 | O | Crystal 2: Output from the inverting oscillator amplifier. |

NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{DD} + 0.5V or V_{SS} - 0.5V, respectively.

CMOS single-chip 8-bit microcontrollers

80C652/83C652

Table 1. 8XC652/654 Special Function Registers

| SYMBOL | DESCRIPTION | DIRECT ADDRESS | BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION | | | | | | | | RESET VALUE |
|---------|------------------------|----------------|---|-------------|-----|-----|------|-------------|-----|-----|-------------|
| | | | MSB | | | | LSB | | | | |
| ACC* | Accumulator | E0H | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 | 00H |
| B* | B register | F0H | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | 00H |
| DPTR: | Data pointer (2 bytes) | | | | | | | | | | |
| DPH | Data pointer high | 83H | | | | | | | | | 00H |
| DPL | Data pointer low | 82H | AF | AE | AD | AC | AB | AA | A9 | A8 | 00H |
| IE*# | Interrupt enable | A8H | EA | | ES1 | ES0 | ET1 | EX1 | ET0 | EX0 | 0x000000B |
| | | | BF | BE | BD | BC | BB | BA | B9 | B8 | |
| IP*# | Interrupt priority | B8H | — | | PS1 | PS0 | PT1 | PX1 | PT0 | PX0 | xx000000B |
| | | | 87 | 86 | 85 | 84 | 83 | 82 | 81 | 80 | |
| P0* | Port 0 | 80H | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | FFH |
| | | | 97 | 96 | 95 | 94 | 93 | 92 | 91 | 90 | |
| P1*# | Port 1 | 90H | SDA | SCL | | | | | | | FFH |
| | | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| P2* | Port 2 | A0H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | FFH |
| | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| P3* | Port 3 | B0H | R \bar{D} | WR | T1 | T0 | INT1 | INT0 | TXD | RXD | FFH |
| PCON | Power control | 87H | SMOD | — | — | — | GF1 | GF0 | PD | IDL | 0xxx0000B |
| | | | 9F | 9E | 9D | 9C | 9B | 9A | 99 | 98 | |
| S0CON*# | Serial 0 port control | 98H | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI | 00H |
| S0BUF# | Serial 0 data buffer | 99H | | | | | | | | | xxxxxxxxB |
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PSW* | Program status word | D0H | CY | AC | F0 | RS1 | RS0 | OV | F1 | P | 00H |
| S1DAT# | Serial 1 data | DAH | | | | | | | | | 00H |
| SP | Stack pointer | 81H | | | | | | | | | 07H |
| S1ADR# | Serial 1 address | DBH | SLAVE ADDRESS | | | | | | | | GC |
| | | | | | | | | | | | |
| S1STA# | Serial 1 status | D9H | SC4 | SC3 | SC2 | SC1 | SC0 | 0 | 0 | 0 | F8H |
| | | | DF | DE | DD | DC | DB | DA | D9 | D8 | |
| S1CON*# | Serial 1 control | D8H | CR2 | ENS1 | STA | STO | SI | AA | CR1 | CR0 | 00000000B |
| | | | 8F | 8E | 8D | 8C | 8B | 8A | 89 | 88 | |
| TCON* | Timer control | 88H | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00H |
| TH1 | Timer high 1 | 8DH | | | | | | | | | 00H |
| TH0 | Timer high 0 | 8CH | | | | | | | | | 00H |
| TL1 | Timer low 1 | 8BH | | | | | | | | | 00H |
| TL0 | Timer low 0 | 8AH | | | | | | | | | 00H |
| TMOD | Timer mode | 89H | GATE | C \bar{T} | M1 | M0 | GATE | C \bar{T} | M1 | M0 | 00H |

* SFRs are bit addressable.

SFRs are modified from or added to the 80C51 SFRs.

CMOS single-chip 8-bit microcontrollers

80C652/83C652

ROM CODE PROTECTION (83C652)

The 8XC652 has an additional security feature. ROM code protection may be selected by setting a mask-programmable security bit (i.e., user dependent). This feature may be requested during ROM code submission. When selected, the ROM code is protected and cannot be read out at any time by any test mode or by any instruction in the external program memory space.

The MOVC instructions are the only instructions that have access to program code in the internal or external program memory. The \overline{EA} input is latched during RESET and is "don't care" after RESET (also if the security bit is not set). This implementation prevents reading internal program code by switching from external program memory to internal program memory during a MOVC instruction or any other instruction that uses immediate data.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the Logic Symbol, page 2.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{DD} and RST must come up at the same time for a proper start-up.

Idle Mode

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any

enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 2 shows the state of the I/O ports during low current operating modes.

I²C Serial Communication—SIO1

The I²C serial port is identical to the I²C serial port on the 8XC552. The operation of this subsystem is described in detail in the 8XC552 section of this manual.

Note that in both the 8XC652/4 and the 8XC552 the I²C pins are alternate functions to port pins P1.6 and P1.7. Because of this, P1.6 and P1.7 on these parts do not have a pull-up structure as found on the 80C51. Therefore P1.6 and P1.7 have open drain outputs on the 8XC652/4.

Table 2. External Pin Status During Idle and Power-Down Mode

| MODE | PROGRAM MEMORY | ALE | \overline{PSEN} | PORT 0 | PORT 1 | PORT 2 | PORT 3 |
|------------|----------------|-----|-------------------|--------|--------|---------|--------|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power-down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power-down | External | 0 | 0 | Float | Data | Data | Data |

Serial Control Register (S1CON) – See Table 3

| | | | | | | | | |
|-------------|-----|------|-----|-----|----|----|-----|-----|
| S1CON (D8H) | CR2 | ENS1 | STA | STO | SI | AA | CR1 | CR0 |
|-------------|-----|------|-----|-----|----|----|-----|-----|

Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

Table 3. Serial Clock Rates

| CR2 | CR1 | CR0 | BIT FREQUENCY (kHz) AT f_{osc} | | | | f_{osc} DIVIDED BY |
|-----|-----|-----|----------------------------------|-------------------------|-------------------------|-------------------------|---|
| | | | 6MHz | 12MHz | 16MHz | 24MHz | |
| 0 | 0 | 0 | 23 | 47 | 62.5 | 94 | 256 |
| 0 | 0 | 1 | 27 | 54 | 71 | 107 ¹ | 224 |
| 0 | 1 | 0 | 31.25 | 62.5 | 83.3 | 125 ¹ | 192 |
| 0 | 1 | 1 | 37 | 75 | 100 | 150 ¹ | 160 |
| 1 | 0 | 0 | 6.25 | 12.5 | 17 | 25 | 960 |
| 1 | 0 | 1 | 50 | 100 | 133 ¹ | 200 ¹ | 120 |
| 1 | 1 | 0 | 100 | 200 ¹ | 267 ¹ | 400 ¹ | 60 |
| 1 | 1 | 1 | 0.24 < 62.5 0 to 255 | 0.49 < 62.5 0 to 254 | 0.65 < 55.6 0 to 253 | 0.98 < 50.0 0 to 251 | 96 × (256 – (reload value Timer 1)) reload value range Timer 1 (in mode 2) |

NOTES:

1. These frequencies exceed the upper limit of 100kHz of the I²C-bus specification and cannot be used in an I²C-bus application.

CMOS single-chip 8-bit microcontrollers

80C652/83C652

ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

| PARAMETER | RATING | UNIT |
|--|---------------|------|
| Storage temperature range | -65 to +150 | °C |
| Voltage on any other pin to V_{SS} | -0.5 to + 6.0 | V |
| Input, output current on any single pin | ±5 | mA |
| Power dissipation (based on package heat transfer limitations, not device power consumption) | 1 | W |

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DEVICE SPECIFICATIONS

| TYPE | SUPPLY VOLTAGE (V) | | FREQUENCY (MHz) | | TEMPERATURE RANGE (°C) |
|------------|--------------------|------|-----------------|------|------------------------|
| | MIN. | MAX. | MIN. | MAX. | |
| P8XC652EBx | 4.5 | 5.5 | 3.5 | 16 | 0 to +70 |
| P8XC652EFx | 4.5 | 5.5 | 3.5 | 16 | -40 to +85 |
| P8XC652EHx | 4.5 | 5.5 | 3.5 | 16 | -40 to +125 |
| P8XC652IBx | 4.5 | 5.5 | 3.5 | 24 | 0 to +70 |
| P83X652IFx | 4.5 | 5.5 | 3.5 | 24 | -40 to +85 |

CMOS single-chip 8-bit microcontrollers

80C652/83C652

DC ELECTRICAL CHARACTERISTICS

 $V_{SS} = 0V$; $V_{DD} = 5V \pm 10\%$

| SYMBOL | PARAMETER | PART TYPE | TEST CONDITIONS | LIMITS | | UNIT |
|-----------|---|---------------|--|-----------------|------------------|--------------------|
| | | | | MIN. | MAX. | |
| V_{IL} | Input low voltage, except \overline{EA} , P1.6/SCL, P1.7/SDA | 0 to +70°C | | -0.5 | $0.2V_{DD}-0.1$ | V |
| | | -40 to +85°C | | -0.5 | $0.2V_{DD}-0.15$ | V |
| | | -40 to +125°C | | -0.5 | $0.2V_{DD}-0.25$ | V |
| V_{IL1} | Input low voltage to \overline{EA} | 0 to +70°C | | -0.5 | $0.2V_{DD}-0.3$ | V |
| | | -40 to +85°C | | -0.5 | $0.2V_{DD}-0.35$ | V |
| | | -40 to +125°C | | -0.5 | $0.2V_{DD}-0.45$ | V |
| V_{IL2} | Input low voltage to P1.6/SCL, P1.7/SDA ⁶ | | | -0.5 | $0.3V_{DD}$ | V |
| V_{IH} | Input high voltage, except XTAL1, RST, P1.6/SCL, P1.7/SDA | 0 to +70°C | | $0.2V_{DD}+0.9$ | $V_{DD}+0.5$ | V |
| | | -40 to +85°C | | $0.2V_{DD}+1.0$ | $V_{DD}+0.5$ | V |
| | | -40 to +125°C | | $0.2V_{DD}+1.0$ | $V_{DD}+0.5$ | V |
| V_{IH1} | Input high voltage, XTAL1, RST | 0 to +70°C | | $0.7V_{DD}$ | $V_{DD}+0.5$ | V |
| | | -40 to +85°C | | $0.7V_{DD}+0.1$ | $V_{DD}+0.5$ | V |
| | | -40 to +125°C | | $0.7V_{DD}+0.1$ | $V_{DD}+0.5$ | V |
| V_{IH2} | Input high voltage, P1.6/SCL, P1.7/SDA ⁶ | | | $0.7V_{DD}$ | 6.0 | V |
| V_{OL} | Output low voltage, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA | | $I_{OL} = 1.6mA^{8,9}$ | | 0.45 | V |
| V_{OL1} | Output low voltage, port 0, ALE, PSEN | | $I_{OL} = 3.2mA^{8,9}$ | | 0.45 | V |
| V_{OL2} | Output low voltage, P1.6/SCL, P1.7/SDA | | $I_{OL} = 3.0mA$ | | 0.4 | V |
| V_{OH} | Output high voltage, ports 1, 2, 3, ALE, \overline{PSEN}^{10} | | $I_{OH} = -60\mu A$ | 2.4 | | V |
| | | | $I_{OH} = -25\mu A$ | $0.75V_{DD}$ | | V |
| | | | $I_{OH} = -10\mu A$ | $0.9V_{DD}$ | | V |
| V_{OH1} | Output high voltage; port 0 in external bus mode | | $I_{OH} = -800\mu A$ | 2.4 | | V |
| | | | $I_{OH} = -300\mu A$ | $0.75V_{DD}$ | | V |
| | | | $I_{OH} = -80\mu A$ | $0.9V_{DD}$ | | V |
| I_{IL} | Logical 0 input current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA | 0 to +70°C | $V_{IN} = 0.45V$ | | -50 | μA |
| | | -40 to +85°C | | | -75 | μA |
| | | -40 to +125°C | | | -75 | μA |
| I_{TL} | Logical 1-to-0 transition current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA | 0 to +70°C | See note 7 | | -650 | μA |
| | | -40 to +85°C | | | -750 | μA |
| | | -40 to +125°C | | | -750 | μA |
| I_{L1} | Input leakage current, port 0, \overline{EA} | | $0.45V < V_I < V_{DD}$ | | ± 10 | μA |
| I_{L2} | Input leakage current, P1.6/SCL, P1.7/SDA | | $0V < V_I < 6.0V$ $0V < V_{DD} < 6.0V$ | | ± 10 | μA |
| I_{DD} | Power supply current: Active mode @ 16MHz ^{2, 11} Active mode @ 24MHz ^{2, 11} Idle mode @ 16MHz ^{3, 11} Idle mode @ 24MHz ^{3, 11} Power down mode ^{4, 5} Power down mode ^{4, 5} | | See note 1 $V_{DD}=5.5V$ $V_{DD}=5.5V$ | | 26.5 | mA |
| | | | | | 33.8 | mA |
| | | | | | 6 | mA |
| | | | | | 7 | mA |
| | | -40 to +125°C | | | 50 100 | μA μA |
| R_{RST} | Internal reset pull-down resistor | | | 50 | 150 | k Ω |
| C_{IO} | Pin capacitance | | Freq.=1MHz | | 10 | pF |

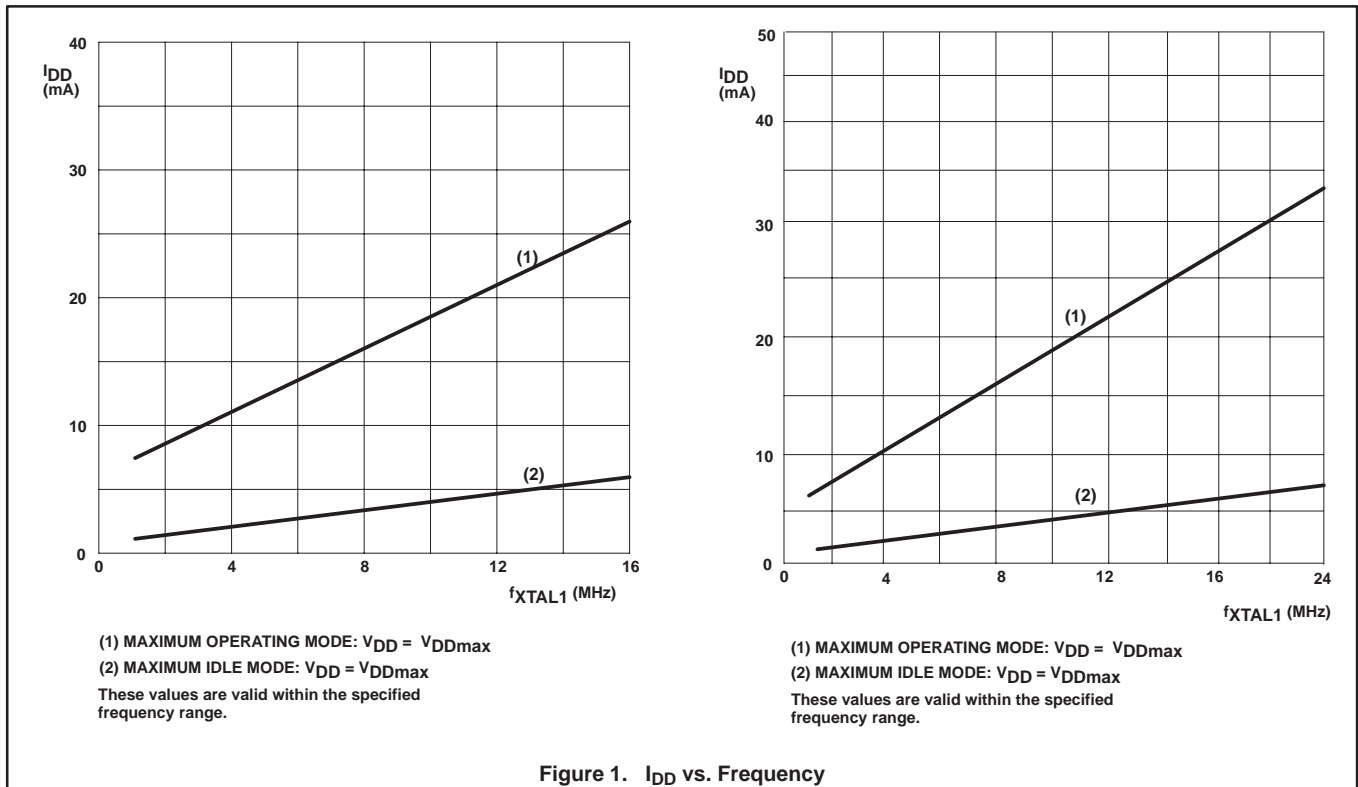
NOTES ON NEXT PAGE.

CMOS single-chip 8-bit microcontrollers

80C652/83C652

NOTES FOR DC ELECTRICAL CHARACTERISTICS:

1. See Figures 9 through 11 for I_{DD} test conditions.
2. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 5\text{ns}$; $V_{IL} = V_{SS} + 0.5\text{V}$; $V_{IH} = V_{DD} - 0.5\text{V}$; XTAL2 not connected; $\overline{EA} = \text{RST} = \text{Port 0} = \text{P1.6} = \text{P1.7} = V_{DD}$. See Figure 9.
3. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 5\text{ns}$; $V_{IL} = V_{SS} + 0.5\text{V}$; $V_{IH} = V_{DD} - 0.5\text{V}$; XTAL2 not connected; Port 0 = P1.6 = P1.7 = V_{DD} ; $\overline{EA} = \text{RST} = V_{SS}$. See Figure 10.
4. The power-down current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = P1.6 = P1.7 = V_{DD} ; $\overline{EA} = \text{RST} = V_{SS}$. See Figure 11.
5. $2\text{V} \leq V_{PD} \leq V_{DDmax}$.
6. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I²C specification, so an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
7. Pins of ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
8. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OLs} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
9. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows: Maximum $I_{OL} = 10\text{mA}$ per port pin; Maximum $I_{OL} = 26\text{mA}$ total for Port 0; Maximum $I_{OL} = 15\text{mA}$ total for Ports 1, 2, and 3; Maximum $I_{OL} = 71\text{mA}$ total for all output pins. If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
10. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{\text{PSEN}}$ to momentarily fall below the $0.9V_{DD}$ specification when the address bits are stabilizing.
11. I_{DDMAX} for other frequencies can be derived from Figure 1, where FREQ is the external oscillator frequency in MHz. I_{DDMAX} is given in mA.



CMOS single-chip 8-bit microcontrollers

80C652/83C652

AC ELECTRICAL CHARACTERISTICS^{1, 2} (16 MHz type)

| SYMBOL | FIGURE | PARAMETER | 16MHz CLOCK | | VARIABLE CLOCK | | UNIT |
|-----------------------|--------|---|-------------|-----|--------------------------|---------------------------------------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1/t _{CLCL} | 2 | Oscillator frequency | | | 3.5 | 16 | MHz |
| t _{LHLL} | 2 | ALE pulse width | 85 | | 2t _{CLCL} -40 | | ns |
| t _{AVLL} | 2 | Address valid to ALE low | 8 | | t _{CLCL} -55 | | ns |
| t _{LLAX} | 2 | Address hold after ALE low | 28 | | t _{CLCL} -35 | | ns |
| t _{LLIV} | 2 | ALE low to valid instruction in | | 150 | | 4t _{CLCL} -100 | ns |
| t _{LLPL} | 2 | ALE low to PSEN low | 23 | | t _{CLCL} -40 | | ns |
| t _{PLPH} | 2 | PSEN pulse width | 143 | | 3t _{CLCL} -45 | | ns |
| t _{PLIV} | 2 | PSEN low to valid instruction in | | 83 | | 3t _{CLCL} -105 | ns |
| t _{PXIX} | 2 | Input instruction hold after PSEN | 0 | | 0 | | ns |
| t _{PXIZ} | 2 | Input instruction float after PSEN | | 38 | | t _{CLCL} -25 | ns |
| t _{AVIV} | 2 | Address to valid instruction in | | 208 | | 5t _{CLCL} -105 | ns |
| t _{PLAZ} | 2 | PSEN low to address float | | 10 | | 10 | ns |
| Data Memory | | | | | | | |
| t _{RLRH} | 3, 4 | RD pulse width | 275 | | 6t _{CLCL} -100 | | ns |
| t _{WLWH} | 3, 4 | WR pulse width | 275 | | 6t _{CLCL} -100 | | ns |
| t _{RLDV} | 3, 4 | RD low to valid data in | | 148 | | 5t _{CLCL} -165 | ns |
| t _{RHDX} | 3, 4 | Data hold after RD | 0 | | 0 | | ns |
| t _{RHDZ} | 3, 4 | Data float after RD | | 55 | | 2t _{CLCL} -70 | ns |
| t _{LLDV} | 3, 4 | ALE low to valid data in | | 350 | | 8t _{CLCL} -150 | ns |
| t _{AVDV} | 3, 4 | Address to valid data in | | 398 | | 9t _{CLCL} -165 | ns |
| t _{LLWL} | 3, 4 | ALE low to RD or WR low | 138 | 238 | 3t _{CLCL} -50 | 3t _{CLCL} +50 | ns |
| t _{AVWL} | 3, 4 | Address valid to WR low or RD low | 120 | | 4t _{CLCL} -130 | | ns |
| t _{QVWX} | 3, 4 | Data valid to WR transition | 3 | | t _{CLCL} -60 | | ns |
| t _{DW} | 3, 4 | Data setup time before WR | 288 | | 7t _{CLCL} -150 | | ns |
| t _{WHQX} | 3, 4 | Data hold after WR | 13 | | t _{CLCL} -50 | | ns |
| t _{RLAZ} | 3, 4 | RD low to address float | | 0 | | 0 | ns |
| t _{WHLH} | 3, 4 | RD or WR high to ALE high | 23 | 103 | t _{CLCL} -40 | t _{CLCL} +40 | ns |
| Shift Register | | | | | | | |
| t _{XLXL} | 5 | Serial port clock cycle time ³ | 0.75 | | 12t _{CLCL} | | μs |
| t _{QVXH} | 5 | Output data setup to clock rising edge ³ | 492 | | 10t _{CLCL} -133 | | ns |
| t _{XHQX} | 5 | Output data hold after clock rising edge ³ | 80 | | 2t _{CLCL} -117 | | ns |
| t _{XHDX} | 5 | Input data hold after clock rising edge ³ | 0 | | 0 | | ns |
| t _{XHDV} | 5 | Clock rising edge to input data valid ³ | | 492 | | 10t _{CLCL} -133 | ns |
| External Clock | | | | | | | |
| t _{CHCX} | 6 | High time ³ | 20 | | 20 | t _{CLCL} - t _{CLCX} | ns |
| t _{CLCX} | 6 | Low time ³ | 20 | | 20 | t _{CLCL} - t _{CHCX} | ns |
| t _{CLCH} | 6 | Rise time ³ | | 20 | | 20 | ns |
| t _{CHCL} | 6 | Fall time ³ | | 20 | | 20 | ns |

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- These values are characterized but not 100% production tested.

CMOS single-chip 8-bit microcontrollers

80C652/83C652

AC ELECTRICAL CHARACTERISTICS^{1, 2} (24 MHz type)

| SYMBOL | FIGURE | PARAMETER | 24MHz CLOCK | | VARIABLE CLOCK | | UNIT |
|-----------------------|--------|---|-------------|-----|--------------------------|---------------------------------------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1/t _{CLCL} | 2 | Oscillator frequency | | | 3.5 | 24 | MHz |
| t _{LHLL} | 2 | ALE pulse width | 43 | | 2t _{CLCL} -40 | | ns |
| t _{AVLL} | 2 | Address valid to ALE low | 17 | | t _{CLCL} -25 | | ns |
| t _{LLAX} | 2 | Address hold after ALE low | 17 | | t _{CLCL} -25 | | ns |
| t _{LLIV} | 2 | ALE low to valid instruction in | | 102 | | 4t _{CLCL} -65 | ns |
| t _{LLPL} | 2 | ALE low to PSEN low | 17 | | t _{CLCL} -25 | | ns |
| t _{PLPH} | 2 | PSEN pulse width | 80 | | 3t _{CLCL} -45 | | ns |
| t _{PLIV} | 2 | PSEN low to valid instruction in | | 65 | | 3t _{CLCL} -60 | ns |
| t _{PXIX} | 2 | Input instruction hold after PSEN | 0 | | 0 | | ns |
| t _{PXIZ} | 2 | Input instruction float after PSEN | | 17 | | t _{CLCL} -25 | ns |
| t _{AVIV} | 2 | Address to valid instruction in | | 128 | | 5t _{CLCL} -80 | ns |
| t _{PLAZ} | 2 | PSEN low to address float | | 10 | | 10 | ns |
| Data Memory | | | | | | | |
| t _{RLRH} | 3, 4 | RD pulse width | 150 | | 6t _{CLCL} -100 | | ns |
| t _{WLWH} | 3, 4 | WR pulse width | 150 | | 6t _{CLCL} -100 | | ns |
| t _{RLDV} | 3, 4 | RD low to valid data in | | 118 | | 5t _{CLCL} -90 | ns |
| t _{RHDX} | 3, 4 | Data hold after RD | 0 | | 0 | | ns |
| t _{RHDZ} | 3, 4 | Data float after RD | | 55 | | 2t _{CLCL} -28 | ns |
| t _{LLDV} | 3, 4 | ALE low to valid data in | | 180 | | 8t _{CLCL} -150 | ns |
| t _{AVDV} | 3, 4 | Address to valid data in | | 210 | | 9t _{CLCL} -165 | ns |
| t _{LLWL} | 3, 4 | ALE low to RD or WR low | 75 | 175 | 3t _{CLCL} -50 | 3t _{CLCL} +50 | ns |
| t _{AVWL} | 3, 4 | Address valid to WR low or RD low | 92 | | 4t _{CLCL} -75 | | ns |
| t _{QVWX} | 3, 4 | Data valid to WR transition | 12 | | t _{CLCL} -30 | | ns |
| t _{DW} | 3, 4 | Data setup time before WR | 162 | | 7t _{CLCL} -130 | | ns |
| t _{WHQX} | 3, 4 | Data hold after WR | 17 | | t _{CLCL} -25 | | ns |
| t _{RLAZ} | 3, 4 | RD low to address float | | 0 | | 0 | ns |
| t _{WHLH} | 3, 4 | RD or WR high to ALE high | 17 | 67 | t _{CLCL} -25 | t _{CLCL} +25 | ns |
| Shift Register | | | | | | | |
| t _{XLXL} | 5 | Serial port clock cycle time ³ | 0.5 | | 12t _{CLCL} | | μs |
| t _{QVXH} | 5 | Output data setup to clock rising edge ³ | 283 | | 10t _{CLCL} -133 | | ns |
| t _{XHQX} | 5 | Output data hold after clock rising edge ³ | 23 | | 2t _{CLCL} -60 | | ns |
| t _{XHDX} | 5 | Input data hold after clock rising edge ³ | 0 | | 0 | | ns |
| t _{XHDV} | 5 | Clock rising edge to input data valid ³ | | 283 | | 10t _{CLCL} -133 | ns |
| External Clock | | | | | | | |
| t _{CHCX} | 6 | High time ³ | 17 | | 17 | t _{CLCL} - t _{CLCX} | ns |
| t _{CLCX} | 6 | Low time ³ | 17 | | 17 | t _{CLCL} - t _{CHCX} | ns |
| t _{CLCH} | 6 | Rise time ³ | | 5 | | 5 | ns |
| t _{CHCL} | 6 | Fall time ³ | | 5 | | 5 | ns |

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- These values are characterized but not 100% production tested.

CMOS single-chip 8-bit microcontrollers

80C652/83C652

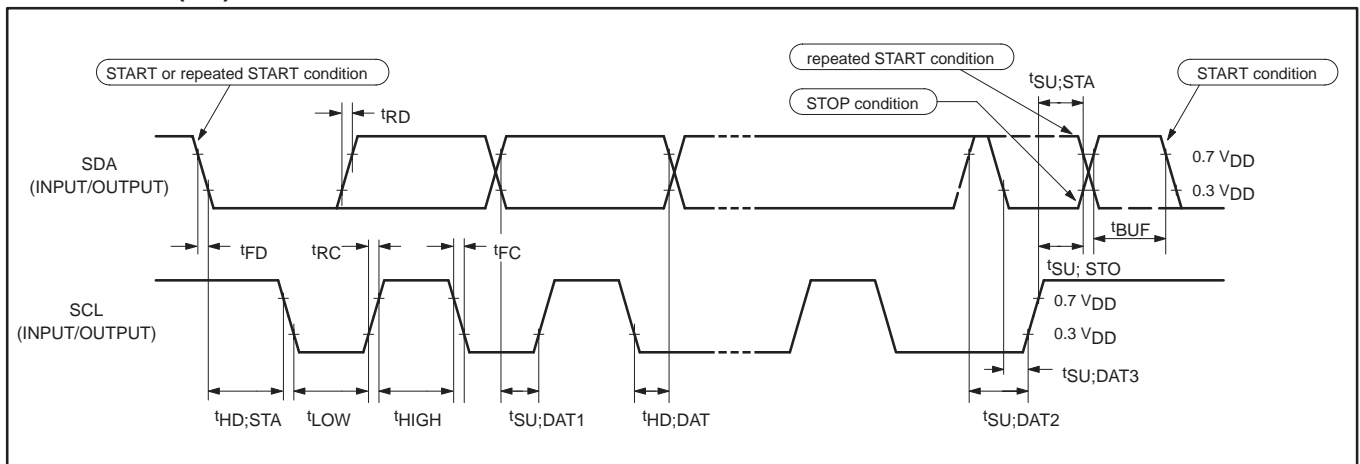
AC ELECTRICAL CHARACTERISTICS – I²C INTERFACE

| SYMBOL | PARAMETER | INPUT | OUTPUT |
|-----------------------------------|---|------------------------|--|
| SCL TIMING CHARACTERISTICS | | | |
| t _{HD;STA} | START condition hold time | ≥ 14 t _{CLCL} | > 4.0μs ¹ |
| t _{LOW} | SCL LOW time | ≥ 16 t _{CLCL} | > 4.7μs ¹ |
| t _{HIGH} | SCL HIGH time | ≥ 14 t _{CLCL} | > 4.0μs ¹ |
| t _{RC} | SCL rise time | ≤ 1μs | – ² |
| t _{FC} | SCL fall time | ≤ 0.3μs | < 0.3μs ³ |
| SDA TIMING CHARACTERISTICS | | | |
| t _{SU;DAT1} | Data set-up time | ≥ 250ns | > 20 t _{CLCL} – t _{RD} |
| t _{SU;DAT2} | SDA set-up time (before rep. START cond.) | ≥ 250ns | > 1μs ¹ |
| t _{SU;DAT3} | SDA set-up time (before STOP cond.) | ≥ 250ns | > 8 t _{CLCL} |
| t _{HD;DAT} | Data hold time | ≥ 0ns | > 8 t _{CLCL} – t _{FC} |
| t _{SU;STA} | Repeated START set-up time | ≥ 14 t _{CLCL} | > 4.7μs ¹ |
| t _{SU;STO} | STOP condition set-up time | ≥ 14 t _{CLCL} | > 4.0μs ¹ |
| t _{BUF} | Bus free time | ≥ 14 t _{CLCL} | > 4.7μs ¹ |
| t _{RD} | SDA rise time | ≤ 1μs | – ² |
| t _{FD} | SDA fall time | ≤ 0.3μs | < 0.3μs ³ |

NOTES:

- At 100 kbit/s. At other bit rates this value is inversely proportional to the bit-rate of 100 kbit/s.
- Determined by the external bus-line capacitance and the external bus-line pull-resistor, this must be < 1μs.
- Spikes on the SDA and SCL lines with a duration of less than 3 t_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400pF.
- t_{CLCL} = 1/f_{OSC} = one oscillator clock period at pin XTAL1. For 63ns (42ns) < t_{CLCL} < 285ns (16MHz (24MHz) > f_{OSC} > 3.5MHz) the SIO1 interface meets the I²C-bus specification for bit-rates up to 100 kbit/s.

TIMING SIO1 (I²C) INTERFACE



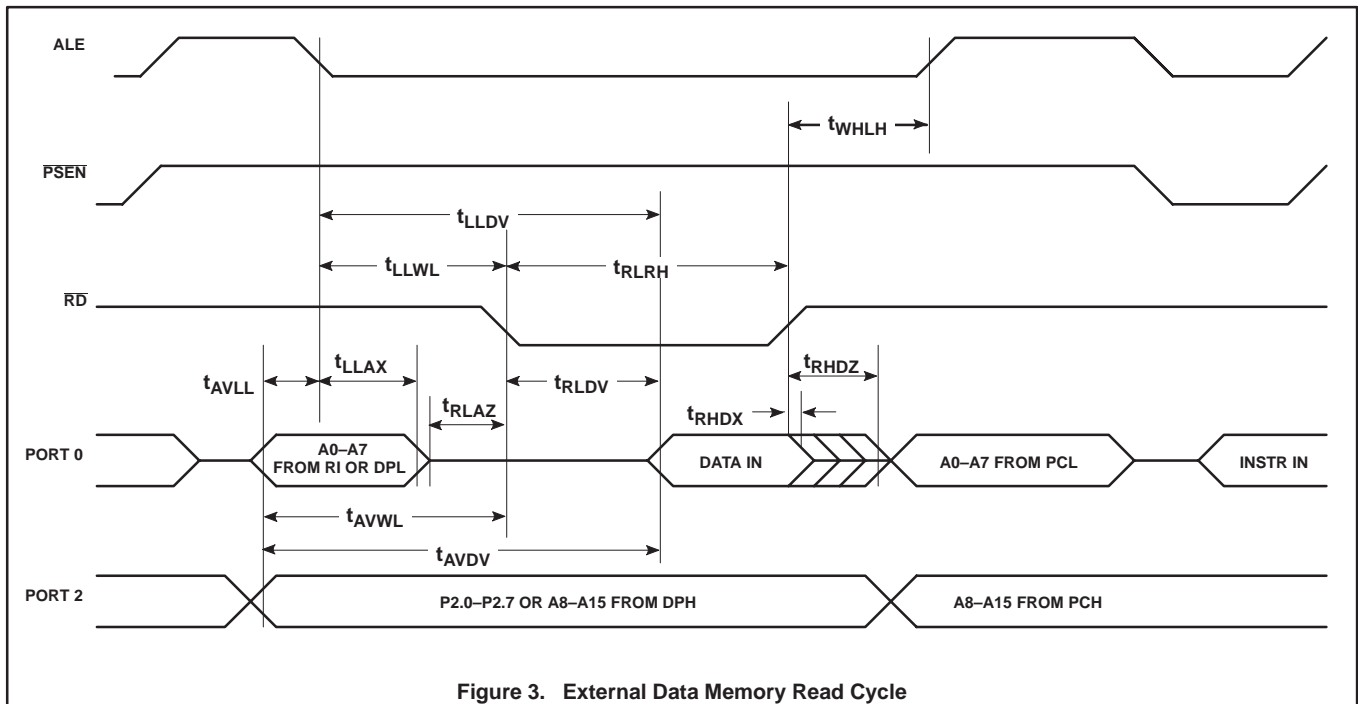
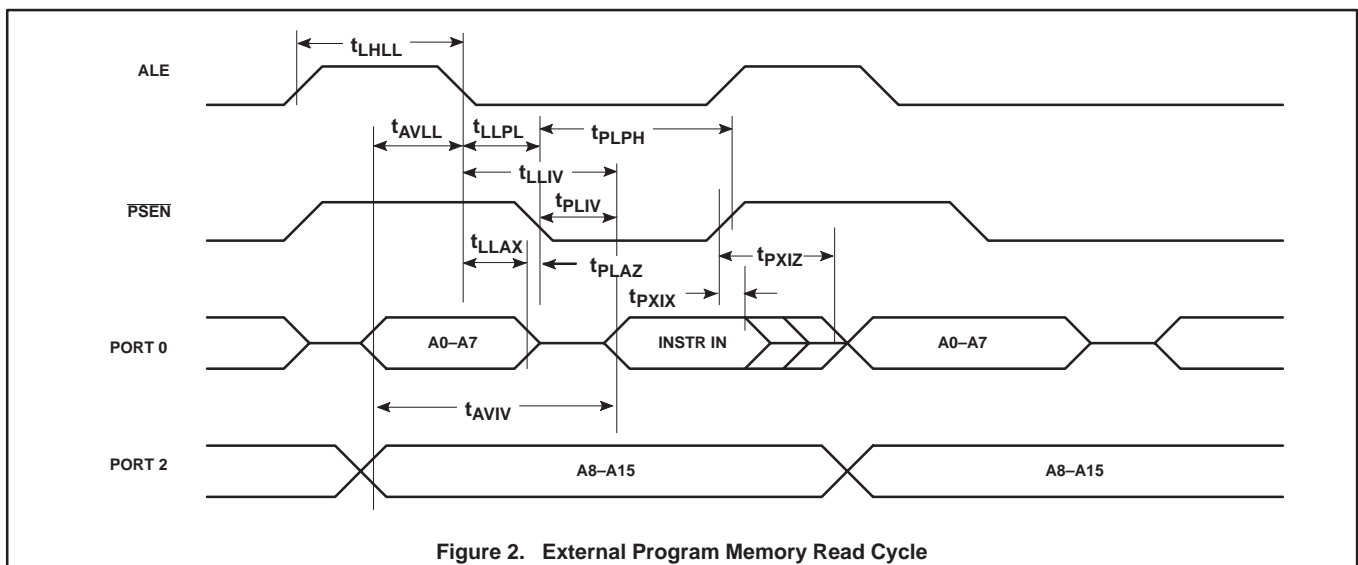
CMOS single-chip 8-bit microcontrollers

80C652/83C652

EXPLANATION OF THE AC SYMBOLS

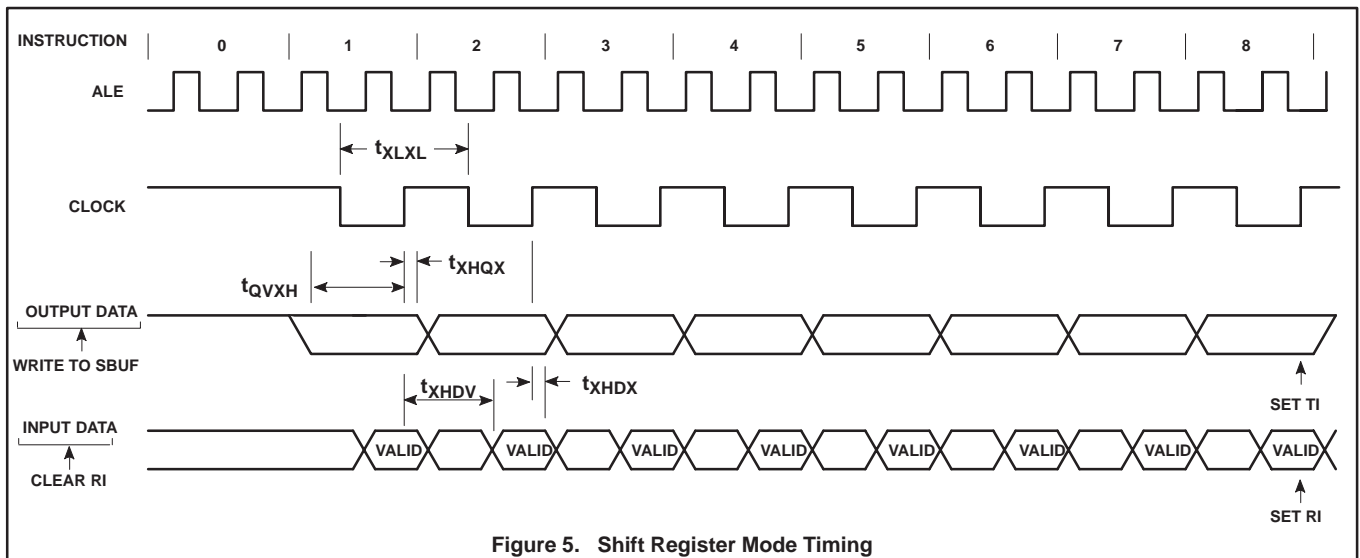
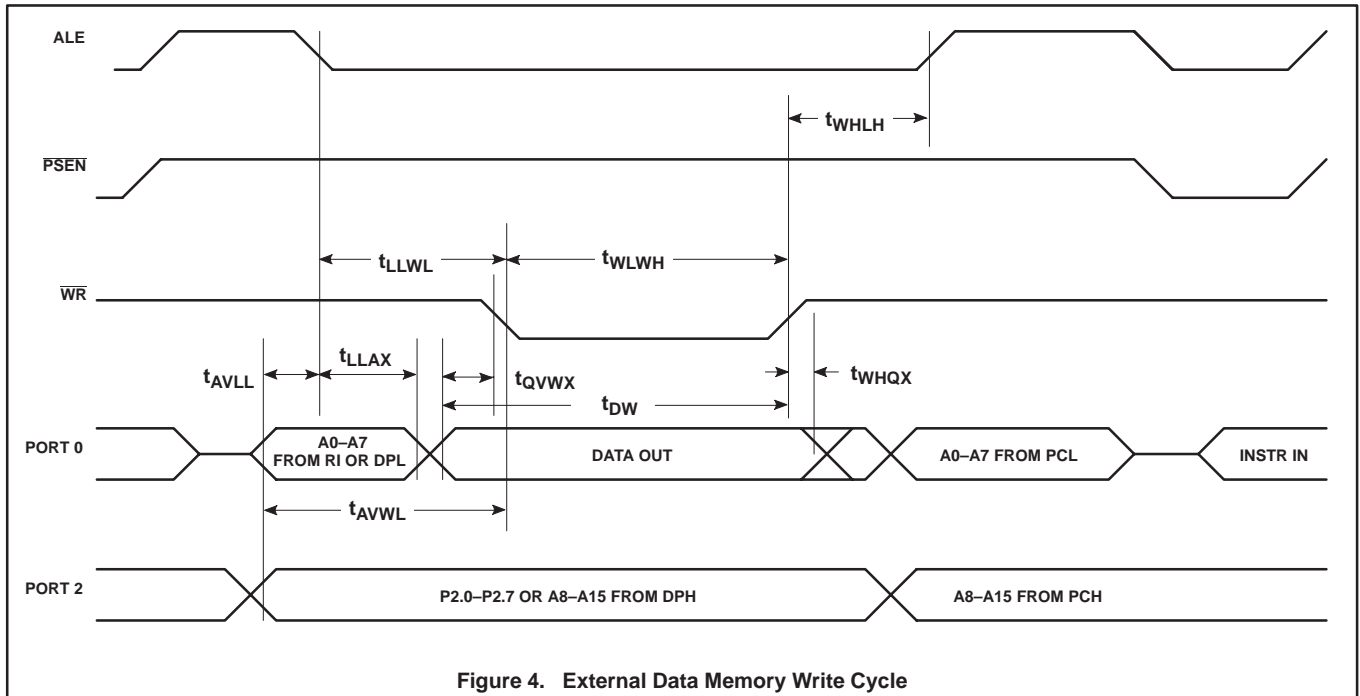
Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:
 A – Address
 C – Clock
 D – Input data
 H – Logic level high
 I – Instruction (program memory contents)
 L – Logic level low, or ALE
 P – $\overline{\text{PSEN}}$

Q – Output data
 R – $\overline{\text{RD}}$ signal
 t – Time
 V – Valid
 W – $\overline{\text{WR}}$ signal
 X – No longer a valid logic level
 Z – Float
Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.



CMOS single-chip 8-bit microcontrollers

80C652/83C652



CMOS single-chip 8-bit microcontrollers

80C652/83C652

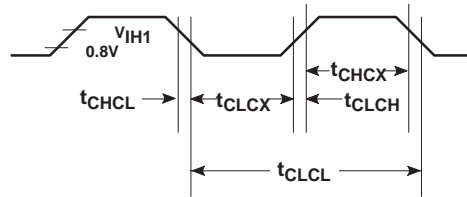
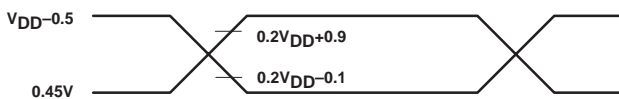
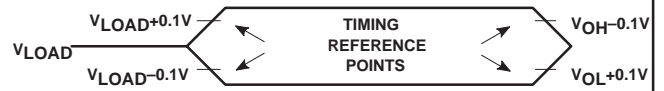


Figure 6. External Clock Drive at XTAL1



NOTE:
 AC INPUTS DURING TESTING ARE DRIVEN AT $V_{DD}-0.5$ FOR A LOGIC '1' AND 0.45V FOR A LOGIC '0'. TIMING MEASUREMENTS ARE MADE AT V_{IH} MIN FOR A LOGIC '1' AND V_{IL} MAX FOR A LOGIC '0'.

Figure 7. AC Testing Input/Output

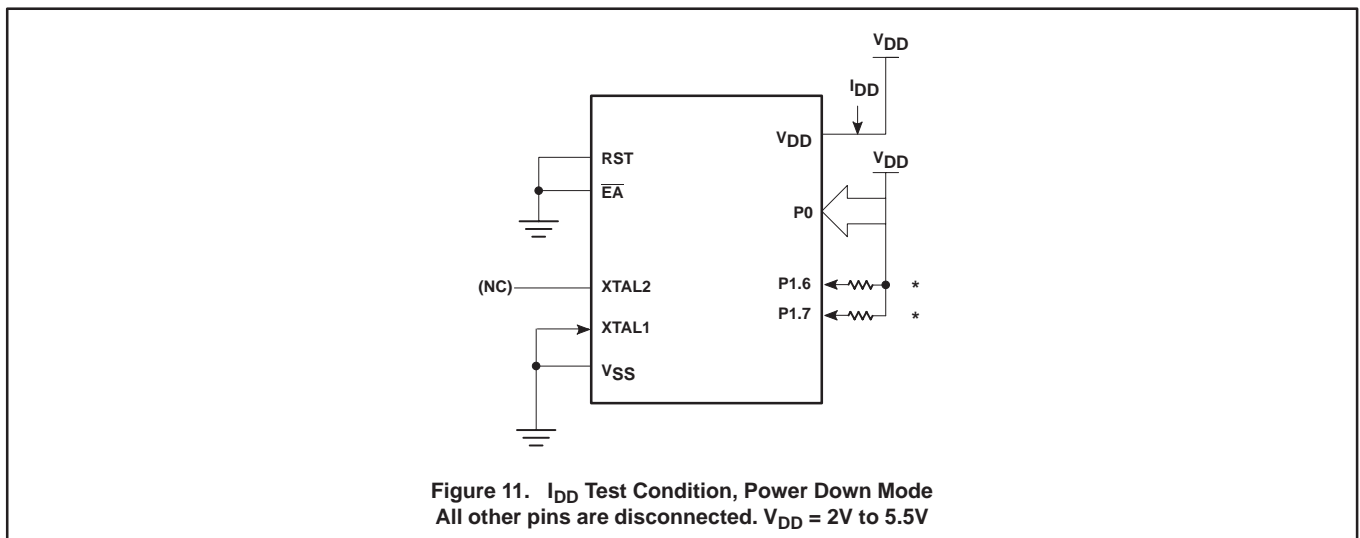
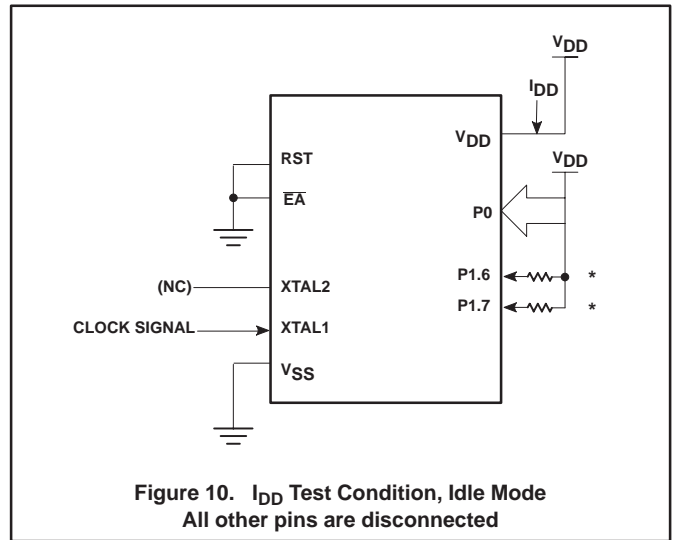
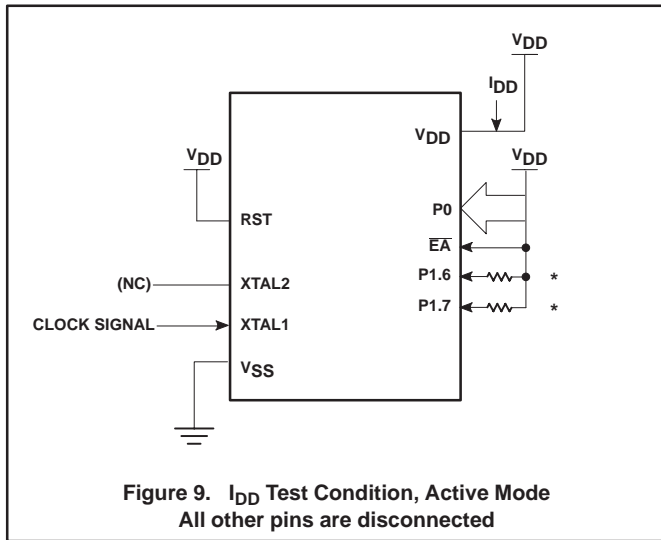


NOTE:
 FOR TIMING PURPOSES, A PORT IS NO LONGER FLOATING WHEN A 100mV CHANGE FROM LOAD VOLTAGE OCCURS, AND BEGINS TO FLOAT WHEN A 100mV CHANGE FROM THE LOADED V_{OH}/V_{OL} LEVEL OCCURS. $I_{OH}/I_{OL} \geq \pm 20mA$.

Figure 8. Float Waveform

CMOS single-chip 8-bit microcontrollers

80C652/83C652



NOTE:

* Ports 1.6 and 1.7 should be connected to V_{CC} through resistors of sufficiently high value such that the sink current into these pins does not exceed the I_{OL1} specification.



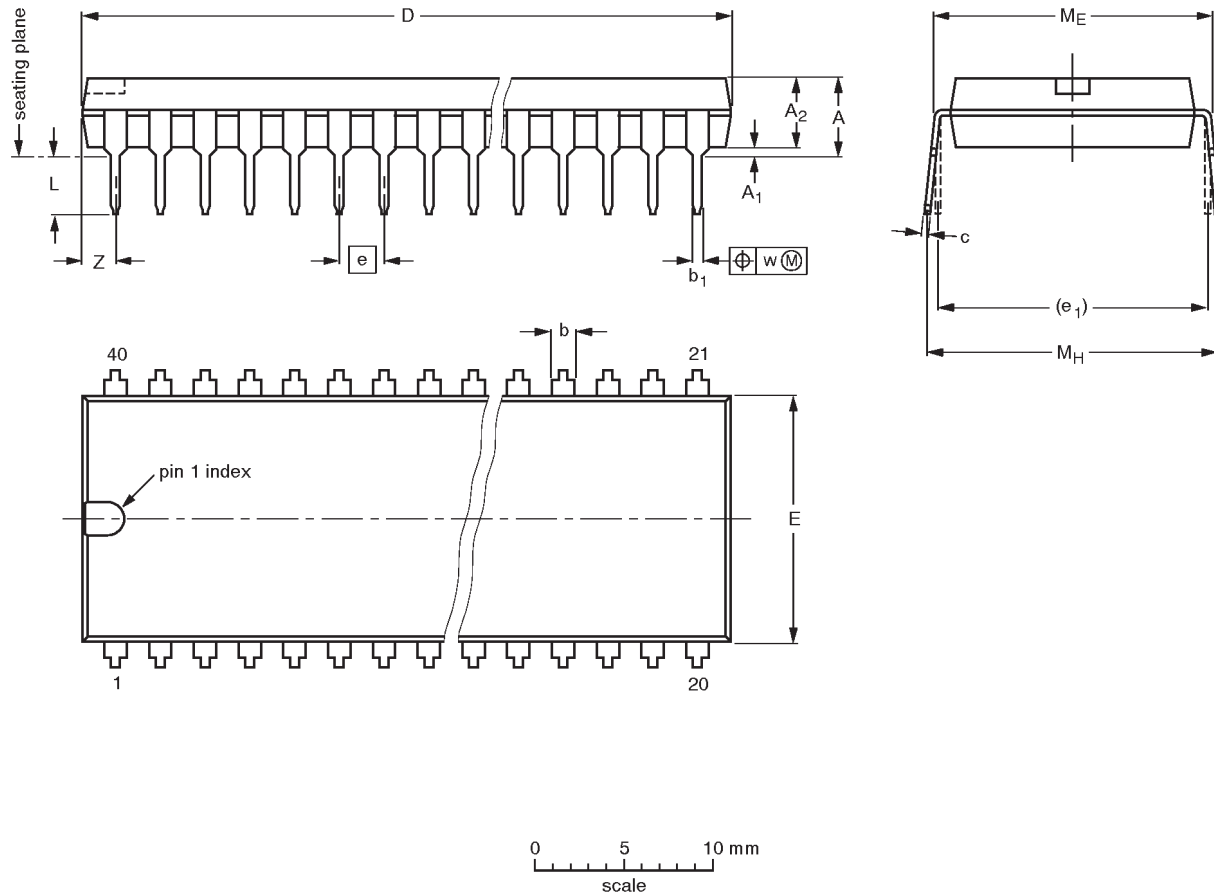
Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

CMOS single-chip 8-bit microcontrollers

80C652/83C652

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.7 | 0.51 | 4.0 | 1.70 1.14 | 0.53 0.38 | 0.36 0.23 | 52.50 51.50 | 14.1 13.7 | 2.54 | 15.24 | 3.60 3.05 | 15.80 15.24 | 17.42 15.90 | 0.254 | 2.25 |
| inches | 0.19 | 0.020 | 0.16 | 0.067 0.045 | 0.021 0.015 | 0.014 0.009 | 2.067 2.028 | 0.56 0.54 | 0.10 | 0.60 | 0.14 0.12 | 0.62 0.60 | 0.69 0.63 | 0.01 | 0.089 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

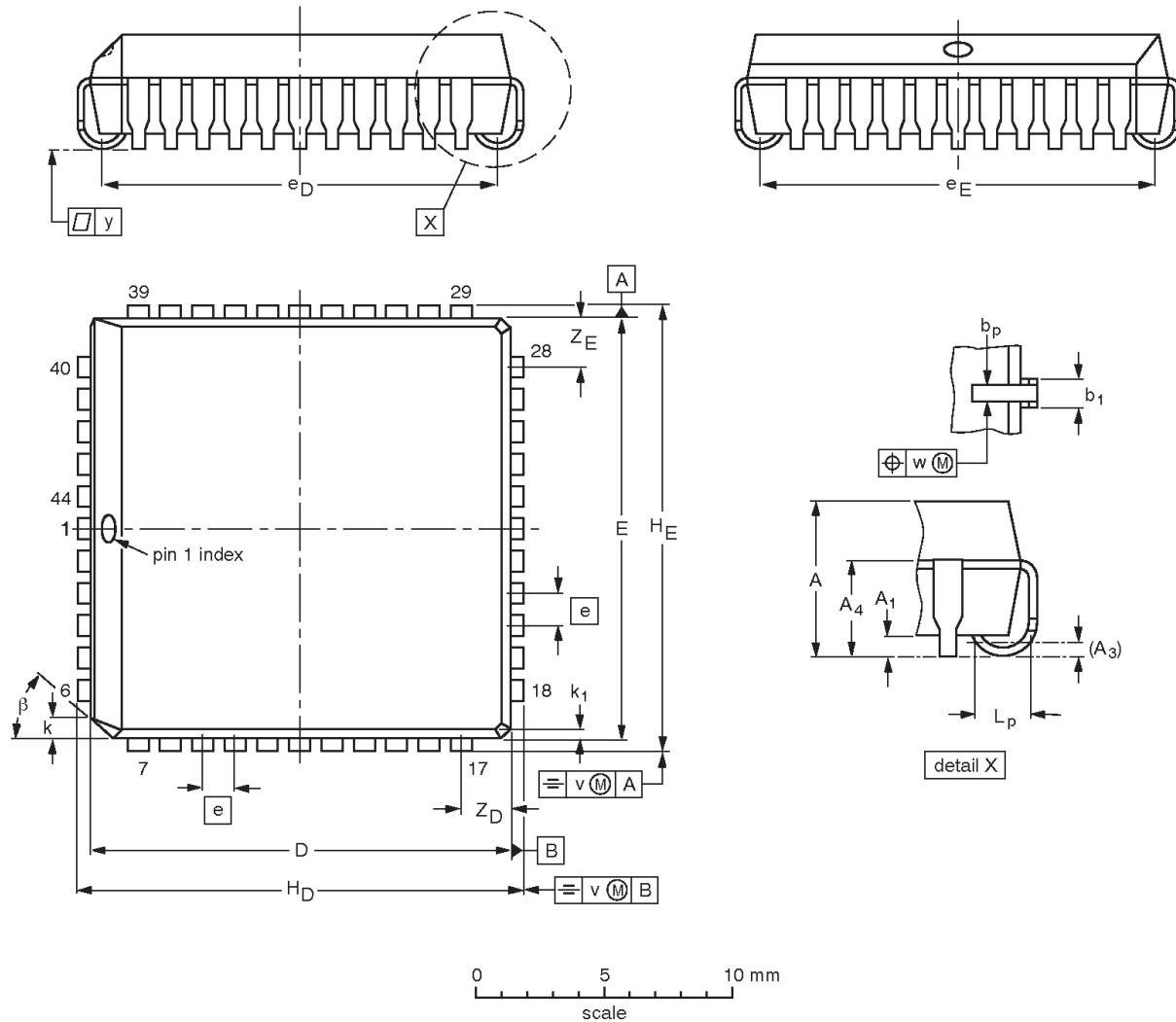
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT129-1 | 051G08 | MO-015AJ | | | | 92-11-17 95-01-14 |

CMOS single-chip 8-bit microcontrollers

80C652/83C652

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

| UNIT | A | A ₁ min. | A ₃ | A ₄ max. | b _p | b ₁ | D ⁽¹⁾ | E ⁽¹⁾ | e | e _D | e _E | H _D | H _E | k | k ₁ max. | L _p | v | w | y | Z _D ⁽¹⁾ max. | Z _E ⁽¹⁾ max. | β |
|--------|----------------|------------------------|----------------|------------------------|----------------|----------------|------------------|------------------|------|----------------|----------------|----------------|----------------|----------------|------------------------|----------------|-------|-------|-------|---------------------------------------|---------------------------------------|-----|
| mm | 4.57 4.19 | 0.51 | 0.25 | 3.05 | 0.53 0.33 | 0.81 0.66 | 16.66 16.51 | 16.66 16.51 | 1.27 | 16.00 14.99 | 16.00 14.99 | 17.65 17.40 | 17.65 17.40 | 1.22 1.07 | 0.51 | 1.44 1.02 | 0.18 | 0.18 | 0.10 | 2.16 | 2.16 | 45° |
| inches | 0.180 0.165 | 0.020 | 0.01 | 0.12 | 0.021 0.013 | 0.032 0.026 | 0.656 0.650 | 0.656 0.650 | 0.05 | 0.630 0.590 | 0.630 0.590 | 0.695 0.685 | 0.695 0.685 | 0.048 0.042 | 0.020 | 0.057 0.040 | 0.007 | 0.007 | 0.004 | 0.085 | 0.085 | |

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

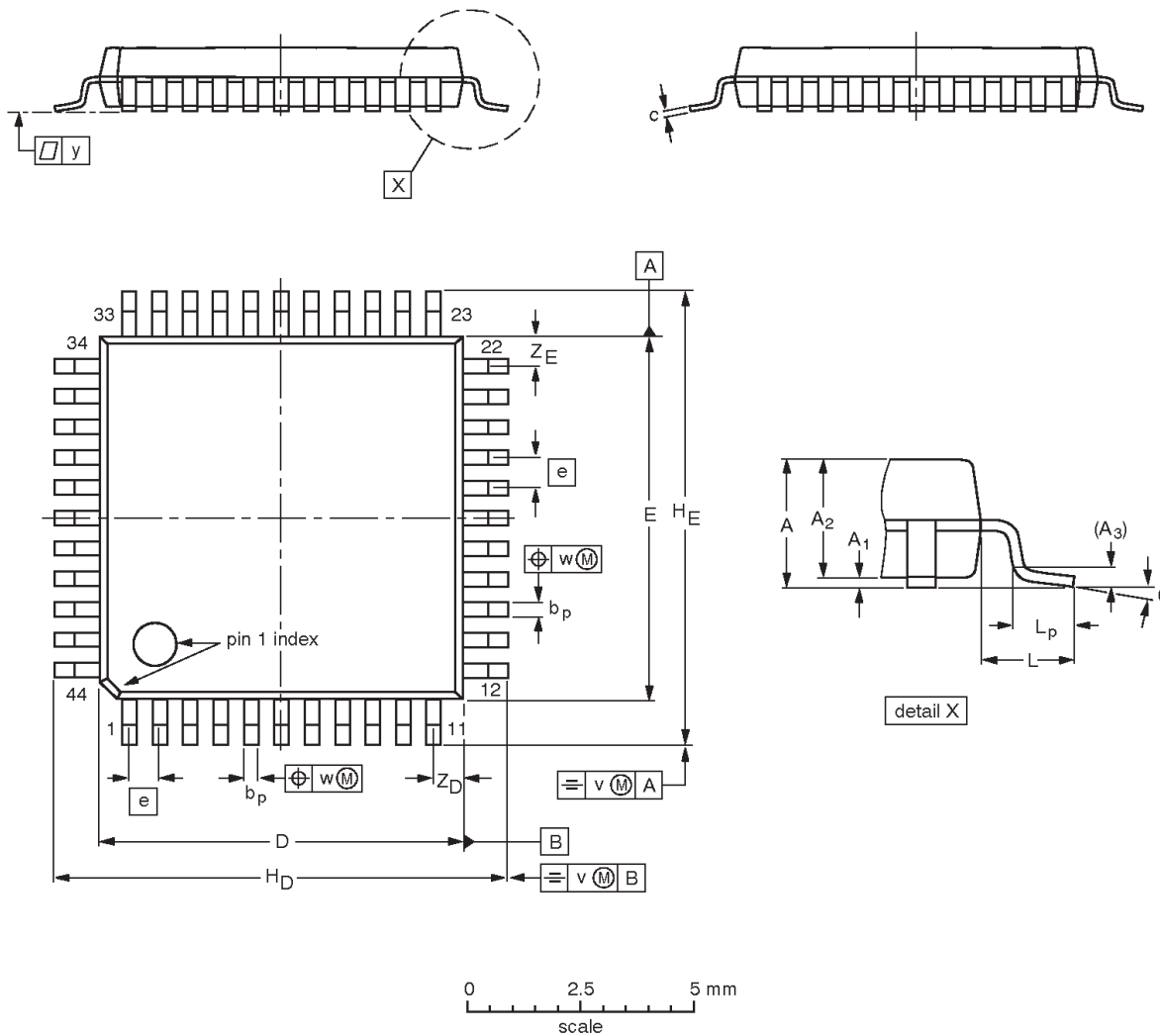
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT187-2 | 112E10 | MO-047AC | | | | 95-02-25 97-12-16 |

CMOS single-chip 8-bit microcontrollers

80C652/83C652

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _D | H _E | L | L _p | v | w | y | Z _D ⁽¹⁾ | Z _E ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|----------------|-----|----------------|------|------|-----|-------------------------------|-------------------------------|-----------|
| mm | 2.10 | 0.25 0.05 | 1.85 1.65 | 0.25 | 0.40 0.20 | 0.25 0.14 | 10.1 9.9 | 10.1 9.9 | 0.8 | 12.9 12.3 | 12.9 12.3 | 1.3 | 0.95 0.55 | 0.15 | 0.15 | 0.1 | 1.2 0.8 | 1.2 0.8 | 10° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT307-2 | | | | | | 95-02-04 97-08-01 |

CMOS single-chip 8-bit microcontrollers

80C652/83C652

Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1998
All rights reserved. Printed in U.S.A.

Date of release: 06-98

Document order number:

9397 750 04047

Let's make things better.