HS-81C55RH, HS-81C56RH

Radiation Hardened 256 x 8 CMOS RAM

March 1996

Features

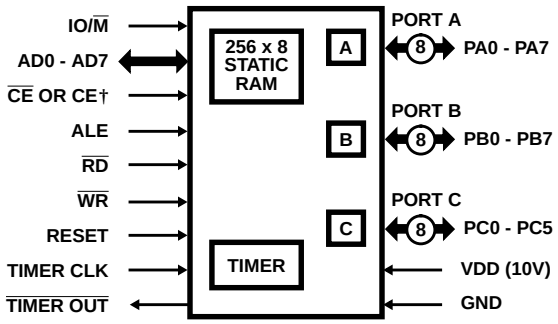
- **Devices QML Qualified in Accordance with MIL-PRF-38535**
- **Detailed Electrical and Screening Requirements are Contained in SMD# 5962-95818 and Intersil' QM Plan**
- **Radiation Hardened EPI-CMOS**
  - **Parametrics Guaranteed 1 x 10^5 RAD(Si)**
  - **Transient Upset > 1 x 10^8 RAD(Si)/s**
  - **Latch-Up Free > 1 x 10^{12} RAD(Si)/s**
- **Electrically Equivalent to Sandia SA 3001**
- **Pin Compatible with Intel 8155/56**
- **Bus Compatible with HS-80C85RH**
- **Single 5V Power Supply**
- **Low Standby Current 200μA Max**
- **Low Operating Current 2mA/MHz**
- **Completely Static Design**
- **Internal Address Latches**
- **Two Programmable 8-Bit I/O Ports**
- **One Programmable 6-Bit I/O Port**
- **Programmable 14-Bit Binary Counter/Timer**
- **Multiplexed Address and Data Bus**
- **Self Aligned Junction Isolated (SAJI) Process**
- **Military Temperature Range -55°C to +125°C**

Description

The HS-81C55/56RH are radiation hardened RAM and I/O chips fabricated using the Intersil radiation hardened Self-Aligned Junction Isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

The HS-81C55/56RH is intended for use with the HS-80C85RH radiation hardened microprocessor system. The RAM portion is designed as 2048 static cells organized as 256 x 8. A maximum post irradiation access time of 500ns allows the HS-81C55/56RH to be used with the HS-80C85RH CPU without any wait states. The HS-81C55RH requires an active low chip enable while the HS-81C56RH requires an active high chip enable. These chips are designed for operation utilizing a single 5V power supply.

Functional Diagram



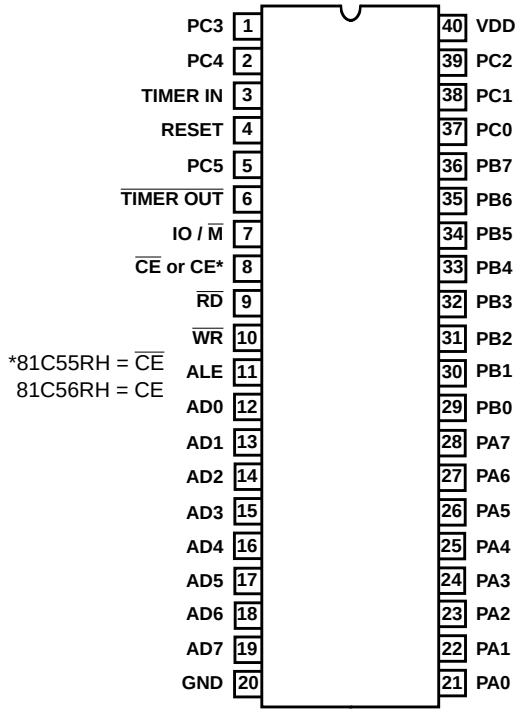
†81C55RH = $\overline{CE}$
81C56RH = CE

Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962R9XXXX01QRC	-55°C to +125°C	MIL-PRF-38535 Level Q	40 Lead SBDIP
5962R9XXXX01VRC	-55°C to +125°C	MIL-PRF-38535 Level V	40 Lead SBDIP
5962R9XXXX01QXC	-55°C to +125°C	MIL-PRF-38535 Level Q	42 Lead Ceramic Flatpack
5962R9XXXX01VXC	-55°C to +125°C	MIL-PRF-38535 Level V	42 Lead Ceramic Flatpack
5962R9XXXX02QRC	-55°C to +125°C	MIL-PRF-38535 Level Q	40 Lead SBDIP
5962R9XXXX02VRC	-55°C to +125°C	MIL-PRF-38535 Level V	40 Lead SBDIP
5962R9XXXX02QXC	-55°C to +125°C	MIL-PRF-38535 Level Q	42 Lead Ceramic Flatpack
5962R9XXXX02VXC	-55°C to +125°C	MIL-PRF-38535 Level V	42 Lead Ceramic Flatpack
HS1-81C55RH/Sample	+25°C	Sample	40 Lead SBDIP
HS9-81C55RH/Sample	+25°C	Sample	42 Lead Ceramic Flatpack
HS1-81C56RH/Sample	+25°C	Sample	40 Lead SBDIP
HS9-81C56RH/Sample	+25°C	Sample	42 Lead Ceramic Flatpack

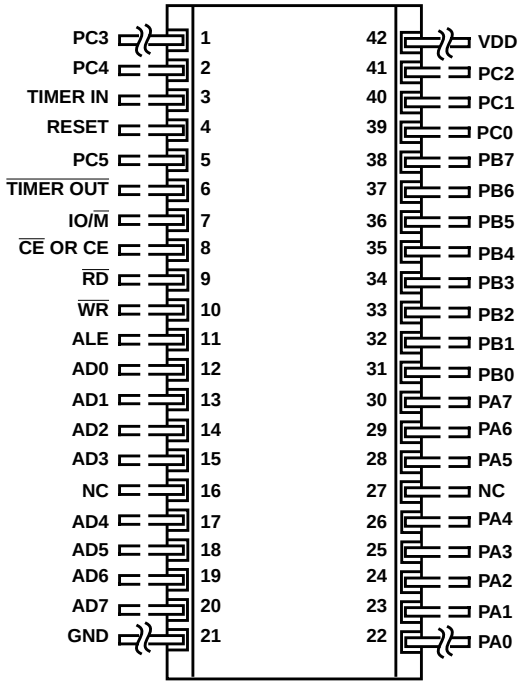
Pinouts

40 LEAD DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T40
TOP VIEW



*81C55RH = $\overline{CE}$
81C56RH = CE

42 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
INTERSIL OUTLINE K42.A
TOP VIEW



Pin Description

SYMBOL	TYPE	NAME AND FUNCTION
RESET	I	**Reset:** Pulse provided by the HS-80C85RH to initialize the system (connect to HS-80C85RH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two HS-80C85RH clock cycle times.
AD0 - AD7	I/O	**Address/Data:** Tri-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the HS-81C55 and HS-81C56RH on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
$\overline{CE}$ or CE	I	**Chip Enable:** On the HS-81C55RH, this pin is $\overline{CE}$ and is ACTIVE LOW. On the HS-81C56RH, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$	I	**Read Control:** Input low on this line with the Chip Enable active enables and AD0 - AD7 buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$	I	**Write Control:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{M}$.
ALE	I	**Address Latch Enable:** This control signal latches both the address on the AD0 - AD7 lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$	I	**I/O Memory:** Selects memory if low and I/O and command/status registers if high.
PA0 - PA7 (8)	I/O	**Port A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB0 - PB7 (8)	I/O	**Port B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC0 - PC7 (8)	I/O	**Port C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC0 - PC5 are used as control signals, they will provide the following: PC0 - A INTR (Port A Interrupt) PC1 - ABF (Port A Buffer Full) PC2 - $\overline{A}$ $\overline{STB}$ (Port A Strobe) PC3 - B INTR (Port B Interrupt) PC4 - B BF (Port B Buffer Full) PC5 - $\overline{B}$ $\overline{STB}$ (Port B Strobe)
TIMER IN	I	**Timer Input:** Input to the counter-timer.
$\overline{TIMER\ OUT}$	O	**Timer Output:** This output can be either a square wave or a pulse, depending on the timer mode.
VDD	I	**Voltage:** +5V.
GND	I	**Ground:** Ground reference.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . . -65^{o}C to +150^{o}C
Junction Temperature . . . . . +175^{o}C
Lead Temperature (Soldering 10s) . . . . . +300^{o}C
Typical Derating Factor . . . . . 2mA/MHz Increase in IDDOP
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	40.0^{o}C/W	5.0^{o}C/W
Ceramic Flatpack Package	45.0^{o}C/W	5.0^{o}C/W

Maximum Package Power Dissipation at +125^{o}C
SBDIP Package 1.25W
Ceramic Flatpack Package 1.11W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package . . . . . 25.0mW/^{o}C
Ceramic Flatpack Package . . . . . 22.2mW/^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.75V to +5.25V
Operating Temperature Range . . . . . -55^{o}C to +125^{o}C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VDD -0.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Input Leakage Current	IIH	VDD = 5.25V, VIN = 0V, Pin under test = VDD	1, 2, 3	-55^{o}C, +25^{o}C, +125^{o}C	-	1	µA
Low Input Leakage Current	IIL	VDD = 5.25V, VIN = 5.25V, Pin under test = 0V	1, 2, 3	-55^{o}C, +25^{o}C, +125^{o}C	-1	-	µA
Low Output Voltage	VOL	VDD = 5.25V, IOL = 2mA	1, 2, 3	-55^{o}C, +25^{o}C, +125^{o}C	-	0.5	V
High Output Voltage	VOH	VDD = 4.75V, IOH = 2mA	1, 2, 3	-55^{o}C, +25^{o}C, +125^{o}C	4.25	-	V
Static Current	IDDSB	VDD = 5.25V	1, 2, 3	-55^{o}C, +25^{o}C, +125^{o}C	-	200	µA
Dynamic Current	IDDOP	VDD = 5.25V, f = 1MHz	1, 2, 3	-55^{o}C, +25^{o}C, +125^{o}C	-	2	mA
Functional Tests	FT	VDD = 4.75V and 5.25V, VIH = VDD-0.5V, VIL = 0.8V	7, 8A, 8B	-55^{o}C, +25^{o}C, +125^{o}C	-	-	-

NOTE: All devices are guaranteed at worst case limits and over radiation. Dynamic current is proportional to operating frequency (2mA/MHz).

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Latch Setup Time	TAL	Notes 1, 4	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	60	-	ns
Address Hold Time After Latch	TLA	Notes 1, 4	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	60	-	ns
Latch to READ/WRITE Control	TLC	Notes 1, 4	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	200	-	ns
Valid Data Out From Read Control	TRD	Notes 1, 4	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	-	250	ns
Address Stable to Data Out Valid	TAD	Notes 1, 4	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	-	500	ns
Latch Enable Width	TLL	Notes 1, 4	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	200	-	ns
READ/WRITE Control to Latch Enable	TCL	Notes 1, 4,7	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	20	-	ns
READ/WRITE Control Width	TCC	Notes 1, 4	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	250	-	ns
Data In to WRITE Setup Time	TDW	Notes 1, 4	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	200	-	ns
Data In Hold Time After WRITE	TWD	Notes 1, 4	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	25	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
WRITE to Port Output	TWP	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	300	ns
Port Input Setup Time	TPR	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	ns
Port Input Hold Time	TRP	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	ns
Strobe to Buffer Full	TSBF	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	300	ns
Strobe Width	TSS	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	ns
READ to Buffer Empty	TRBE	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	300	ns
Strobe to INTR Off	TSI	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	300	ns
READ to INTR Off	TRDI	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$		360	ns
Port Setup Time to Strobe	TPSS	Notes 1, 4, 5	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	ns
Post Hold Time After Strobe	TPHS	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	ns
Strobe to Buffer Empty	TSBE	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	300	ns
WRITE to Buffer full	TWBF	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	300	ns
WRITE to INTR Off	TWI	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	340	ns
TIMER-IN to TIMER OUT Low	TTL	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	300	ns
TIMER-IN to TIMER-OUT High	TTH	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	300	ns
Data Bus Enable from READ Control	TRDE	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	ns
TIMER-IN Low Time	T1	Notes 1, 4, 6	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	ns
TIMER-IN High Time	T2	Notes 1, 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	115	-	ns

NOTES:

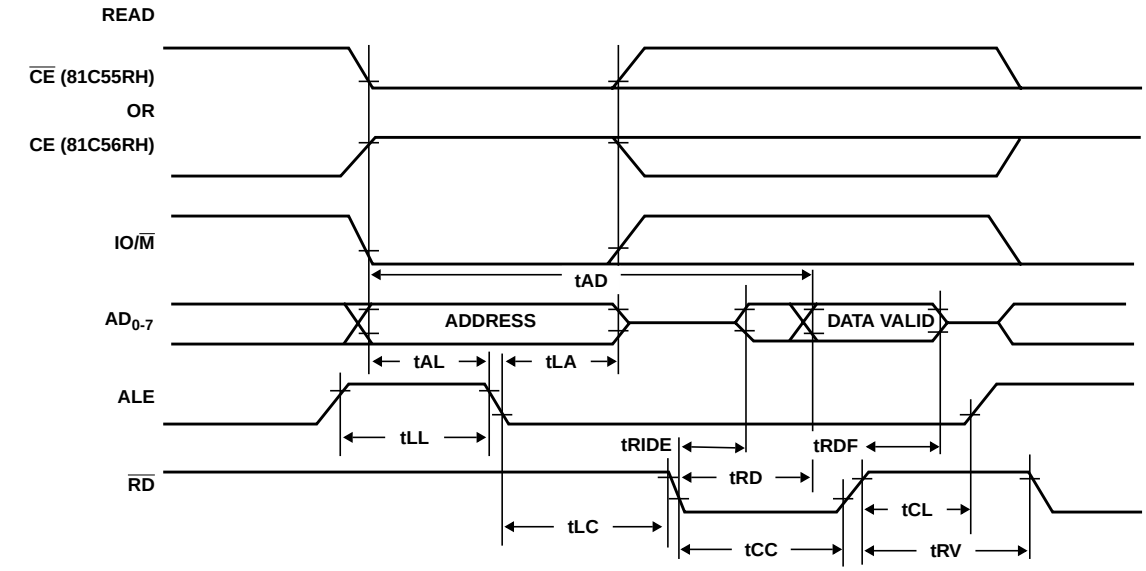
1. All devices guaranteed at worst case limits and over radiation.
2. Operating supply current (IDDOP) is proportional to operating frequency.
3. Output timings are measured with purely capacitive load.
4. For design purposes the limits are given as shown. For compatibility with the 80C85RH microprocessor, the AC parameters are tested as maximums.
5. Parameter tested as part of the functional test. No read and record data available.
6. At low temperature, T1 is measured down to 10ns. If the reading is less than 10ns, the parameter will read 10ns.
7. Read and Record data available on failing data only.

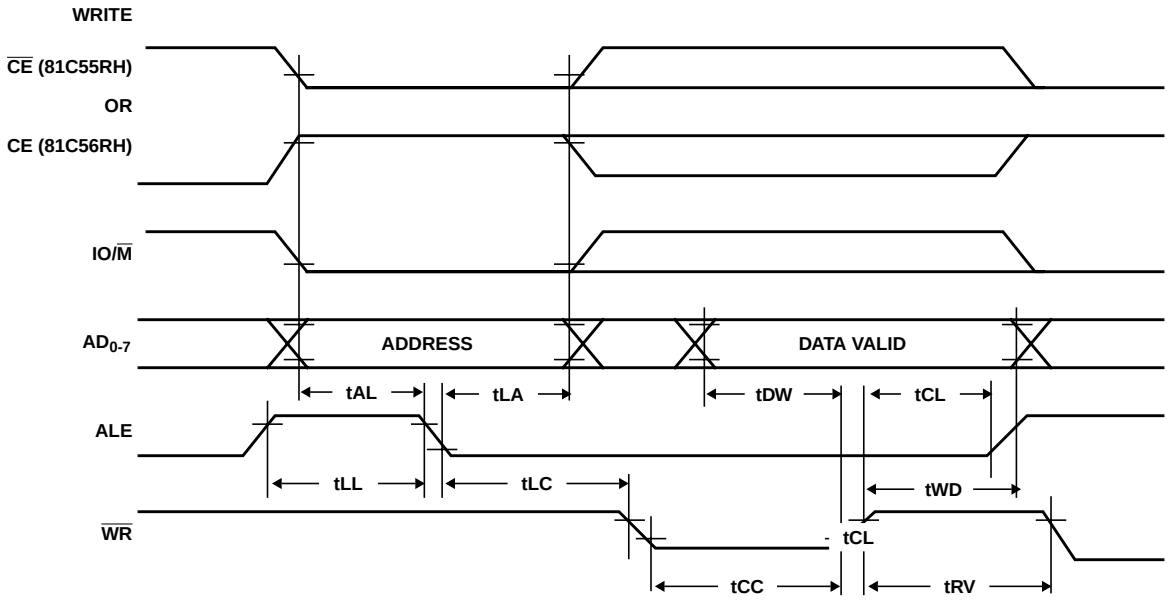
TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz, All measurements referenced to device ground	$T_A = +25^oC$	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz, All measurements referenced to device ground	$T_A = +25^oC$	-	10	pF
Data Bus Float After READ	TRDF	VDD = 4.75V	-55^oC, $+25^oC$, $+125^oC$	10	100	ns
Recovery Time Between Controls	TRV	VDD = 4.75V	-55^oC, $+25^oC$, $+125^oC$	-	220	ns

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

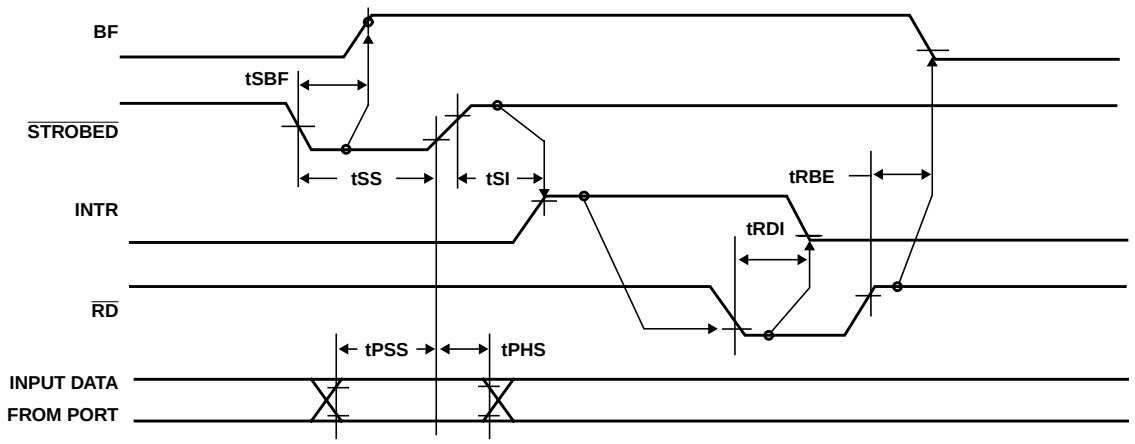
Waveforms


READ
CE (81C55RH)
OR
CE (81C56RH)
IO/M
tAD
AD0-7
ADDRESS
DATA VALID
tAL
tLA
ALE
tLL
tRIDE
tRDF
RD
tRD
tCL
tLC
tCC
tRV

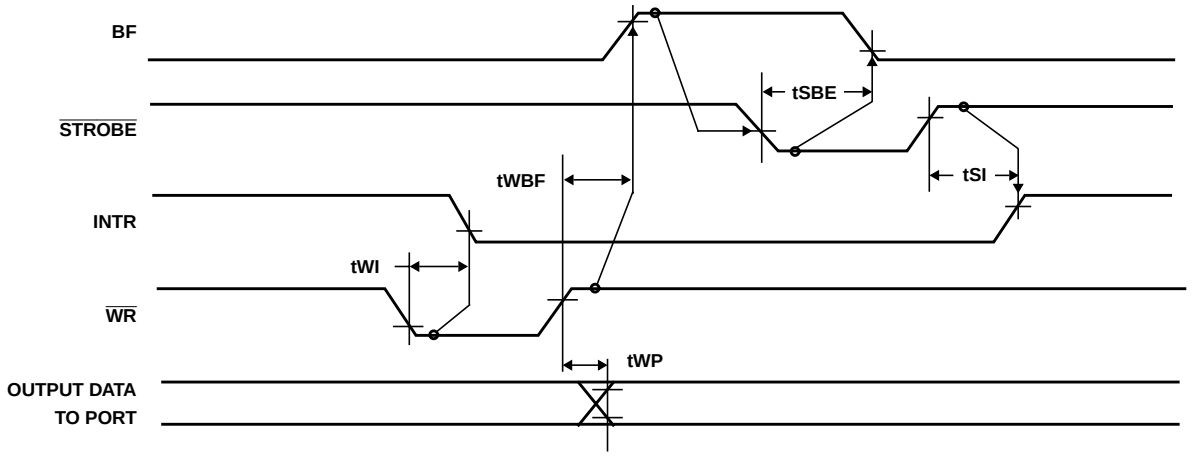

WRITE
CE (81C55RH)
OR
CE (81C56RH)
IO/M
AD0-7
ADDRESS
DATA VALID
tAL
tLA
tDW
tCL
ALE
tLL
tLC
tWD
WR
tCL
tCC
tRV

Waveforms (Continued)

STROBED INPUT

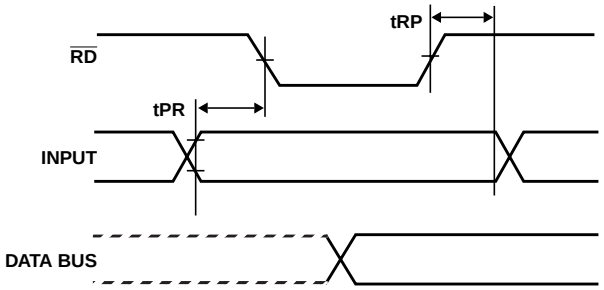


STROBED OUTPUT

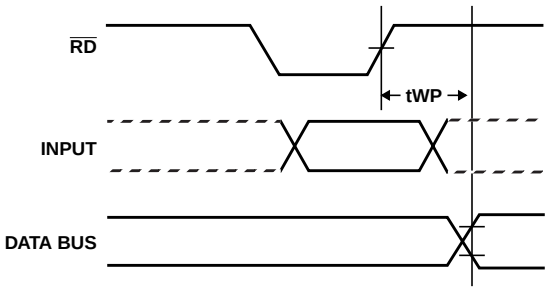


Waveforms (Continued)

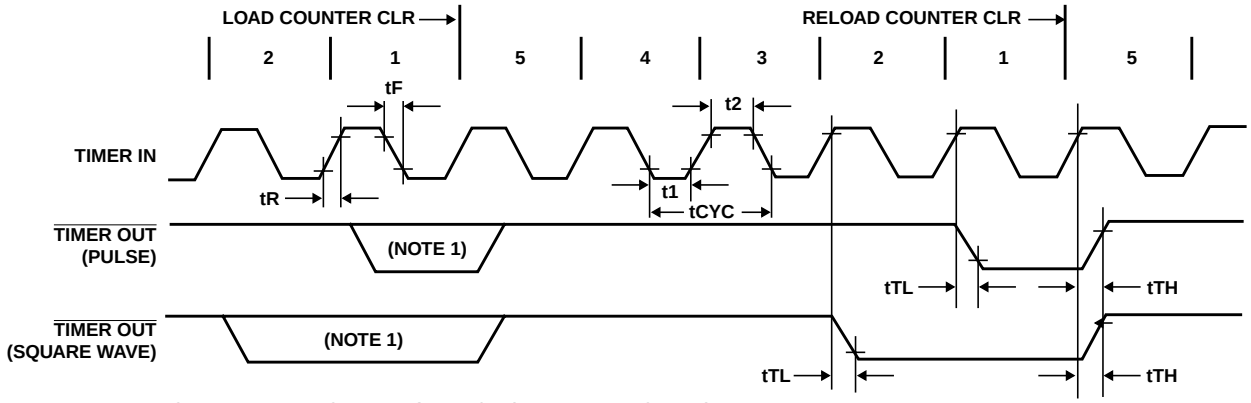
BASIC INPUT



BASIC INPUT



TIMER OUTPUT COUNTDOWN FROM 5 TO 1



NOTE: THE TIMER OUTPUT IS PERIODIC IF IN AN AUTOMATIC RELOAD MODE (M, MODE BIT = 1)

Metallization Topology

DIE DIMENSIONS:

222 x 202 x 14 ± 1mil (Die Thickness)

METALLIZATION:

Type: AlSi

Thickness: 11kÅ ± 2kÅ

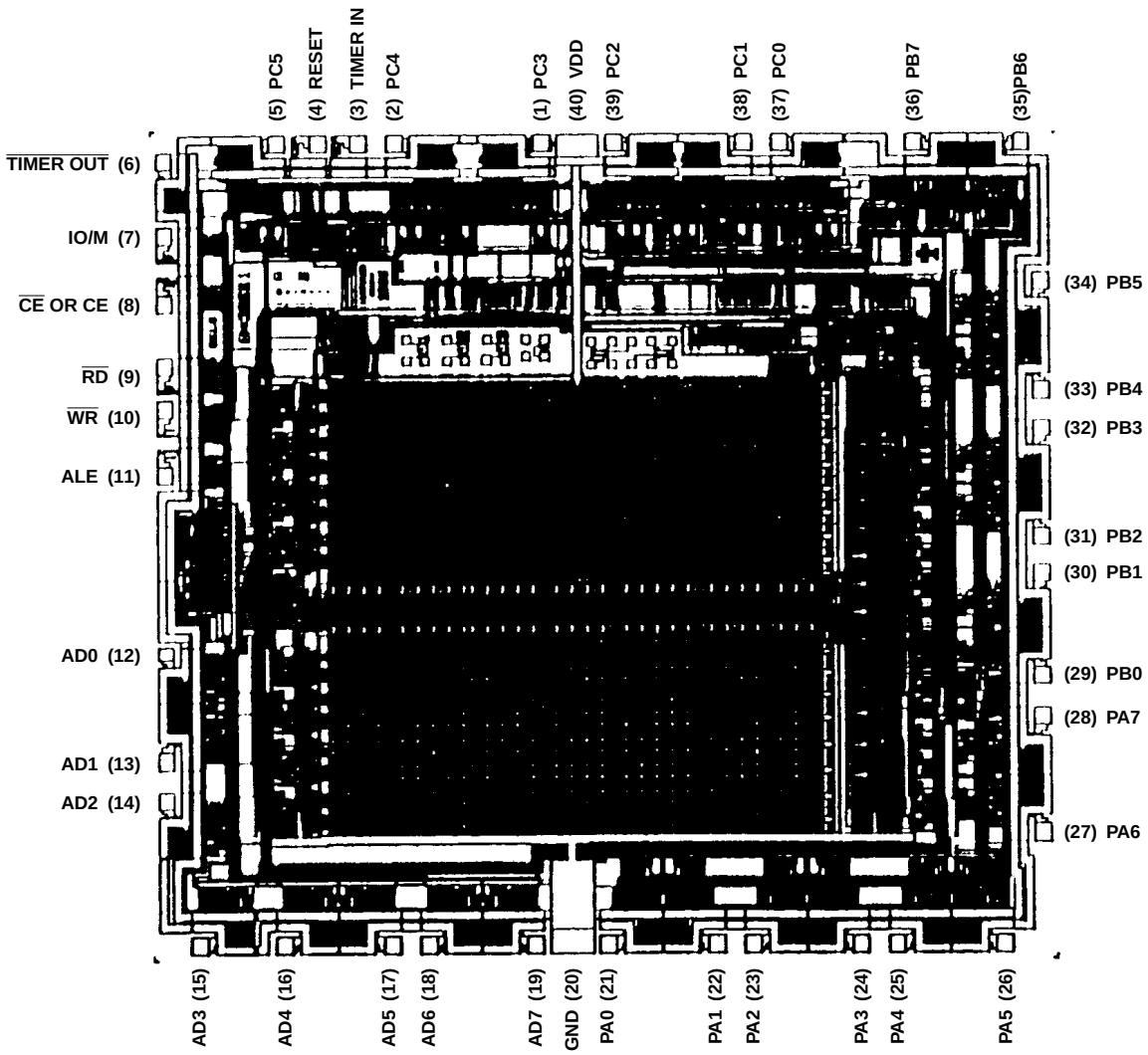
GLASSIVATION:

Type: SiO2

Thickness: 8kÅ ± 1kÅ

Metallization Mask Layout

HS-81C55RH, HS-81C56RH



Functional Description

The HS-81C55RH and 81C56RH contains the following:

- 2K Bit Static RAM Organized as 256 x 8
- Two 8-Bit I/O Ports (PA and PB) and One 6-Bit I/O Port (PC)
- 14-Bit Timer-Counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five register (Command, Status, PA0 - PA7, PB0 - PB7, PC0 - PC5) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input $\overline{CE}$ or CE and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

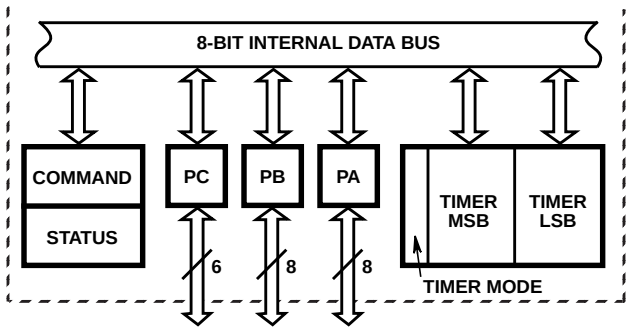


FIGURE 1. INTERNAL REGISTERS

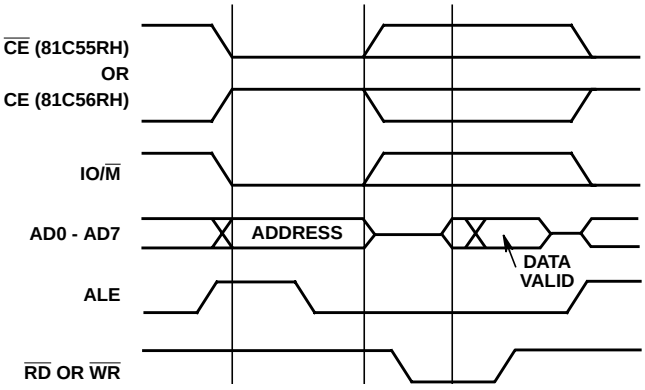


FIGURE 2. ON-BOARD MEMORY READ/WRITE CYCLE

Programming of the Command Register

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bit (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at anytime by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 3. The contents of the command register may never be read.

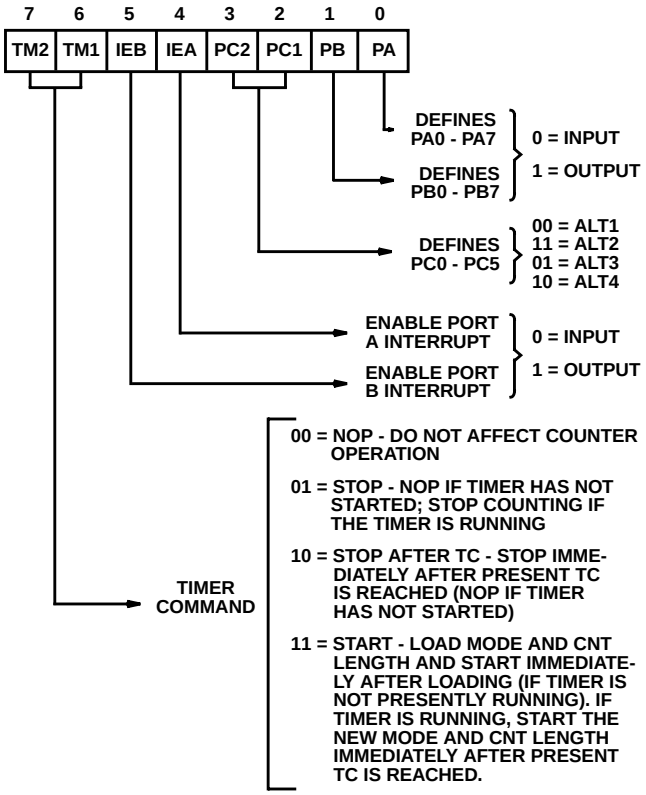


FIGURE 3. COMMAND REGISTER BIT ASSIGNMENT

Reading the Status Register

The status register consists of seven latches, one for each bit six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 4. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

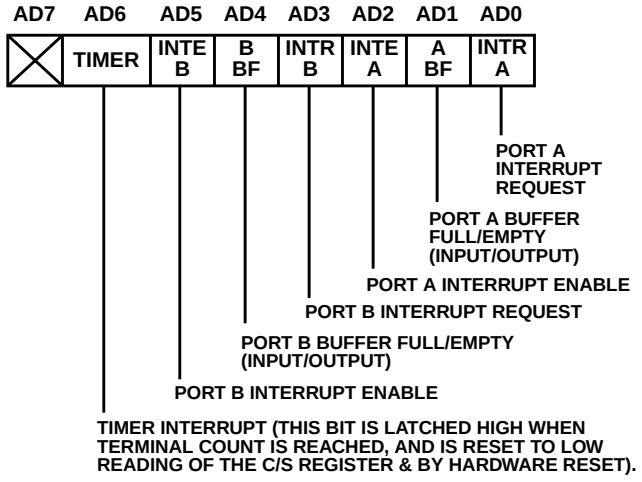


FIGURE 4. STATUS REGISTER BIT ASSIGNMENT

Input/Output Section

The I/O section of the HS-81C55RH and HS-81C56RH consists of five registers: (See Figure 5)

- **Command/Status Register (C/S)** - Both register are assigned the address XXXXX000. The C/S address serves the dual prupose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are not accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD0 - AD7 lines.

- **PA Register** - This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). the I/O pins assigned in relation to this register are PA0 - PA7. The address of this register is XXXXX001.

- **PB Register -** This register functions the same as PA Register. the I/O pins assigned are PB0 - PB7. The address of this register is XXXXX010

- **PC Register -** This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD2 and AD3 bits of the C/S register.

  When PC0 - PC5 is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an Interrupt that the HS-81C55RH and HS-81C56RH sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 1).

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and Pb are initialized as follows: :

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS†								
A7	A6	A5	A4	A3	A2	A1	A0	SELECTION
X	X	X	X	X	0	0	0	Interval Command/ Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	General Purpose I/O or Control Port C
X	X	X	X	X	1	0	0	Low-Order 8 Bits of Timer Count
X	X	X	X	X	1	0	1	High 6 Bits of Timer Count and 2 Bits of Timer Mode

† I/O Address must be qualified by CE = 1(81C56RH) or $\overline{CE}$ = 0(81C55RH) and IO/$\overline{M}$ = 1 in order to select the appropriate register.
X = Don't Care

FIGURE 5. I/O PORT AND TIMER ADDRESSING SCHEME

Figure 6 shows how I/O Ports A and B are structured within the HS-81C55RH and HS-81C56RH.

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

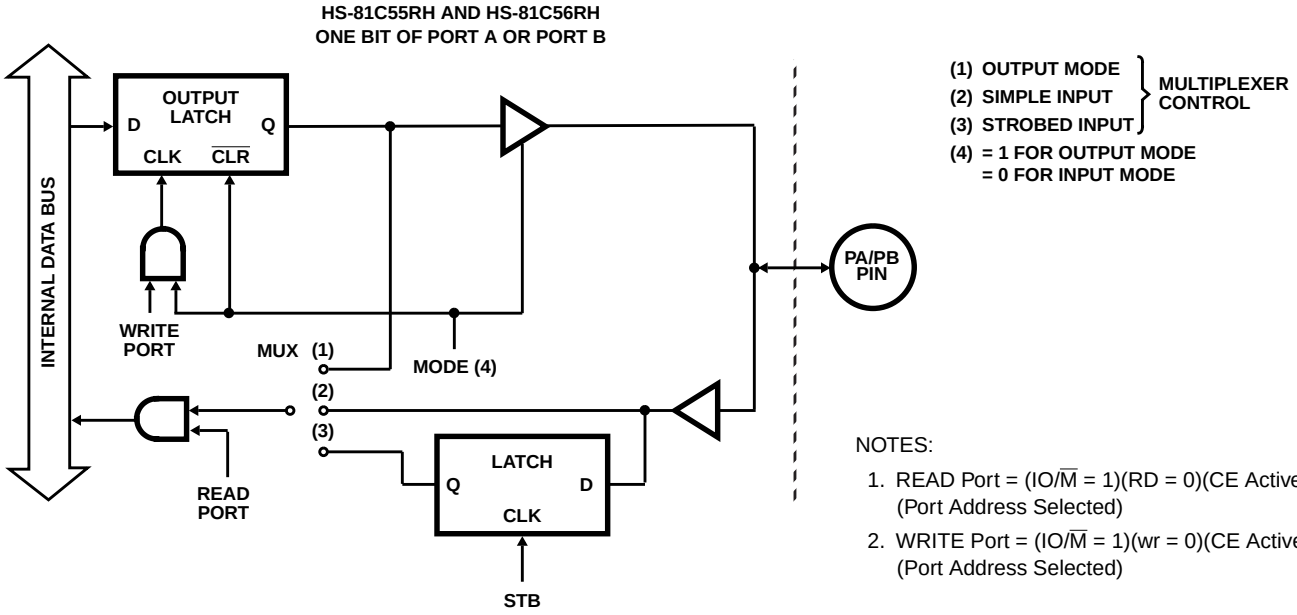


FIGURE 6. HS-81C55RH AND HS-81C56RH PORT FUNCTION

The outputs of the HS-81C55/56RH are “glitch-free” meaning that you can write a “1” to a bit position that was previously “1” and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. the output latch cannot be loaded by writing to the port if the port is in theinput mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the HS-81C55/56RH is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT1 or ALT2 modes, the bits of Port C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 7 shows how the HS-81C55/56RH I/O ports might be configured in a typical system.

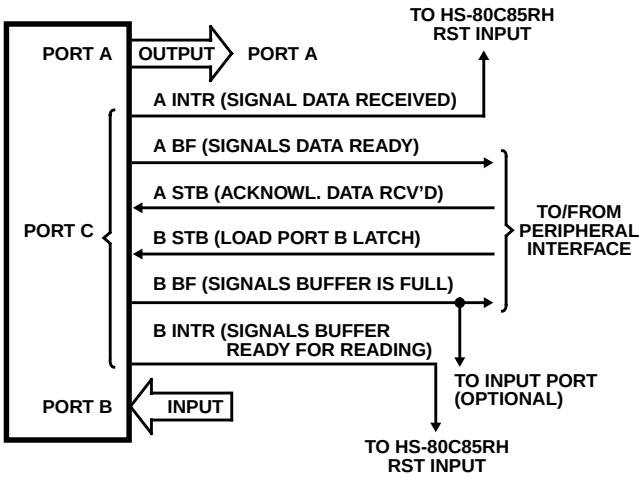


FIGURE 7. EXAMPLE: COMMAND REGISTER = 00111001

Timer Section

The timer is a 14 bit down counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 5).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 8). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0-13.

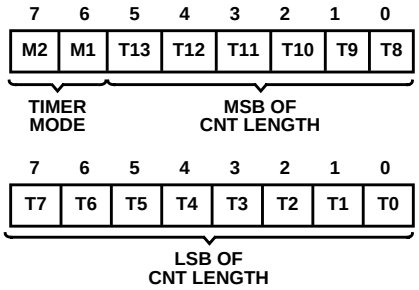


FIGURE 8. TIMER FORMAT

TABLE 1. PORT CONTROL ASSIGNMENT

PIN	ALT1	ALT2	ALT3	ALT4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A STB (Port A Strobe)	A STB (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B STB (Port B Strobe)

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 9.

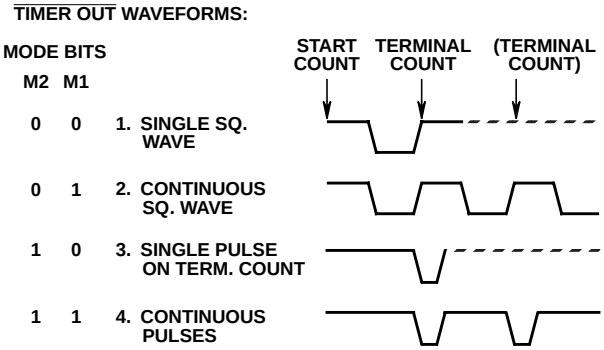


FIGURE 9. TIMER MODES

Bits 6-7 (TM2 and TM1) of command register contents are used to start and stop the counter. there are four commands to choose from:

TM2	TM1	
0	0	NOP - Do not affect counter operation
0	1	STOP-NOP - If timer has not started; stop counting if the timer is running
1	0	STOP AFTER TC - Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START - Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you *must* issue a START command to the counter. This applies even thought you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 10.

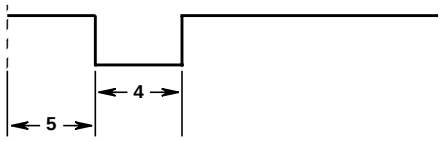


FIGURE 10. ASYMMETRICAL SQUARE-WAVE OUTPUT RESULTING FROM COUNT OF 9

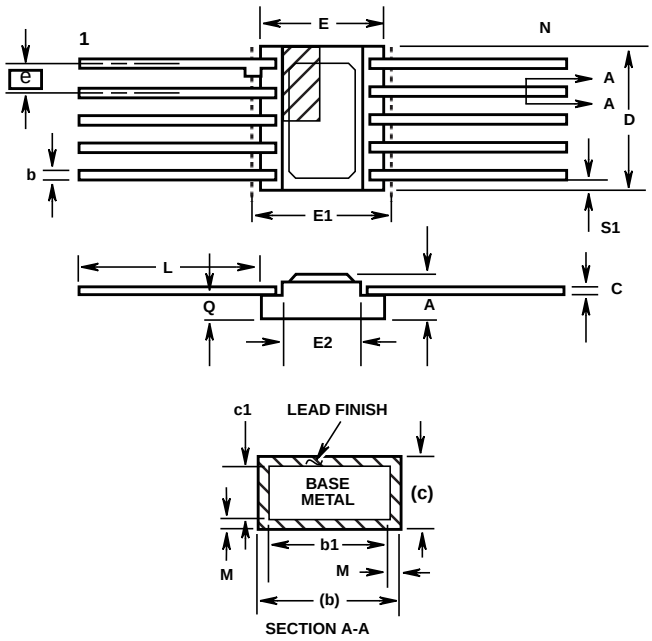
The counter in the HS-81C55/56RH is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the HS-81C55/56RH chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the HS-80C85RH be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16 bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count - 1 if full count is odd).

NOTE: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the HS-81C55/56RH always counts out the right number of pulses in generating the TIMER OUT waveforms.

Ceramic Metal Seal Flatpack Packages (Flatpack)



K42.A TOP BRAZED
42 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.100	-	2.54	-
b	0.017	0.025	0.43	0.64	-
b1	0.017	0.023	0.43	0.58	-
c	0.007	0.013	0.18	0.33	-
c1	0.007	0.010	0.18	0.25	-
D	1.045	1.075	26.54	27.31	3
E	0.630	0.650	16.00	16.51	-
E1	-	0.680	-	17.27	3
E2	0.530	0.550	13.46	13.97	-
e	0.050 BSC		1.27 BSC		11
k	-	-	-	-	-
L	0.320	0.350	8.13	8.89	-
Q	0.045	0.065	1.14	1.65	8
S1	0.000	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	42		42		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.
11. The basic lead spacing is 0.050 inch (1.27mm) between center lines. Each lead centerline shall be located within ±0.005 inch (0.13mm) of its exact longitudinal position relative to lead 1 and the highest numbered (N) lead.

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