Document Title

4 Mbit CMOS 3.3 Volt-only Low Pin Count Flash Memory

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	February 17, 2004	Preliminary
0.1	Add Pb-Free package type	August 20, 2004	

A49LF040

4 Mbit CMOS 3.3Volt-only Low Pin Count Flash Memory

Preliminary

FEATURES

• Single Power Supply Operation
- Low voltage range: 3.0 V - 3.6 V for Read and Write Operations

• Standard Intel Low Pin Count Interface
- Read compatible to Intel® Low Pin Count (LPC) interface

• Memory Configuration
- 512K x 8 (4 Mbit)

• Block Architecture
- 4Mbit: eight uniform 64KByte blocks
- Supports full chip erase for Address/Address Multiplexed (A/A Mux) mode

• Automatic Erase and Program Operation
- Embedded Byte Program and Block/Chip Erase algorithms
- Typical 10 µs/byte programming time
- Typical 1s block erase time

• Two Operational Modes
- Low Pin Count Interface (LPC) Mode for in-system operation
- Address/Address Multiplexed (A/A Mux) Interface Mode for programming equipment

• Low Pin Count (LPC) Mode
- 33 MHz synchronous operation with PCI bus
- 5-signal communication interface for in-system read and write operations
- Standard SDP Command Set
- Data# Polling (I/O_7) and Toggle Bit (I/O_6) features
- 4 ID pins for multi-chip selection
- 5 GPI pins for General Purpose Input Register
- TBL# pin for hardware write protection to Boot Block
- WP# pin for hardware write protection to whole memory array except Boot Block

• Address/Address Multiplexed (A/A Mux) Mode
- 11-pin multiplexed address and 8-pin data I/O interface
- Supports fast programming on EPROM programmers
- Standard SDP Command Set
- Data# Polling (I/O_7) and Toggle Bit (I/O_6) features

• Lower Power Consumption
- Typical 12mA active read current
- Typical 24mA program/erase current

• High Product Endurance
- Guarantee 100,000 program/erase cycles for each block
- Minimum 20 years data retention

• Compatible Pin-out and Packaging
- 32-pin (8 mm x 14 mm) TSOP (TYPE I)
- 32-pin PLCC

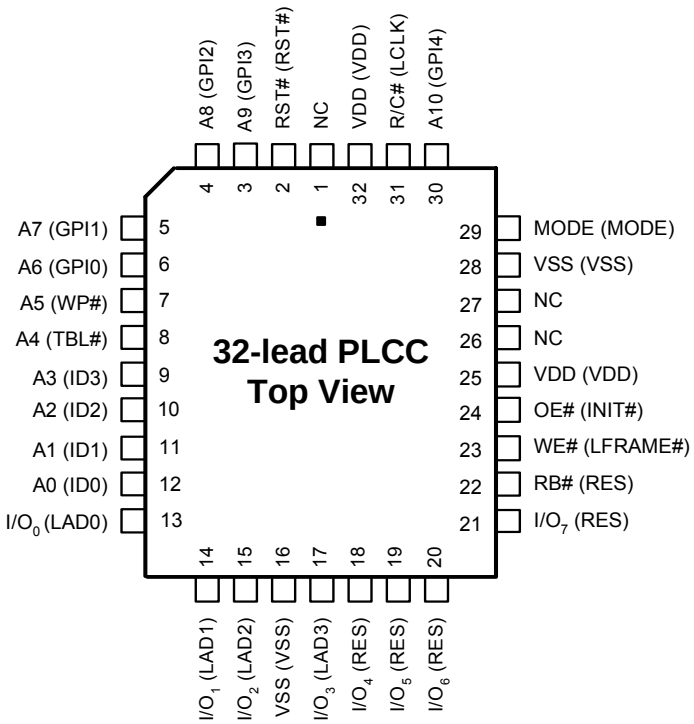
GENERAL DESCRIPTION

The A49LF040 flash memory device is designed to be read-compatible with the Intel Low Pin Count (LPC) Interface Specification 1.1. This device is designed to use a single low voltage, range from 3.0 Volt to 3.6 Volt power supply to perform in-system or off-system read and write operations. It provides protection for the storage and update of code and data in addition to adding system design flexibility through five general-purpose inputs. Two interface modes are supported by the A49LF040: Low Pin Count (LPC) Interface mode for In-System programming and Address/Address Multiplexed (A/A Mux) mode for fast factory programming of PC-BIOS applications.

The memory is divided into eight uniform 64Kbyte blocks that can be erased independently without affecting the data in other blocks. Blocks also can be protected individually to prevent accidental Program or Erase commands from modifying the memory. The Program and Erase operations are executed by issuing the Program/Erase commands into the command interface by which activating the internal control logic to automatically process the Program/Erase procedures. The device can be programmed on a byte-by-byte basis after performing the Erase operation. In addition to the Block Erase operation, the Chip Erase feature is provided in A/A Mux mode that allows the whole memory to be erased in one single Erase operation. The A49LF040 provides the status detection such as Data# Polling and Toggle Bit Functions in both LPC and A/A Mux modes. The process or completion of Program and Erase operations can be detected by reading the status bits.

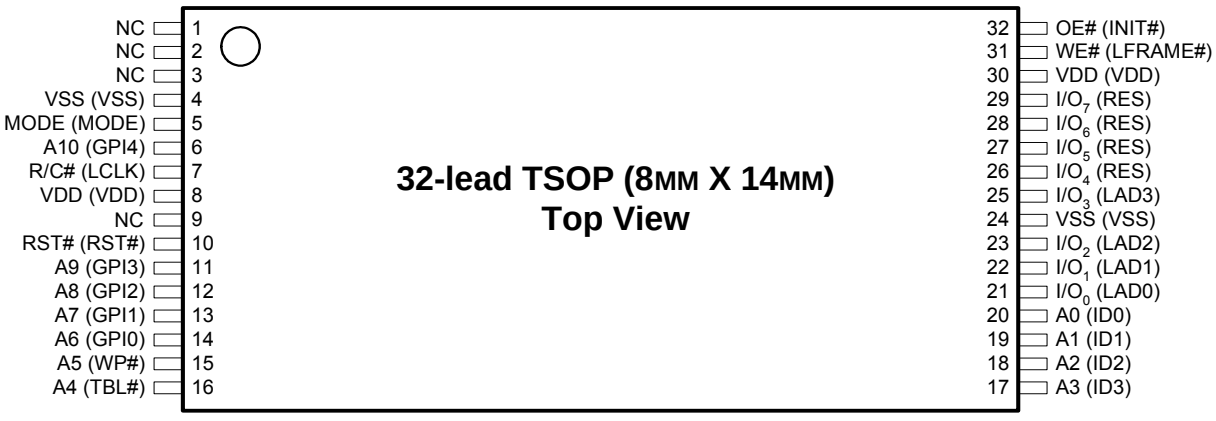
The A49LF040 is offered in 32-lead TSOP and 32-lead PLCC packages. See Figures 1 and 2 for pin assignments and Table 1 for pin descriptions.

PIN CONFIGURATIONS



(*) Designates LPC Mode

FIGURE 1: Pin Assignments for 32-Lead PLCC



(*) Designates LPC Mode

FIGURE 2: Pin Assignments for 32-Lead TSOP

BLOCK DIAGRAM

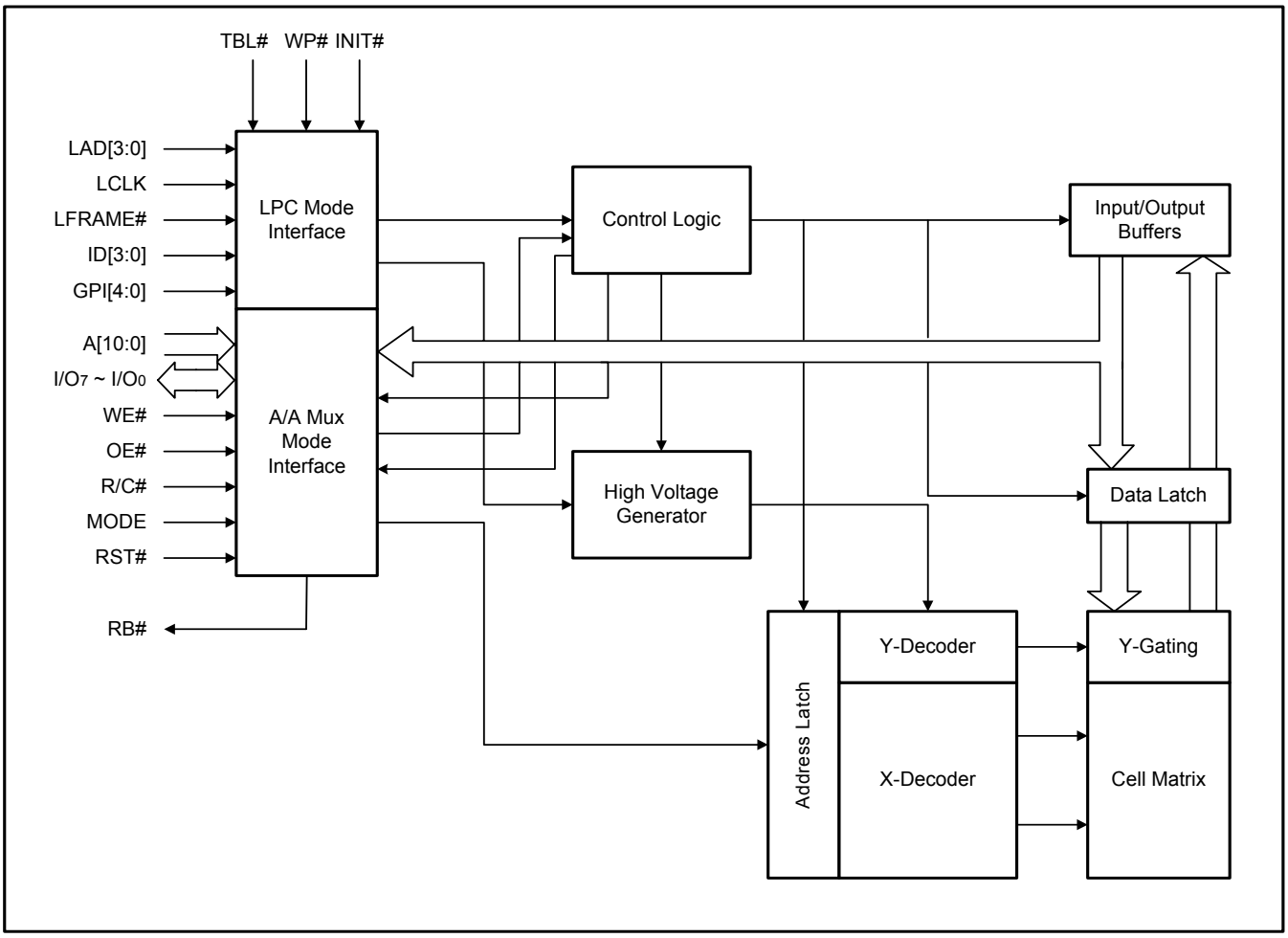


Table 1: Pin Description

Symbol	Pin Name	Type	Interface		Descriptions
			A/A Mux	LPC	
A_{10}-A_0	Address	IN	X		Inputs for addresses during Read and Write operations in A/A Mux mode. Row and column addresses are latched by R/C# pin.
I/O_7-I/O_0	Data	I/O	X		To output data during Read cycle and receive input data during Write cycle in A/A Mux mode. The outputs are in tri-state when OE# is high.
OE#	Output Enable	IN	X		To control the data output buffers.
WE#	Write Enable	IN	X		To control the Write operations.
MODE	Interface Configuration Pin	IN	X	X	To determine which interface is operational. When held high, A/A Mux mode is enabled and when held low, LPC mode is enabled. This pin must be setup at power-up or before return from reset and not change during device operation. This pin is internally pulled down with a resistor between 20-100 KΩ.
INIT#	Initialize	IN		X	This is the second reset pin for in-system use. INIT# and RST# pins are internally combined and initialize a device reset when driven low.
ID[3:0]	Identification Inputs	IN		X	These four pins are part of the mechanism that allows multiple LPC devices to be attached to the same bus. To identify the component, the correct strapping of these pins must be set. The boot device must have ID[3:0]=0000 and it is recommended that all subsequent devices should use sequential up-count strapping. These pins are internally pulled down with a resistor between 20-100 KΩ.
GPI[4:0]	General Purpose Inputs	IN		X	These individual inputs can be used for additional board flexibility. The state of these pins can be read immediately at boot, through LPC internal registers. These inputs should be at their desired state before the start of the PCI clock cycle during which the read is attempted, and should remain in place until the end of the Read cycle. Unused GPI pins must not be floated.
TBL#	Top Block Lock	IN		X	To prevent any write operations to the Boot Block when driven low, regardless of the state of the block lock registers. When TBL# is high it disables hardware write protection for the top Boot Block. This pin cannot be left unconnected.
LAD[3:0]	LPC I/Os	I/O		X	I/O Communications in LPC mode.
LCLK	Clock	IN		X	To provide a clock input to the device. This pin is the same as that for the PCI clock and adheres to the PCI specifications.
LFRAME#	Frame	IN		X	To indicate start of a data transfer operation; also used to abort an LPC cycle in progress.
RST#	Reset	IN	X	X	To reset the operation of the device
WP#	Write Protect	IN		X	When low, prevents any write operations to all but the highest addressable block. When WP# is high it disables hardware write protection for these blocks. This pin cannot be left unconnected.
R/C#	Row/Column Select	IN	X		This pin determines whether the address pins are pointing to the row addresses or the column addresses in A/A Mux mode.
RB#	Ready/Busy#	OUT	X		To determine if the device is busy in write operations. Valid only in A/A Mux mode.
RES	Reserved			X	Reserved. These pins must be left unconnected.
VDD	Power Supply	PWR	X	X	To provide power supply (3.0-3.6Volt).
VSS	Ground	PWR	X	X	Circuit ground. All VSS pins must be grounded.
NC	No Connection		X	X	Unconnected pins.

1. IN=Input, OUT=output, I/O=Input/Output, PWR=Power

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . -55°C to + 125°C
Storage Temperature . . . . . -65°C to + 125°C
D.C. Voltage on Any Pins with Respect to Ground [1]
. . . . -0.5V to VDD + 0.5V
Package Power Dissipation Capability (Ta=25°C)
. . . . -0.5V to VDD + 0.5V
Output Short Circuit Current [2] 50mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot VSS to -2.0V for periods of up to 20ns. Maximum DC voltage on input and I/O pins is VDD + 0.5V. During voltage transitions, input or I/O pins may overshoot to VDD + 2.0V for periods up to 20ns.
2. No more than one output is shorted at a time. Duration of the short circuit should not be greater than one second.

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specifications are not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices

Ambient Temperature (T_A) . . . . 0°C to +85°C

VDD Supply Voltages

VDD for all devices . . . . +3.0V to +3.6V
Operating ranges define those limits between which the functionally of the device is guaranteed.

MODE SELECTION

The A49LF040 flash memory devices can operate in two distinct interface modes: the Low Pin Count Interface (LPC) mode and the Address/Address Multiplexed (A/A Mux) mode. The Mode pin is used to set the interface mode selection. If the Mode pin is set to logic High, the device is in A/A Mux mode; while if the Mode pin is set Low, the device is in the LPC mode. The Mode pin must be configured prior to device operation. The Mode pin is internally pulled down if the pin is not connected. In LPC mode, the device is configured to interface with its host using Intel's Low Pin Count proprietary protocol. Communication between Host and the A49LF040 occurs via the 4-bit I/O communication signals, LAD[3:0] and the LFRAME#. In A/A Mux mode, the device is programmed via an 11-bit address A_{10}-A_0 and an 8-bit data I/O_7-I/O_0 parallel signals. The address inputs are multiplexed in row and column selected by control signal R/C# pin. The column addresses are mapped to the higher internal addresses, and the row addresses are mapped to the lower internal addresses. See the Device Memory Maps in Figure 3 for address assignment.

LPC MODE OPERATION

The LPC interface consists of four data signals (LAD[3:0]), one control signal (LFRAME#) and a clock (LCLK). The data signals, control signal and clock comply with PCI specifications. Operations such as Memory Read and Memory Write use Intel LPC propriety protocol. JEDEC Standard SDP (Software Data Protection) Byte-Program and Block-Erase command sequences are incorporated into the LPC memory cycles. Chip-Erase command is only available in A/A Mux mode. The addresses and data are transferred through LAD[3:0] synchronized with the input clock LCLK during a LPC memory cycle. The pulse of LFRAME# is inserted for at least one clock period to indicate the start of a LPC memory cycle. The address or data on LAD[3:0] is latched on the rising edge of LCLK. The device enters standby mode when LFRAME# is high and no internal operation is in progress. The device is in ready mode when LFRAME# is low and no activity is on the LPC bus.

LPC Read Operation

LPC Read operations read from the memory cells or specific registers in the LPC device. A valid LPC Read operation starts when LFRAME# is Low as LCLK rises and a START value "0000b" is on LAD[3:0] then the next nibble "010X" is on LAD[3:0]. Addresses and data are transferred to and from the device decided by a series of "fields". Field sequences and contents are strictly defined for LPC Read operations. Refer to Table 2 for LPC Read Cycle Definition.

LPC Write Operation

LPC Write operations write to the LPC Interface or LPC registers. A valid LPC Write operation starts when LFRAME# is Low as LCLK rises and a START value "0000b" is on LAD[3:0] then the next nibble "011X" is on LAD[3:0]. Addresses and data are transferred to and from the device decided by a series of "fields". Field sequences and contents are strictly defined for LPC Write operations. Refer to Table 3 for LPC write Cycle Definition.

LPC Abort Operation

If LFRAME# is driven low for one or more clock cycles during a LPC cycle, the cycle will be terminated and the device will wait for the ABORT command. The host may drive the LAD[3:0] with '1111b' (ABORT command) to return the device to Ready mode. If abort occurs during a Write operation such as checking the operation status with Data# Polling (I/O_7) or Toggle Bit (I/O_6) pins, the read status cycle will be aborted but the internal write operation will not be affected. In this case, only the reset operation initiated by RST# or INIT# pin can terminate the Write operation..

Response To Invalid Fields

During LPC operations, the LPC will not explicitly indicate that it has received invalid field sequences. The response to specific invalid fields or sequences is as follows:

Address out of range: The A49LF040 will only response to address range as specified in Table 4. Address A22 has the special function of directing reads and writes to the flash memory (A22=1) or to the register space (A22=0).

Table 2: LPC Read Cycle

Clock Cycle	Field Name	Field Contents LAD[3:0][1]	LAD[3:0] Direction	Comments
1	START	0000	IN	LFRAME# must be active (low) for the part to respond. Only the last start field (before LFRAME# transitioning high) should be recognized.
2	CYCTYPE + DIR	010X	IN	Indicates the type of cycle. Bits 3:2 must be “01b” for memory cycle. Bit 1 indicates the type of transfer “0” for Read. Bit 0 is reserved.
3-10	ADDRESS	YYYY	IN	Address Phase for Memory Cycle. LPC protocol supports a 32-bit address phase. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first. See Table 4 for address bits definition and Table 5 for valid memory address range.
11	TAR0	1111	IN then Float	In this clock cycle, the host has driven the bus to all 1s and then floats the bus. This is the first part of the bus “turnaround cycle.”
12	TAR1	1111(float)	Float then OUT	The A49LF040 takes control of the bus during this cycle.
13	SYNC	0000	OUT	The A49LF040 outputs the value 0000b indicating that data will be available during the next clock cycle.
14	DATA	ZZZZ	OUT	This field is the least-significant nibble of the data byte.
15	DATA	ZZZZ	OUT	This field is the most-significant nibble of the data byte.
16	TAR0	1111	IN then Float	In this clock, the host has driven the bus to all 1s and then floats the bus. This is the first part of the bus “turnaround cycle.”
17	TAR1	1111(float)	Float then OUT	The A49LF040 takes control of the bus during this cycle.

1. Field contents are valid on the rising edge of the present clock cycle.

LPC Single-Byte Read Waveforms

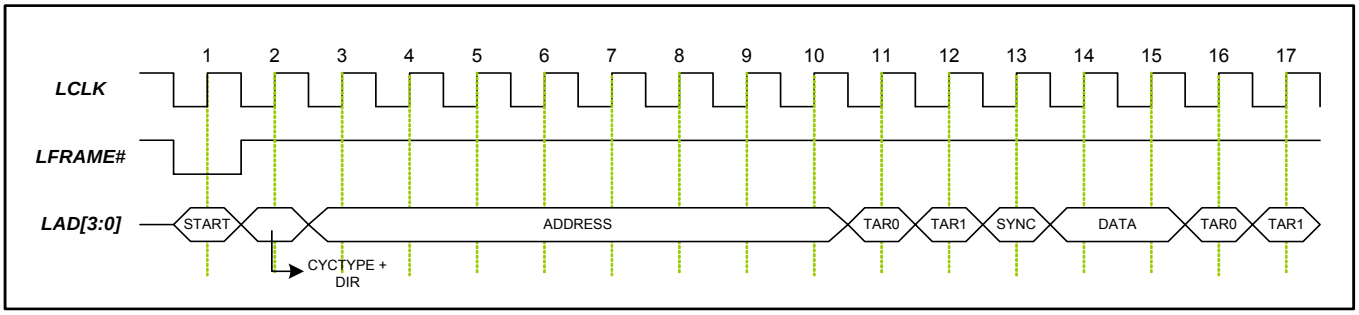
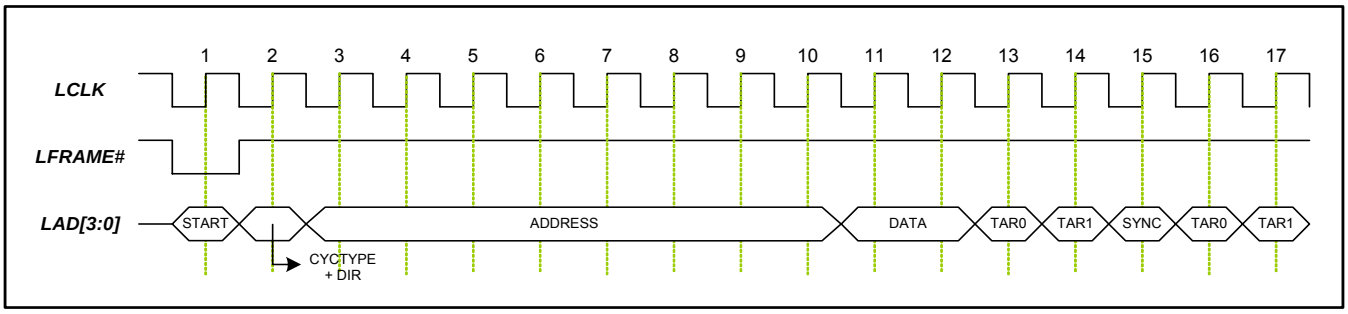


Table 3: LPC Write Cycle

Clock Cycle	Field Name	Field Contents LAD[3:0][1]	LAD[3:0] Direction	Comments
1	START	0000	IN	LFRAME# must be active (low) for the part to respond. Only the last start field (before LFRAME# transitioning high) should be recognized.
2	CYCTYPE + DIR	010X	IN	Indicates the type of cycle. Bits 3:2 must be “01b” for memory cycle. Bit 1 indicates the type of transfer “1” for Write. Bit 0 is reserved.
3-10	ADDRESS	YYYY	IN	Address Phase for Memory Cycle. LPC protocol supports a 32-bit address phase. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first. See Table 4 for address bits definition and Table 5 for valid memory address range.
11	DATA	ZZZZ	IN	This field is the least-significant nibble of the data byte.
12	DATA	ZZZZ	IN	This field is the most-significant nibble of the data byte.
13	TAR0	1111	IN then Float	In this clock cycle, the host has driven the bus to all ‘1’s and then floats the bus. This is the first part of the bus “turnaround cycle.”
14	TAR1	1111(float)	Float then OUT	The A49LF040 takes control of the bus during this cycle.
15	SYNC	0000	OUT	The A49LF040 outputs the values 0000, indicating that it has received data or a flash command.
16	TAR0	1111	OUT then Float	In this clock cycle, the A49LF040 has driven the bus to all ‘1’s and then floats the bus. This is the first part of the bus “turnaround cycle.”
17	TAR1	1111(float)	Float then IN	Host resumes control of the bus during this cycle.

1. Field contents are valid on the rising edge of the present clock cycle.

LPC Write Waveforms



ID mismatch: The A49LF040 will compare ID bits in the address field with the hardware ID strapping. If there is a mismatch, the device will ignore the cycle. Refer to Table 6 Multiple Device Selection Configuration for detail.

Device Memory Hardware Write Protection

The Top Boot Lock (TBL#) and Write Protect (WP#) pins are provided for hardware write protection of device memory in the A49LF040. The TBL# pin is used to write protect the top boot block (64 Kbytes) at the highest flash memory address range for the A49LF040. WP# pin write protects the remaining blocks in the flash memory. An active low signal at the TBL# pin prevents Program and Erase operations of the top boot block. The WP# pin serves the same function for the remaining blocks of the device memory. The TBL# and WP# pins write protection functions operate independently of one another. Both TBL# and WP# pins must be set to their required protection states prior to starting a Program or Erase operation. A logic level change occurring at the TBL# or WP# pin during a Program or Erase operation could cause unpredictable results. TBL# and WP# pins cannot be left unconnected. Clearing the Write-Lock bit in any register when WP# is low will have no functional effect, even though the register may indicate that the block is no longer locked.

Reset

A V_{IL} on INIT# or RST# pin initiates a device reset. INIT# and RST# pins have the same function internally. It is required to drive INIT# or RST# pins low during a system reset to ensure proper CPU initialization. During a Read operation, driving INIT# or RST# pins low deselects the device and places the output drivers, LAD[3:0], in a high-impedance state. The reset signal must be held low for a minimal duration of time T_{RSTP}. A reset latency will occur if a reset procedure is performed during a Program or Erase operation. See Table 19, Reset Timing Parameters for more information. A device reset during an active Program or Erase will abort the operation and memory contents may become invalid due to data being altered or corrupted from an incomplete Erase or Program operation. In this case, the device can take up to T_{RSTE} to abort a Program or Erase operation.

Write Operation Status Detection

The A49LF040 device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (I/O_7) and Toggle Bit (I/O_6). The End-of-Write detection mode is incorporated into the LPC Read cycle. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either I/O_7 or I/O_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (I/O_7)

When the A49LF040 device is in the internal Program operation, any attempt to read I/O_7 will produce the complement of the true data. Once the Program operation is completed, I/O_7 will produce true data. Note that even though I/O_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read I/O_7 will produce a '0'. Once the internal Erase operation is completed, I/O_7 will produce a '1'. Proper status will not be given using Data# Polling if the address is in the invalid range.

Toggle Bit (I/O_6)

During the internal Program or Erase operation, any consecutive attempts to read I/O_6 will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop.

Multiple Device Selection

The four ID pins, ID[3:0], allow multiple devices to be attached to the same bus by using different ID strapping in a system. When the A49LF040 is used as a boot device, ID[3:0] must be strapped as 0000, all subsequent devices should use a sequential up-count strapping (i.e. 0001, 0010, 0011, etc.). The ID bits in the address field are inverse of the hardware strapping. The address bits [A23, A21:A19] for A49LF004 are used to select the device with proper IDs. See Table 6 for IDs. The A49LF040 will compare the strapping values, if there is a mismatch, the device will ignore the remainder of the cycle and go into standby mode. Since there is no ID support in A/A Mux mode, to program multiple devices a stand-alone PROM programmer is recommended.

REGISTERS

There are two types of registers available on the A49LF040, the General Purpose Inputs Register, and the JEDEC ID Registers. These registers appear at their respective address location in the 4 GByte system memory map. Unused register locations will read as 00H. Any attempt to read or write any register during an internal Write operation will be ignored. Refer to Table 7 for the LPC register memory map.

General Purpose Inputs Register

The GPI_REG (General Purpose Inputs Register) passes the state of GPI[4:0] pins at power-up on the A49LF040. It is recommended that the GPI[4:0] pins be in the desired state before LFRAME# is brought low for the beginning of the next bus cycle, and remain in that state until the end of the cycle. There is no default value since this is a pass-through register. See Table 8 for the GPI_REG bits and function, and Table 9 for memory address locations for its respective device strapping.

Table 4: Address Bit Definition

A_{31}:A_{23}	A_{23}	A_{22}	A_{21}:A_{19}	A_{18}:A_0
1111 1111b	ID[3]	1 = Memory access 0 = Register access	ID[2:0]	Device memory address

Table 5: Address Decoding Range

ID Strapping	Device Access	A_{21}:A_{19}	Memory Size
Device #0 – 7	Memory Access	FFFF FFFFH: FFC0 0000H	4 MByte
	Register Access	FFBF FFFFH: FF80 0000H	4 MByte
Device #8 - 15	Memory Access	FF7F FFFFH: FF40 0000H	4 MByte
	Register Access	FF3F FFFFH: FF00 0000H	4 MByte

Table 6: Multiple Device Selection Configuration

Device#	Hardware Strapping ID[3:0]	Address Bits Decoding			
		A23	A21	A20	A19
0 (Boot device)	0000	1	1	1	1
1	0001	1	1	1	0
2	0010	1	1	0	1
3	0011	1	1	0	0
4	0100	1	0	1	1
5	0101	1	0	1	0
6	0110	1	0	0	1
7	0111	1	0	0	0
8	1000	0	1	1	1
9	1001	0	1	1	0
10	1010	0	1	0	1
11	1011	0	1	0	0
12	1100	0	0	1	1
13	1101	0	0	1	0
14	1110	0	0	0	1
15	1111	0	0	0	0

Table 7: LPC Register Memory Map

Memory Address	Mnemonic	Register Name	Default	Type
FFBC0100h	GPI_REG	LPC General Purpose Input Register	N/A	R
FFBC0000h	MANUF_REG	Manufacturer ID Register	37h	R
FFBC0001h	DEV_REG	Device ID Register	9Dh	R
FFBC0003h	CONT_REG	Continuation ID Register	7Fh	R

JEDEC ID Registers

The JEDEC ID registers identify the device as A49LF040 and manufacturer as SST in LPC mode. See Table 9 for memory address locations for its respective JEDEC ID location.

Table 8: General Purpose Inputs Register

Bit	Bit	Function	Pin Number	
			32-PLCC	32-TSOP
7:5	-	Reserved	-	-
4	GPI[4]	GPI_REG Bit 4	30	6
3	GPI[3]	GPI_REG Bit 3	3	11
2	GPI[2]	GPI_REG Bit 2	4	12
1	GPI[1]	GPI_REG Bit 1	5	13
0	GPI[0]	GPI_REG Bit 0	6	14

Table 9 Memory Map Register Addresses for A49LF040

Device#	Hardware Strapping ID[3:0]	GPI_REG	JEDEC ID		
			Manufacturer	Continuation	Device
0 (Boot device)	0000	FFBC 0100H	FFBC 0000H	FFBC 0003H	FFBC 0001H
1	0001	FFB4 0100H	FFB4 0000H	FFB4 0003H	FFB4 0001H
2	0010	FFAC 0100H	FFAC 0000H	FFAC 0003H	FFAC 0001H
3	0011	FFA4 0100H	FFA4 0000H	FFA4 0003H	FFA4 0001H
4	0100	FF9C 0100H	FF9C 0000H	FF9C 0003H	FF9C 0001H
5	0101	FF94 0100H	FF94 0000H	FF94 0003H	FF94 0001H
6	0110	FF8C 0100H	FF8C 0000H	FF8C 0003H	FF8C 0001H
7	0111	FF84 0100H	FF84 0000H	FF84 0003H	FF84 0001H
8	1000	FF3C 0100H	FF3C 0000H	FF3C 0003H	FF3C 0001H
9	1001	FF34 0100H	FF34 0000H	FF34 0003H	FF34 0001H
10	1010	FF2C 0100H	FF2C 0000H	FF2C 0003H	FF2C 0001H
11	1011	FF24 0100H	FF24 0000H	FF24 0003H	FF24 0001H
12	1100	FF1C 0100H	FF1C 0000H	FF1C 0003H	FF1C 0001H
13	1101	FF14 0100H	FF14 0000H	FF14 0003H	FF14 0001H
14	1110	FF0C 0100H	FF0C 0000H	FF0C 0003H	FF0C 0001H
15	1111	FF04 0100H	FF04 0000H	FF04 0003H	FF04 0001H

ADDRESS/ADDRESS MULTIPLEXED (A/A MUX) MODE

Device Operation
Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of WE#. During the software command sequence the row address is latched on the falling edge of R/C# and the column address is latched on the rising edge of R/C#. Refer to Table 8 and Table 9 for operation modes and the command sequence.

Read
The Read operation of the A49LF040 device is controlled by OE#. OE# is the output control and is used to gate data from the output pins. Refer to the Read cycle timing diagram, Figure 10 for further details.

Reset
A V_{IL} on RST# pin initiates a device reset.

Byte-Program Operation
The A49LF040 device is programmed on a byte-by-byte basis. Before programming, one must ensure that the block, in which the byte which is being programmed exists, is fully erased. The Byte-Program operation is initiated by executing a four-byte command load sequence for Software Data Protection with address and data in the last byte sequence. During the Byte-Program operation, the row address (A10-A0) is latched on the falling edge of R/C# and the column Address (A18-A11) is latched on the rising edge of R/C#. The data bus is latched in the rising edge of WE#. See Figure 11 for Program operation timing diagram, Figure 14 for timing waveforms, and Figure 19 for its flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Table 10: A/A Mux Mode Operation Selection

Mode	RST#	OE#	WE#	Address	I/O
Read	V_{IH}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}
Write	V_{IH}	V_{IH}	V_{IL}	A_{IN}	D_{IN}
Standby	V_{IH}	V_{IH}	V_{IH}	X	High Z
Output Disable	V_{IH}	V_{IH}	X	X	High Z
Reset	V_{IL}	X	X	X	High Z
Product Identification	V_{IH}	V_{IL}	V_{IH}	A18 – A2 = X, A1 = V_{IL}, A0 = V_{IL}	Manufacturer ID
				A18 – A2 = X, A1 = V_{IL}, A0 = V_{IH}	Device ID
				A18 – A2 = X, A1 = V_{IH}, A0 = V_{IH}	Continuation ID

Block-Erase Operation
The Block-Erase Operation allows the system to erase the device in 64 KByte uniform block size for the A49LF040. The Block-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Block-Erase command (30H or 50H) and block address. The internal Block-Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 15 for timing waveforms. Any commands written during the Block-Erase operation will be ignored.

Chip-Erase
The A49LF040 device provides a Chip-Erase operation only in A/A Mux mode, which allows the user to erase the entire memory array to the '1's state. This is useful when the entire device must be quickly erased. The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE#.

During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 11 for the command sequence, Figure 16 for timing diagram, and Figure 21 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

Write Operation Status Detection
The A49LF040 device provides two software means to detect the completion of a Write cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (I/O_7) and Toggle Bit (I/O_6). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Write operation. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either I/O_7 or I/O_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (I/O_7)
When the A49LF040 device is in the internal Program operation, any attempt to read I/O_7 will produce the complement of the true data. Once the Program operation is completed, I/O_7 will produce true data. Note that even though I/O_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt

to read I/O_7 will produce a '0'. Once the internal Erase operation is completed, I/O_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# pulse for Program operation. For Block- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# pulse. See Figure 12 for Data# Polling timing diagram. Proper status will not be given using Data# Polling if the address is in the invalid range.

Toggle Bit (I/O_6)

During the internal Program or Erase operation, any consecutive attempts to read I/O_6 will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# pulse for Program operation. For Block- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# pulse. See Figure 13 for Toggle Bit timing diagram.

Data Protection

The A49LF040 device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The A49LF040 provides the JEDEC approved Software Data Protection scheme for all data alteration operation, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequences. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of a six-byte load sequence. The A49LF040 device is shipped with the Software Data Protection permanently enabled. See Table 11 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode, within T_{RC}.

Electrical Specifications

The AC and DC specifications for the LPC Interface signals (LAD[3:0], LCLK, LFRAME#, and RST#) as defined in Section 4.2.2 of the *PCI Local Bus Specification, Rev. 2.1*. Refer to Table 12 for the DC voltage and current specifications. Refer to the specifications on Table 13 to Table 22 for Clock, Read/Write, and Reset operations.

Product Identification

The product identification mode identifies the Manufacturer ID, Continuation ID, and Device ID of the A49LF040. See Table 9 for detail information.

Figure 3: System Memory Map and Device Memory Map for A49LF040

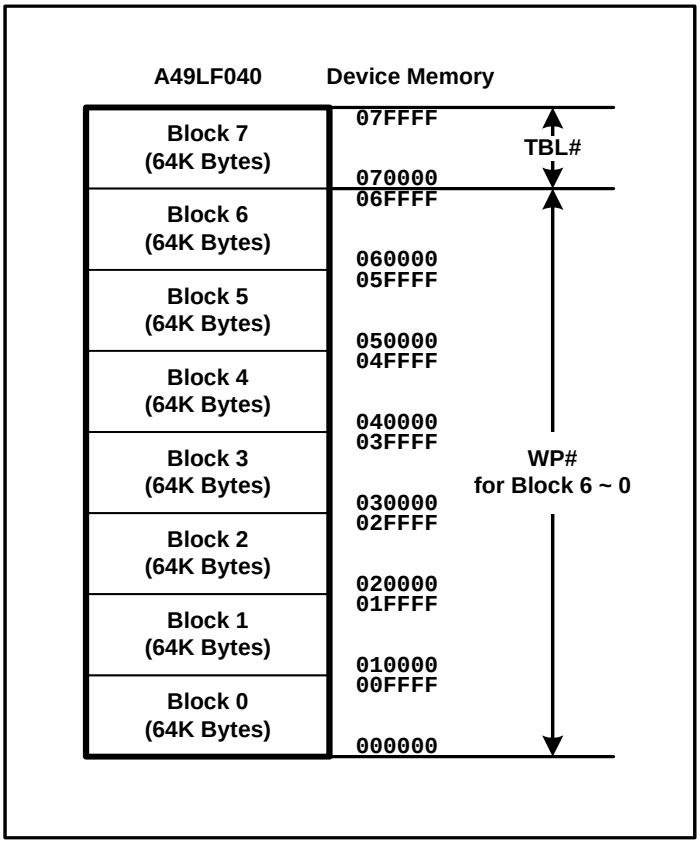


Table 11: Software Data Protection Command Definition

Command	Bus Cycles	1st Cycle(1)		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr(2)	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Block Erase	6	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	80H	YYYY 5555H	AAH	YYYY 2AAAH	55H	BA(4)	30H/50H(5)
Chip Erase(3)	6	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	80H	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	10H
Byte Program	4	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	A0H	PA(6)	PD(6)				
Product ID Entry	3	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	90H						
Product ID Exit(7)	1	XXXX XXXXH	F0H										
Product ID Exit(7)	3	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	F0H						

Notes:
1. LPC Mode uses consecutive Write cycles to complete a command sequence; A/A Mux Mode uses consecutive bus cycles to complete a command sequence.
2. YYYY = A[31:16]. In LPC mode, during SDP command sequence, YYYY must be within memory address range specified in Table 5. In A/A Mux mode, YYYY can be V_{IL} or V_{IH}, but no other value.
3. Chip erase is available in A/A Mux Mode only.
4. BA: Block Erase Address.
5. Either 30H or 50H are acceptable for Block Erase.
6. PA: Program Byte Address; PD: Byte data to be programmed.
7. Both Product ID Exit commands are equivalent.

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +85°C	3.0-3.6V

AC Conditions of Test

Input Rise/Fall Time 3ns
Output Load . . . . . CL = 30pF

Table 12: DC Operating Characteristics (All Interfaces)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Active V_{DD} Current: Read		12	mA	Address Input=V_{IL}/V_{IH}, at F=1/T_{RC}Min, V_{DD}=V_{DD}Max(A/A Mux Mode) OE#=V_{IH}, WE#=V_{IH}
	Active V_{DD} Current: Write(1)		24	mA	
I_{SB}	Standby V_{DD} Current (LPC Mode)		100	µA	LFRAME#=0.9V_{DD},f=33MHz,V_{DD}=V_{DD}Max, All other inputs ≥ 0.9V_{DD} or ≤ 0.1V_{DD}
I_{RY}(2)	Ready Mode V_{DD} Current (LPC Mode)		10	mA	LFRAME#=V_{IL},f=33MHz,V_{DD}=V_{DD}Max, All other inputs ≥ 0.9V_{DD} or ≤ 0.1V_{DD}
I_I	Input Current for Mode and ID[3:0] Pins		100	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD}Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD}Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD}Max
V_{IHI}(3)	INIT# Input High Voltage	1.0	V_{DD}+0.5	V	V_{DD}=V_{DD}Max
V_{ILI}(3)	INIT# Input Low Voltage	-0.5	0.4	V	V_{DD}=V_{DD}Min
V_{IH}	Input High Voltage	0.5V_{DD}	V_{DD}+0.5	V	V_{DD}=V_{DD}Max
V_{IL}	Input Low Voltage	-0.5	0.3V_{DD}	V	V_{DD}=V_{DD}Min
V_{OL}	Output Low Voltage		0.1V_{DD}	V	IOL=1500µA, V_{DD}=V_{DD}Min
V_{OH}	Output High Voltage	0.9V_{DD}		V	IOH=-500µA, V_{DD}=V_{DD}Min

Notes:
1. I_{DD} active while Erase or Program is in progress.
2. The device is in Ready Mode when no activity is on the LPC bus.
3. Do not violate processor or chipset specification regarding INIT# voltage.

Table 13: Recommended System Power-Up Timings

Symbol	Parameter	Min	Units
$T_{PU-READ}$(1)	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$(1)	Power-up to Write Operation	100	µs

Notes:
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 14: Pin Impedance (V_{DD}=3.3V, Ta=25°C, f=1MHz, other pins open)

Parameter	Description	Test Condition	Max
$C_{I/O}$ (1)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12pF
C_{IN} (1)	Input Capacitance	V_{IN} = 0V	12pF
L_{PIN} (2)	Pin Inductance		20nH

Notes:
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Refer to PCI specifications.

Table 15: Clock Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{CYC}	LCLK Cycle Time	30		ns
T_{HIGH}	LCLK High Time	11		ns
T_{LOW}	LCLK Low Time	11		ns
	LCLK Slew Rate (peak-to-peak)	1	4	V/ns

Figure 4: LCLK Waveform

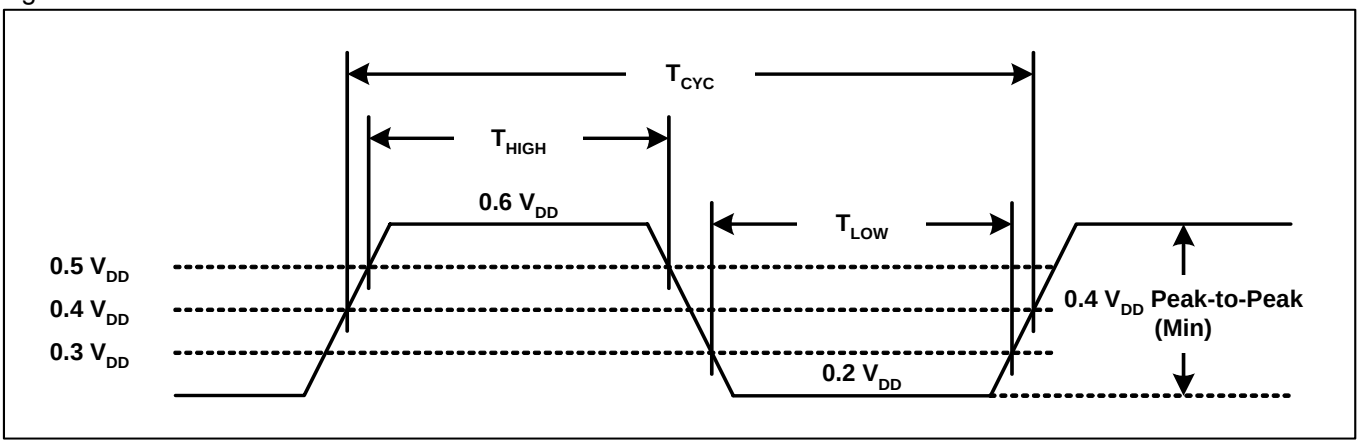


Table 16: LPC Mode Read/Write Cycle Timing Parameters, V_{DD}=3.0-3.6V

Symbol	Parameter	Min	Max	Units
T_{SU}	Input Set Up Time to LCLK Rising	7		ns
T_{DH}	LCLK Rising to Data Hold Time	0		ns
T_{VAL}	LCLK Rising to Data Valid	2	11	ns
T_{ON}	LCLK Rising to Active (Float to Active Delay)	2		ns
T_{OFF}	LCLK Rising to Inactive (Active to Float Delay)		28	ns

Table 17: LPC Mode Interface Measurement Condition Parameters

Symbol	Value	Units
V_{TH}	0.6 V_{DD}	V
V_{TL}	0.2 V_{DD}	V
V_{TEST}	0.4 V_{DD}	V
V_{MAX}	0.4 V_{DD}	V
Input Signal Edge Rate	1V/ns	

Figure 5: Input Timing Parameters

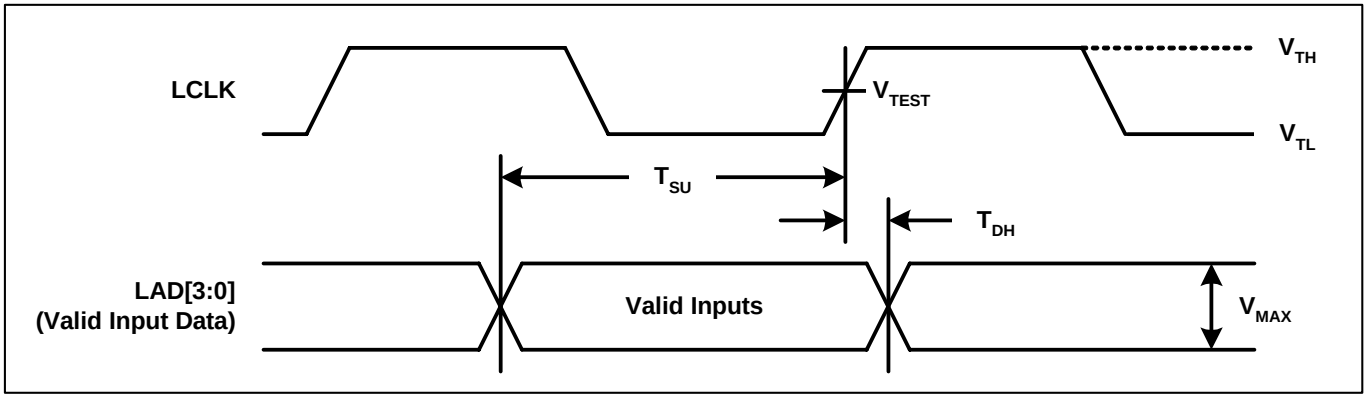


Figure 6: Output Timing Parameters

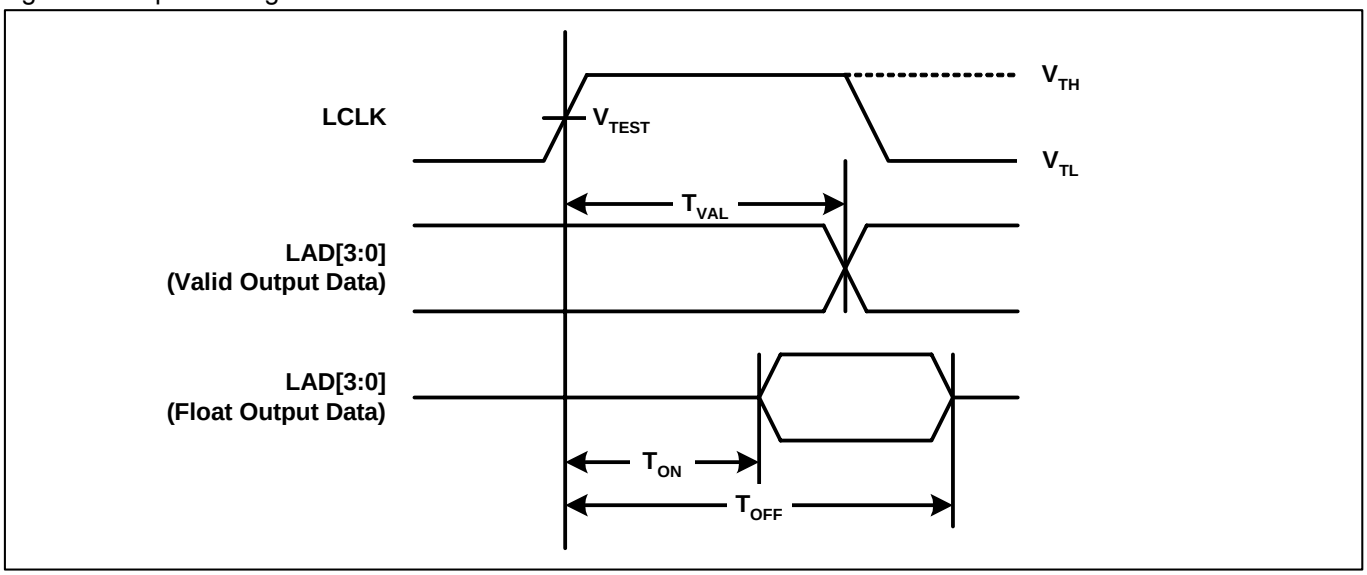


Table 18: LPC Mode Interface AC Input/Output Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{OH} (AC)	Switching Current High	$0 < V_{OUT} \le 0.3V_{DD}$	$-12\ V_{DD}$		mA
		$0.3V_{DD} < V_{OUT} \le 0.9V_{DD}$	$-17.1(V_{DD}-V_{OUT})$		mA
		$0.7V_{DD} < V_{OUT} \le V_{DD}$		Equation C	mA
	(Test Point)	$V_{OUT} = 0.7V_{DD}$		$-32\ V_{DD}$	mA
I_{OL} (AC)	Switching Current Low	$V_{DD} > V_{OUT} \ge 0.6V_{DD}$	$16V_{DD}$		mA
		$0.6V_{DD} > V_{OUT} > 0.1V_{DD}$	$26.7V_{OUT}$		mA
		$0.18V_{DD} > V_{OUT} > 0$		Equation D	mA
	(Test Point)	$V_{OUT}=0.18V_{DD}$		$38V_{DD}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25+(V_{IN}+1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{DD}+4 > V_{IN} > V_{DD}+1$	$25+(V_{IN}-V_{DD}-1)/0.015$		mA
slewr	Output Rise Slew Rate	$0.2V_{DD}$-$0.6V_{DD}$ load	1	4	V/ns
slewf	Output Fall Slew Rate	$0.6V_{DD}$-$0.2V_{DD}$ load	1	4	V/ns

Notes:
1. See PCI specification.
2. PCI specification output load is used.

Table 19: LPC Mode Interface Reset Timing Parameters, V_{DD}=3.0-3.6V

Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} Stable to Reset Low	1		ms
T_{KRST}	Clock Stable to Reset Low	100		µs
T_{RSTP}	RST# Pulse Width	100		ns
T_{RSTF}	RST# Low to Output Float		48	ns
T_{RST}(1)	RST# High to LFRAME# Low	1		µs
T_{RSTE}	RST# Low to Reset During Erase or Program		10	µs
	RST# or INIT# Slew Rate	50		mV/ns

Notes:
1. There will be a latency of T_{RSTE} if a reset procedure is performed during a Program or Erase operation.

Figure 7: Reset Timing Diagram

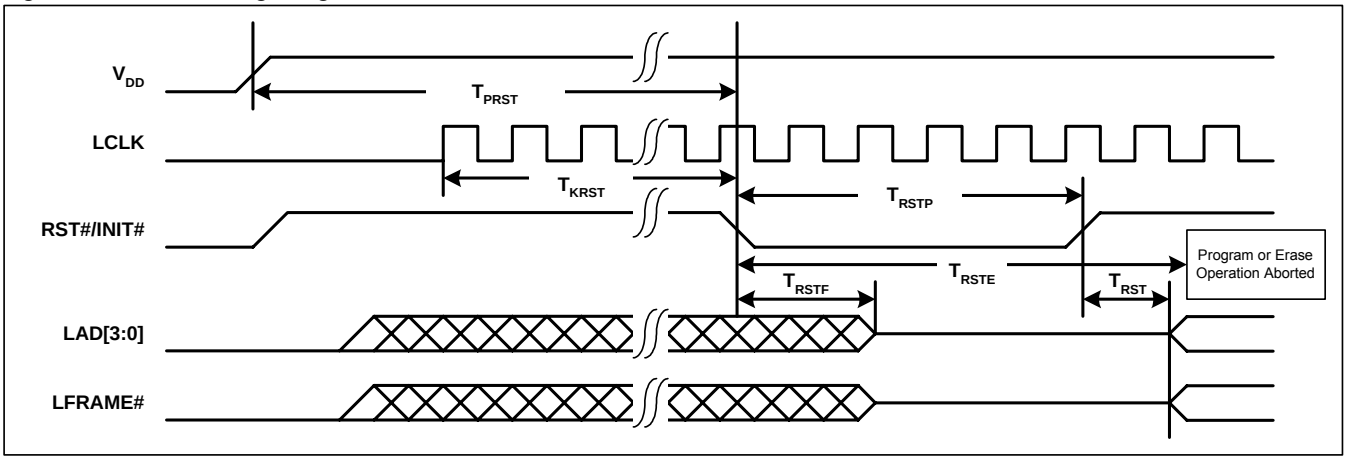
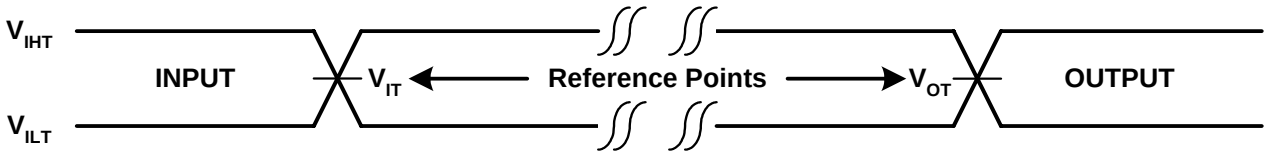


Figure 8: A/A Mux Mode AC Input/Output Reference Waveforms

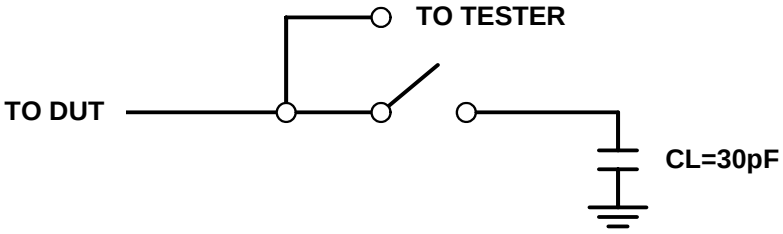


AC test inputs are driven at V_{IHT} ($0.9V_{DD}$) for a logic HIGH and V_{ILT} ($0.1V_{DD}$) for a logic LOW. Measurement reference points for inputs and outputs are V_{IT} ($0.5V_{DD}$) and V_{OT} ($0.5V_{DD}$). Input rise and fall times (10% <-> 90%) are < 5ns

Note:

V_{IT}: V_{INPUT} Test
V_{OT}: V_{OUTPUT} Test
V_{IHT}: V_{INPUT} HIGH Test
V_{ILT}: V_{INPUT} LOW Test

Figure 9: A/A Mux Mode Test Load Condition



A/A MUX MODE AC CHARACTERISTICS

Table 20: Read Cycle Timing Parameters V_{DD}=3.0-3.6V

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	270		ns
T_{RST}	RST# High to Row Address Setup	1		µs
T_{AS}	R/C# Address Set-up Time	45		ns
T_{AH}	R/C# Address Hold Time	45		ns
T_{AA}	Address Access Time		120	ns
T_{OE}	Output Enable Access Time		60	ns
T_{OLZ}	OE# Low to Active Output	0		ns
T_{OHZ}	OE# High to High-Z Output		35	ns
T_{OH}	Output Hold from Address Change	0		ns

Table 21: Program/Erase Cycle Timing Parameters, V_{DD}=3.0-3.6V

Symbol	Parameter	Min	Max	Units
T_{RST}	RST# High to Row Address Setup	1		µs
T_{AS}	R/C# Address Setup Time	50		ns
T_{AH}	R/C# Address Hold Time	50		ns
T_{CWH}	R/C# to Write Enable High Time	50		ns
T_{OES}	OE# High Setup Time	20		ns
T_{OEH}	OE# High Hold Time	20		ns
T_{OEP}	OE# to Data# Polling Delay		40	ns
T_{OET}	OE# to Toggle Bit Delay		40	ns
T_{WP}	WE# Pulse Width	100		ns
T_{WPH}	WE# Pulse Width High	100		ns
T_{DS}	Data Setup Time	50		ns
T_{DH}	Data Hold Time	5		ns
T_{IDA}	Product ID Access and Exit Time		150	ns
T_{BP}	Byte Programming Time		300	µs
T_{BE}	Block Erase Time		8	s
T_{SCE}	Chip Erase Time		10	s

Table 22: Reset Timing Parameters, V_{DD}=3.0-3.6V

Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} Stable to Reset Low	1		ms
T_{RSTP}	RST# Pulse Width	100		ns
T_{RSTF}	RST# Low to Output Float		48	ns
T_{RST}(1)	RST# High to LFRAME# Low	1		µs
T_{RSTE}	RST# Low to Reset During Erase or Program		10	µs

1. There will be a reset latency of TRSTE if a reset procedure is performed during a Program or Erase operation.

Figure 10: A/A Mux Mode Read Cycle Timing Diagram

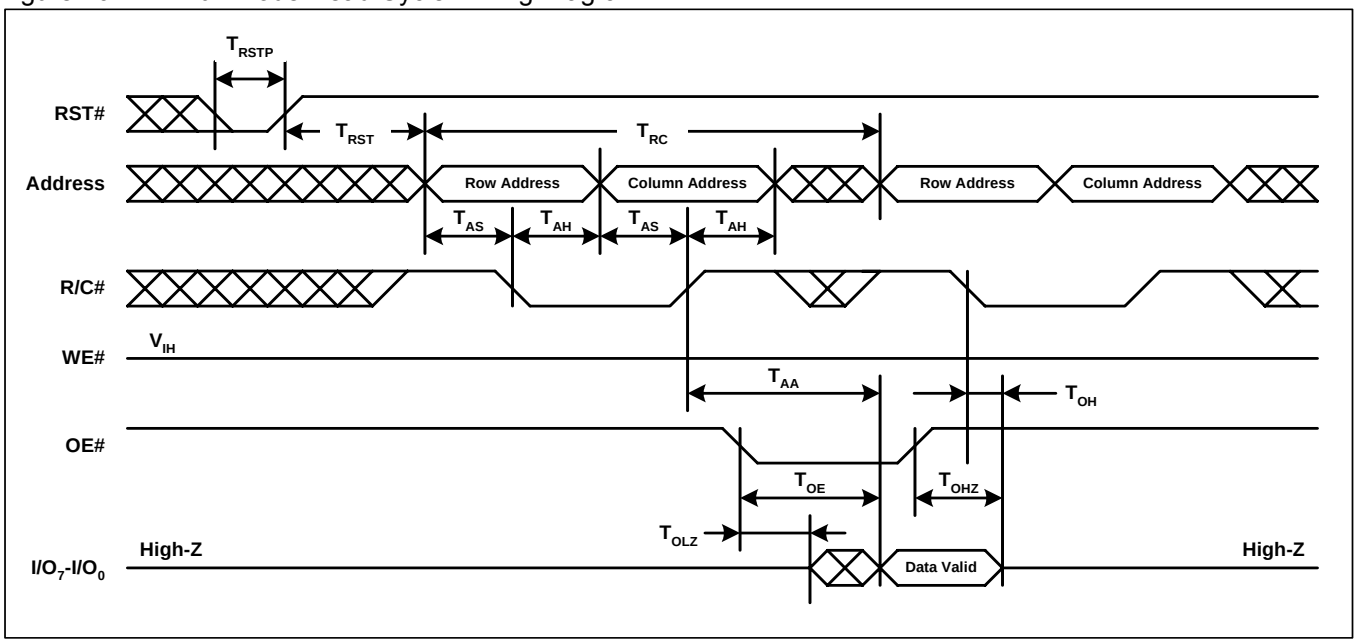


Figure 11: A/A Mux Mode Write Cycle Timing Diagram

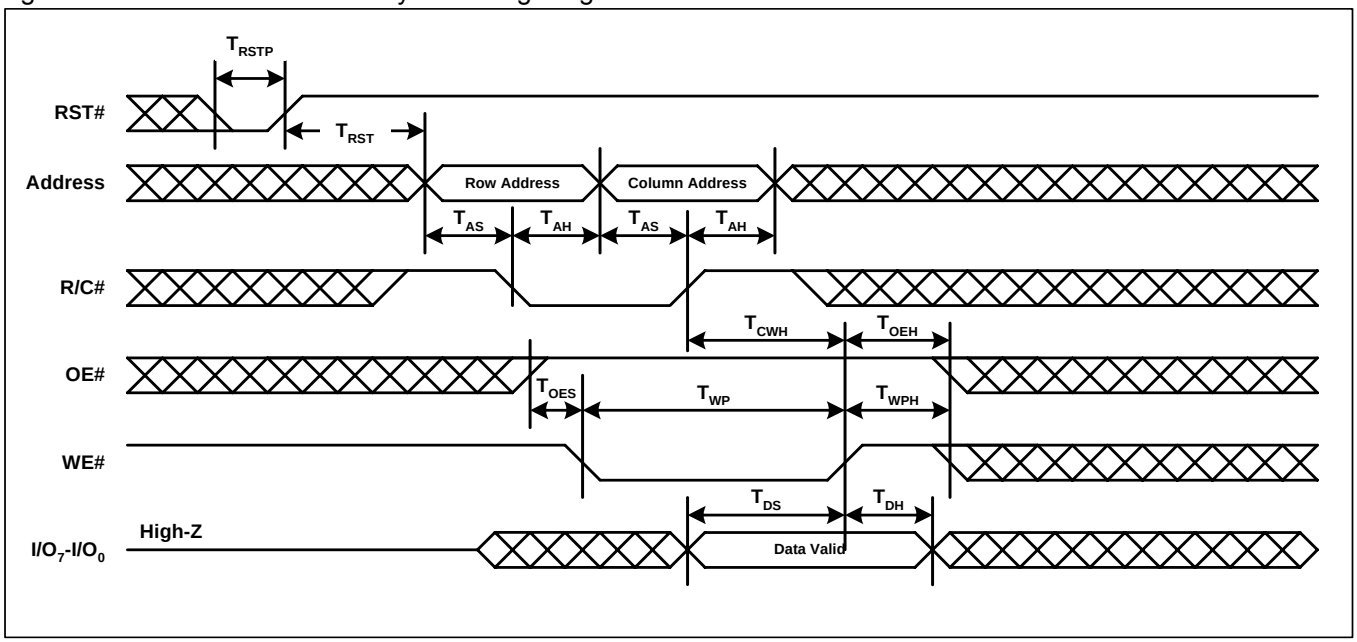


Figure 12: A/A Mux Mode Data# Polling Timing Diagram

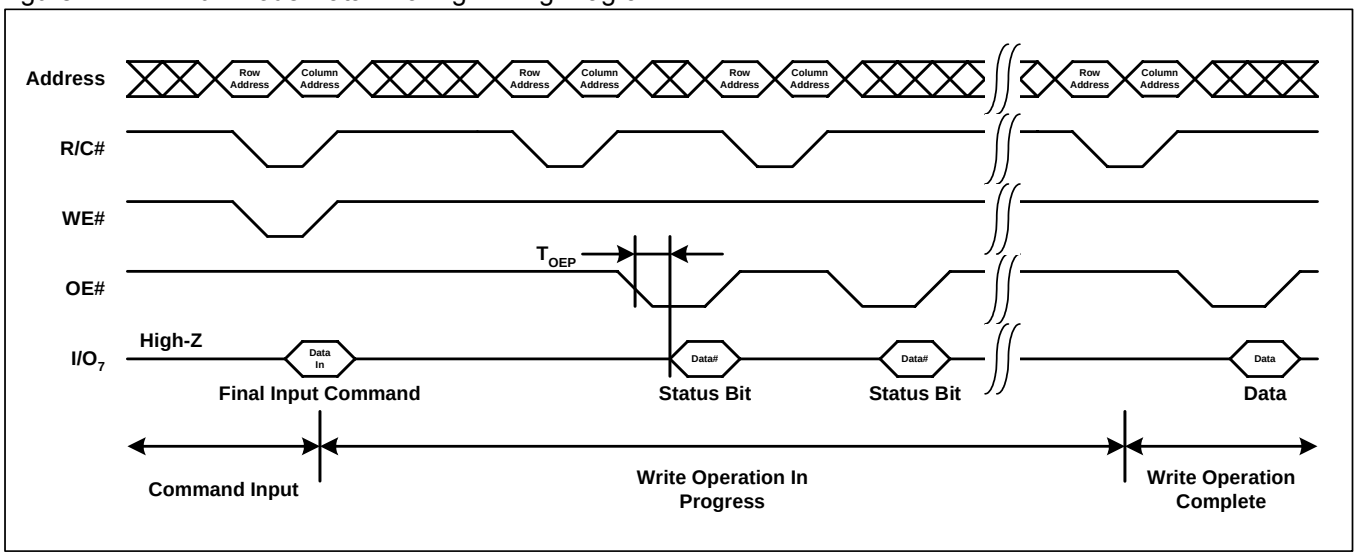


Figure 13: A/A Mux Mode Toggle Bit Timing Diagram

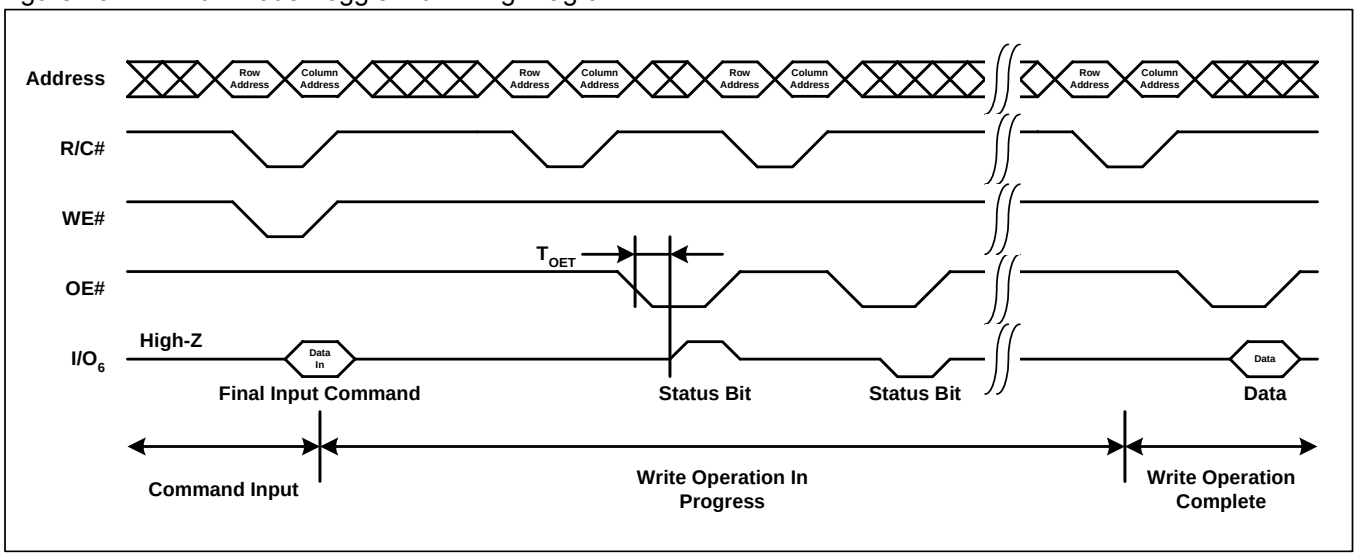


Figure 14: A/A Mux Mode Byte Program Timing Diagram

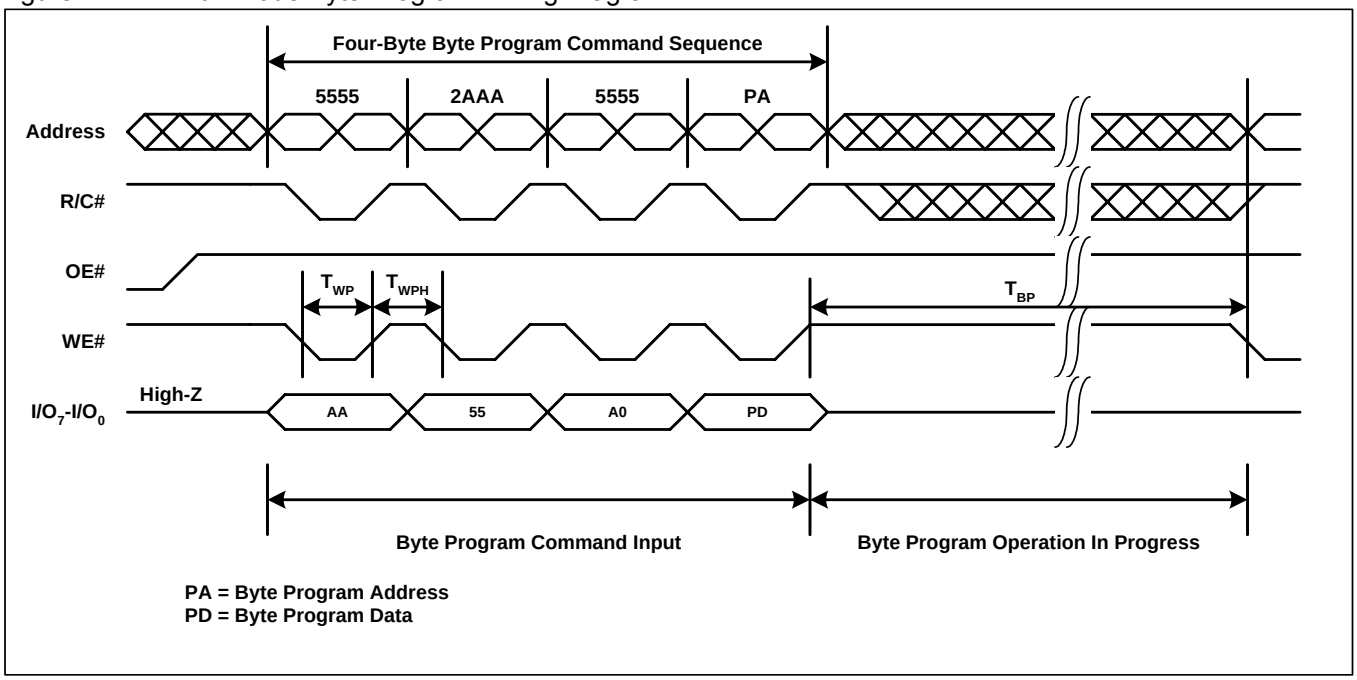


Figure 15: A/A Mux Mode Block Erase Timing Diagram

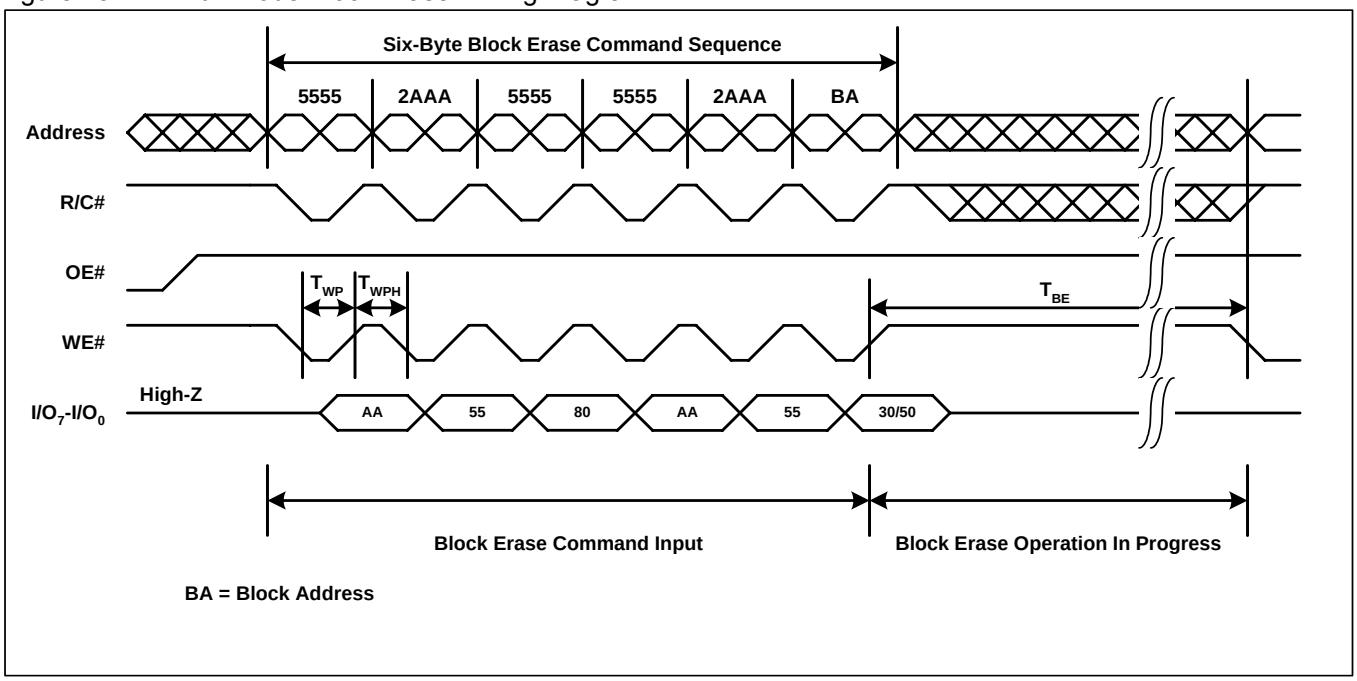


Figure 16: A/A Mux Mode Chip Erase Timing Diagram

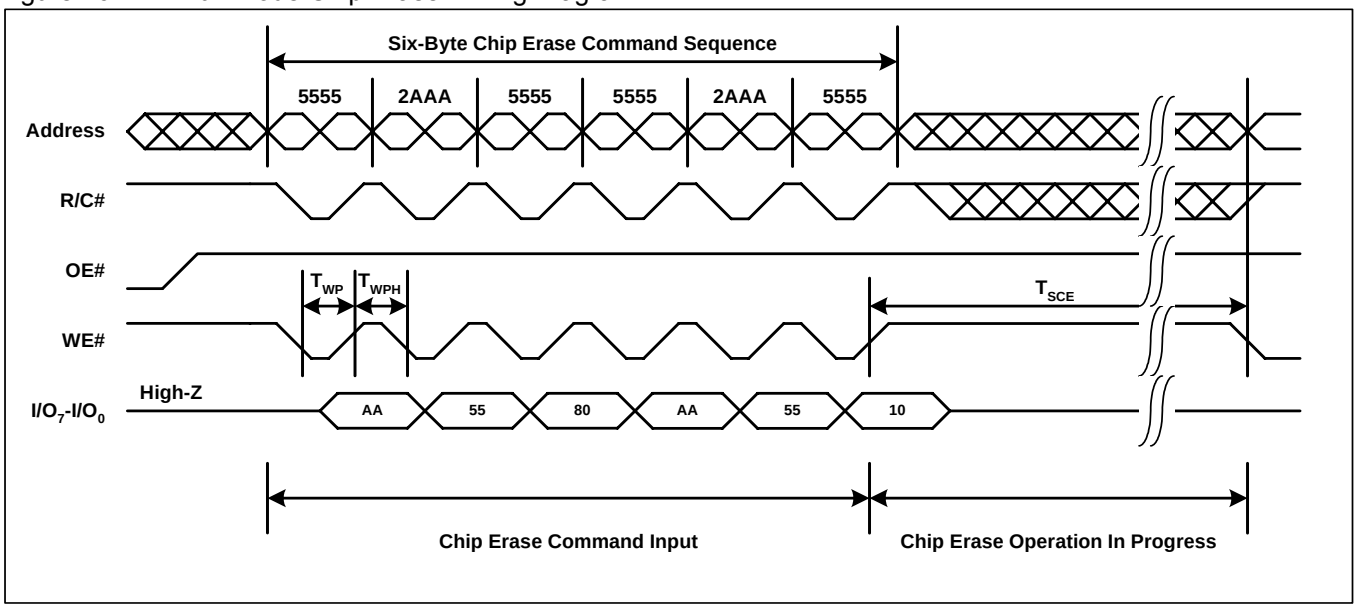


Figure 17: A/A Mux Mode Product ID Entry and Read Timing Diagram

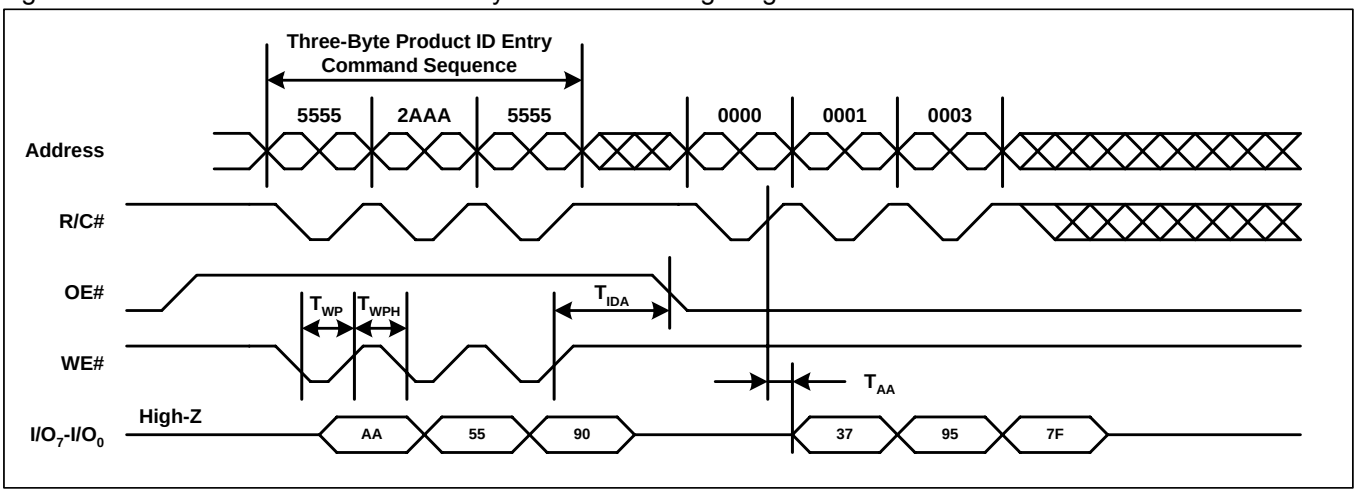


Figure 18: A/A Mux Mode Product ID Exit and Reset Timing Diagram

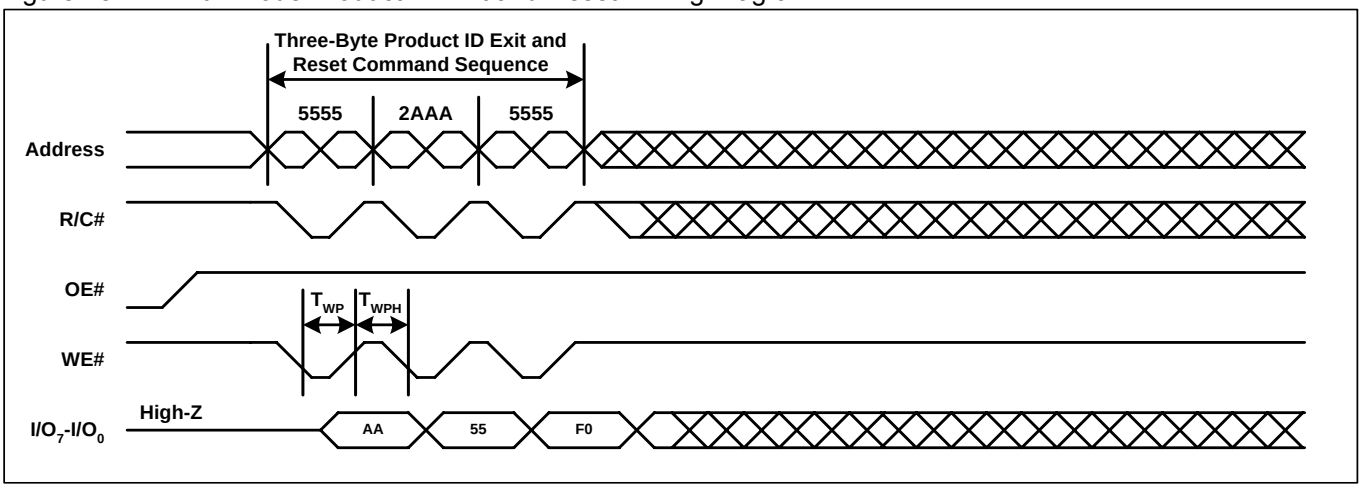


Figure 19: Automatic Byte Program Algorithm

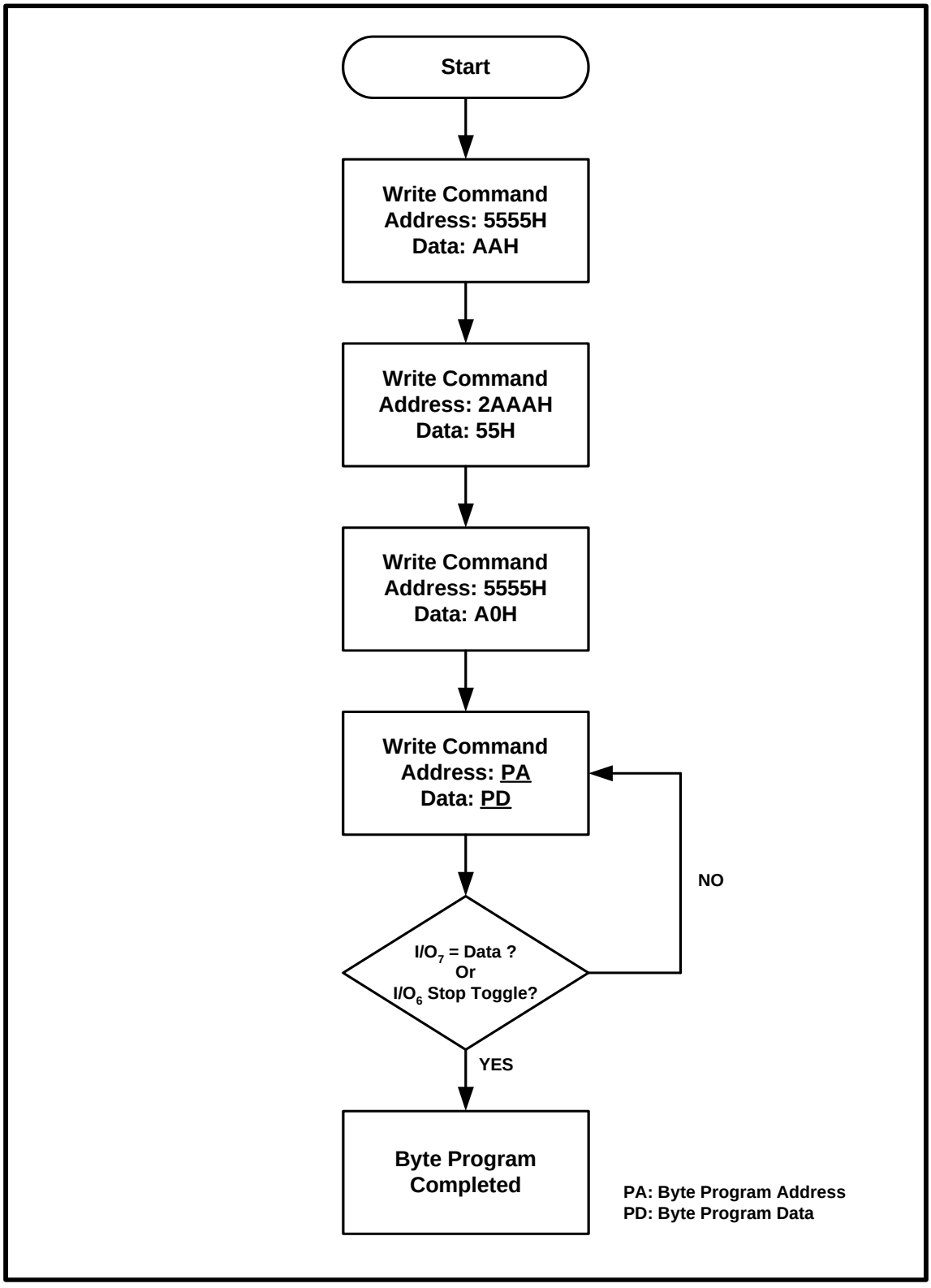


Figure 20: Automatic Block Erase Algorithm

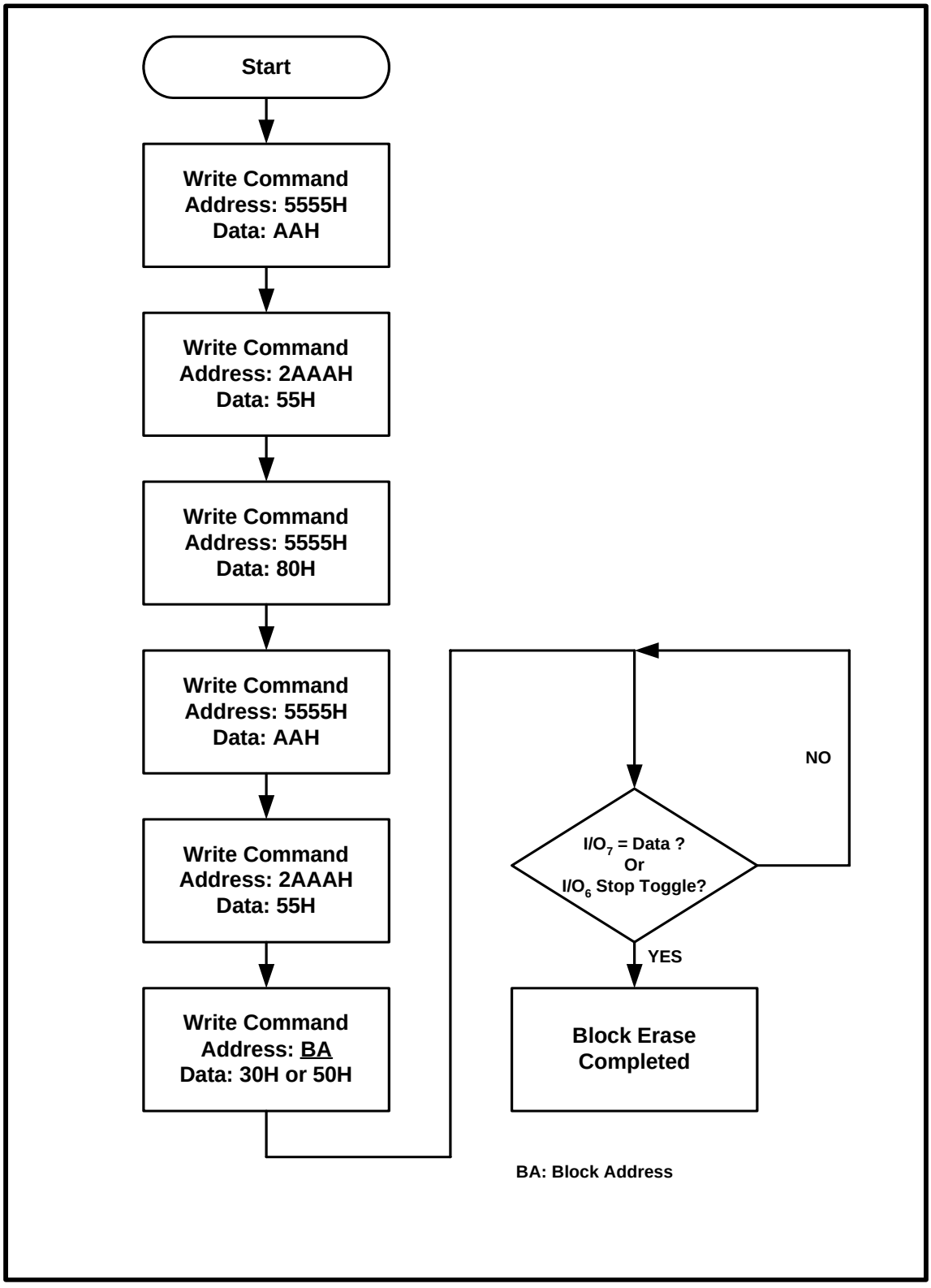


Figure 21: Automatic Chip Erase Algorithm

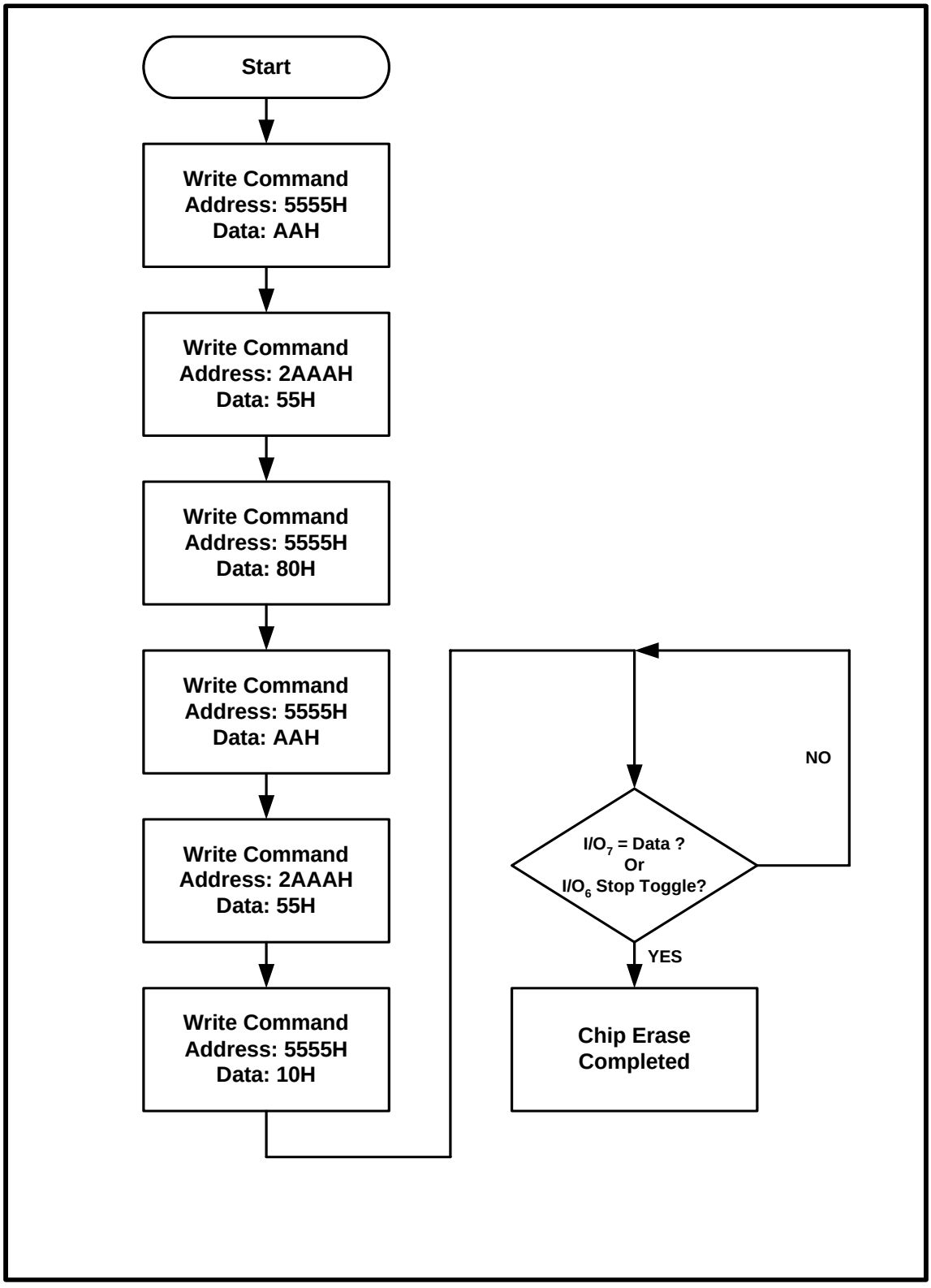
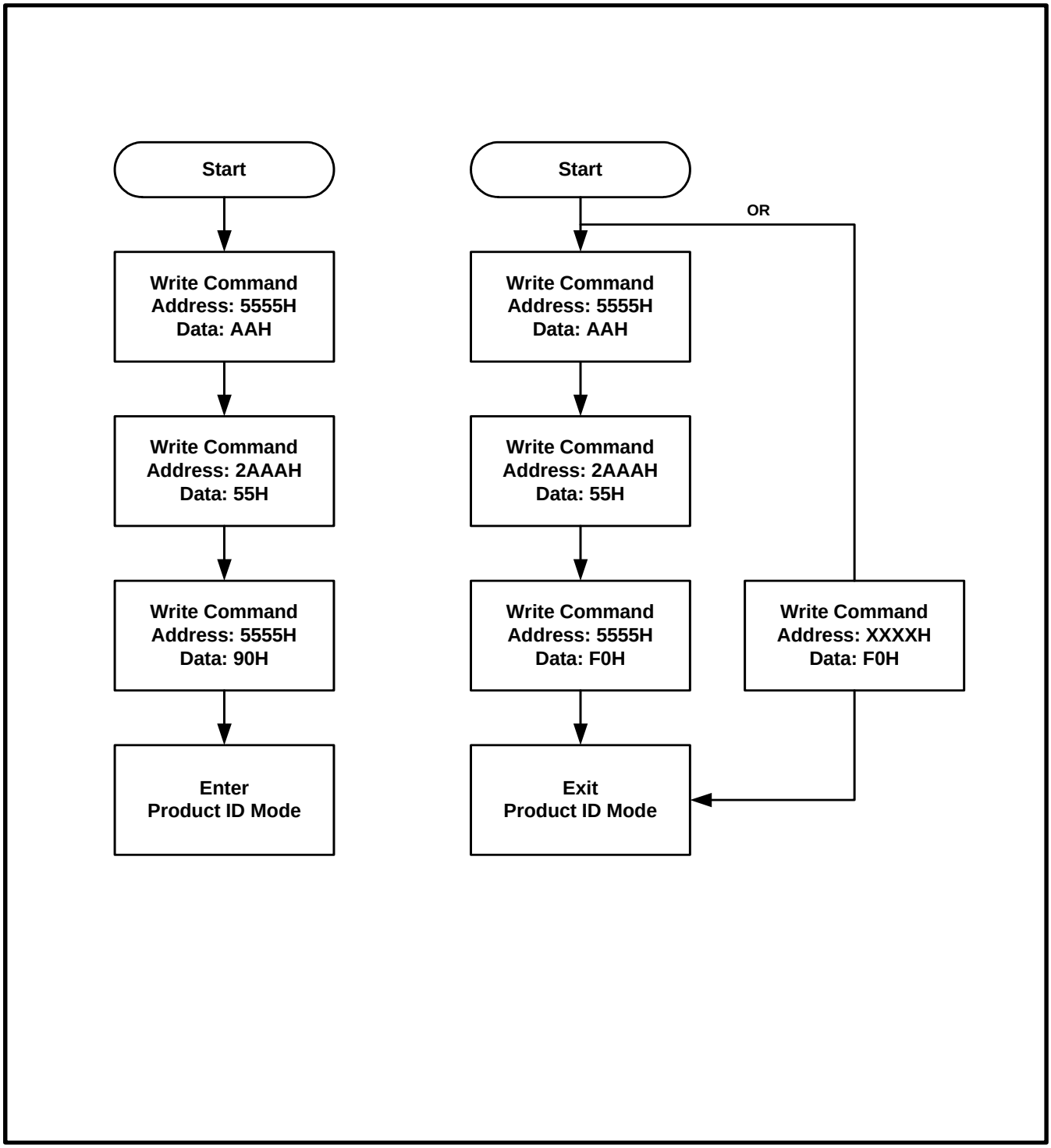
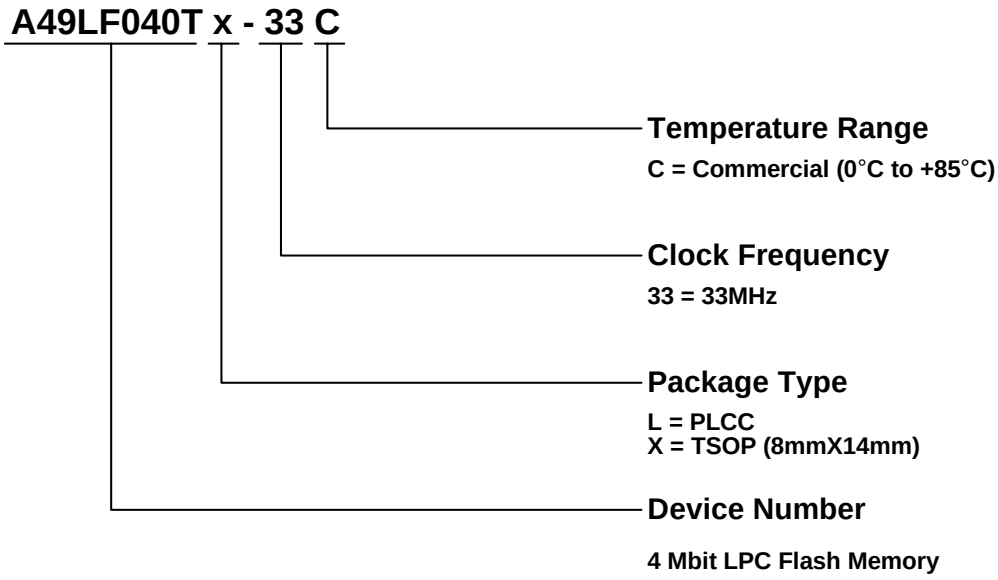


Figure 22: Product ID Command Flowchart



Ordering Information

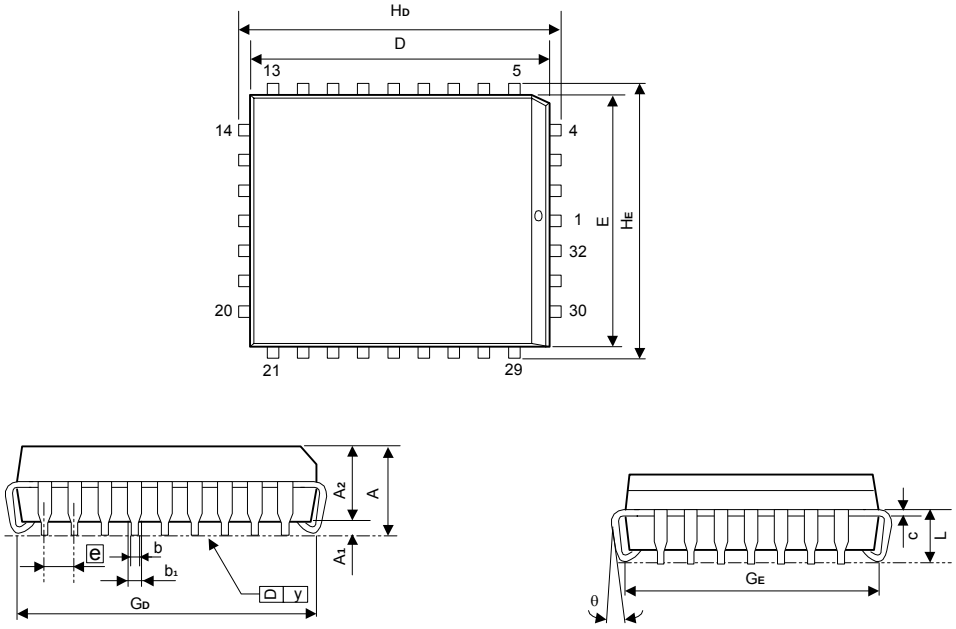


Part No.	Clock Frequency (MHz)	Boot Block Location	Temperature Range	Package Type
A49LF040TL-33	33	Top	0°C to +85°C	32-pin PLCC
A49LF040TL-33F		Top	0°C to +85°C	32-pin Pb-Free PLCC
A49LF040TX-33		Top	0°C to +85°C	32-pin TSOP (8mm X 14 mm)
A49LF040TX-33F		Top	0°C to +85°C	32-pin Pb-Free TSOP (8mm X 14 mm)

Package Information

PLCC 32L Outline Dimension

unit: inches/mm

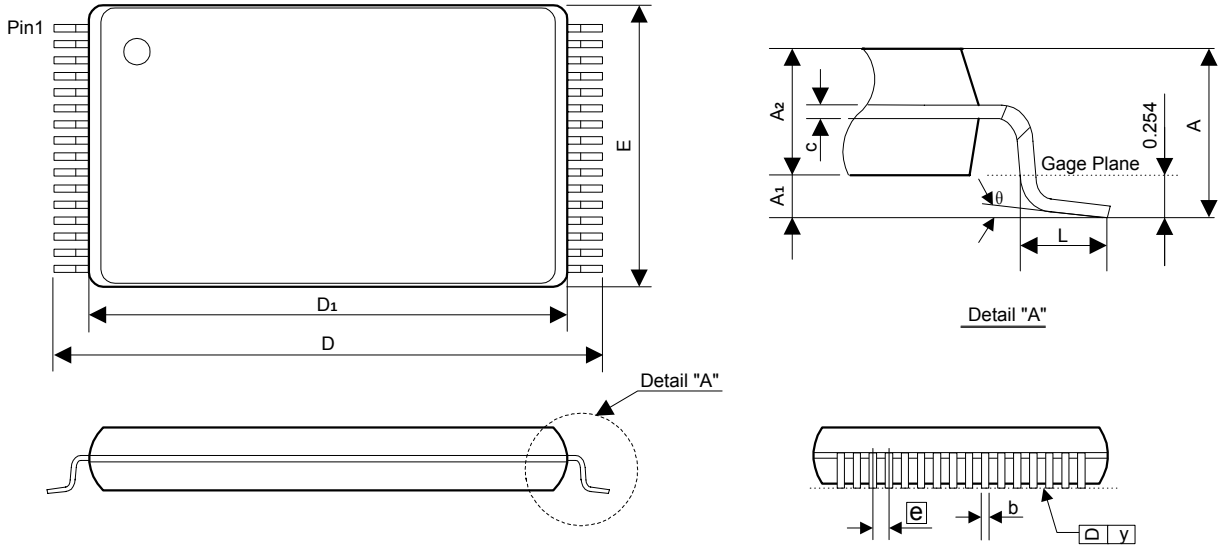


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.134	-	-	3.40
A_1	0.0185	-	-	0.47	-	-
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.021	0.41	0.46	0.54
C	0.008	0.010	0.014	0.20	0.254	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	-	-	0.003	-	-	0.075
θ	0°	-	10°	0°	-	10°

Notes:
1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

Package Information

TSOP 32L TYPE I (8 X 14mm) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.0067	0.0087	0.0106	0.17	0.22	0.27
c	0.004	-	0.0083	0.10	-	0.21
E	0.311	0.315	0.319	7.90	8.00	8.10
e	-	0.0197	-	-	0.50	-
D	0.543	0.551	0.559	13.80	14.00	14.20
D_1	0.484	0.488	0.492	12.30	12.40	12.50
L	0.020	0.024	0.028	0.50	0.60	0.70
y	0.000	-	0.003	0.00	-	0.076
θ	0°	3°	5°	0°	3°	5°

Notes:
1. Dimension E does not include mold flash.
2. Dimension D_1 does not include interlead flash.
2. Dimension b does not include dambar protrusion.