Document Title

128K X 8 BIT HIGH SPEED CMOS SRAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	September 17, 1999	Preliminary
0.1	Change V_{DR}(Max.) from 3.6V to 5.5V Add 32-pin SOP package Modify 32-pin SOJ package outline drawing and Dimensions	November 30, 1999	
0.2	Add 15ns part Change operating current from 180mA to 150mA (Max.) Change V_{DR}(Min.) from 2V to 3V Remove 32-pin SOP package	January 19, 2000	

Preliminary

128K X 8 BIT HIGH SPEED CMOS SRAM

Features

- Single + 5V power supply
- Access times: 10/12/15 ns (max.)
- Current: Operating: 150mA (max.)
  Standby: 12mA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL compatible
- Common I/O using three-state output
- Data retention voltage: 3V (min.)
- Available in 32-pin SOJ and TSOP packages

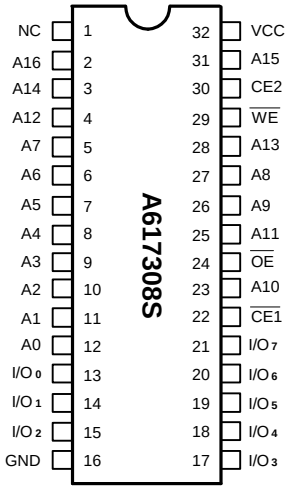
General Description

The A617308 is a high-speed, low-power 1,048,576-bit static random access memory organized as 131,072 words by 8 bits and operates on a single 5V power supply. It is built using high performance CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

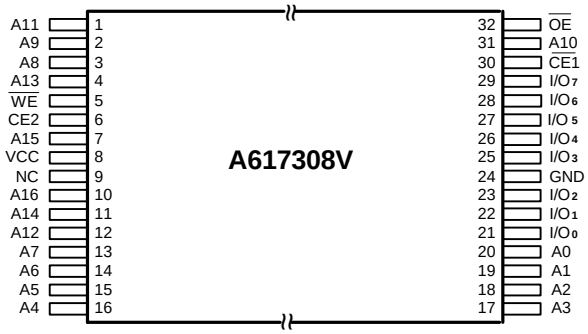
Minimum standby power is drawn by this device when chip enable is disable, independent of the other input levels.
Data retention is guaranteed at a power supply voltage as low as 3V.

Pin Configurations

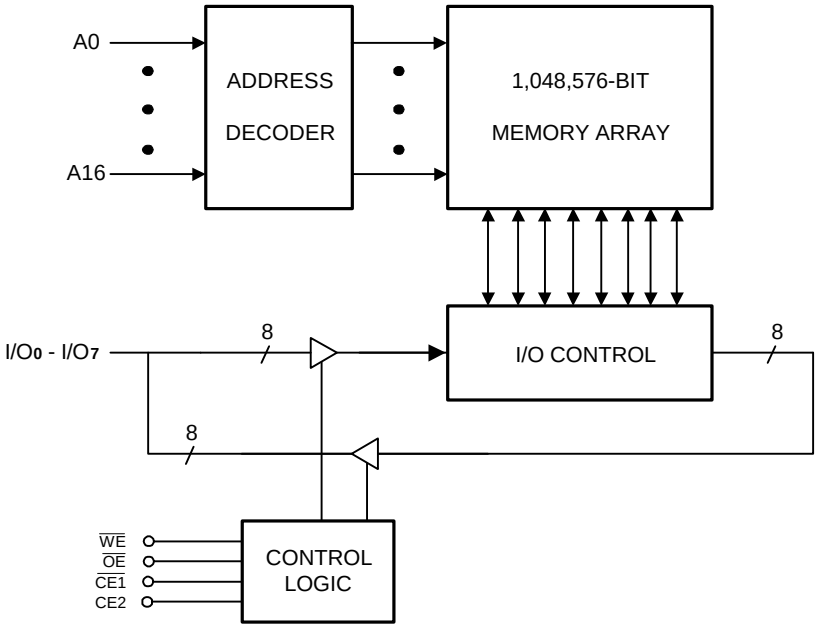
■ **SOJ**



■ **TSOP**



Block Diagram



Pin Descriptions – SOJ

Pin No.	Symbol	Description
2 - 12, 23, 25 - 28, 31	A0 - A16	Address Inputs
13 - 15, 17 - 21	I/O0 - I/O7	Data Inputs/Outputs
22	$\overline{CE1}$	Chip Enable 1
30	CE2	Chip Enable 2
24	$\overline{OE}$	Output Enable
29	$\overline{WE}$	Write Enable
32	VCC	Power Supply
16	GND	Ground
1	NC	No Connection

Pin Description - TSOP

Pin No.	Symbol	Description
1 - 4, 7, 10 - 20, 31	A0 - A16	Address Inputs
21 - 23, 25 - 29	I/O0 - I/O7	Data Inputs/Outputs
30	$\overline{CE1}$	Chip Enable 1
6	CE2	Chip Enable 2
32	$\overline{OE}$	Output Enable
5	$\overline{WE}$	Write Enable
8	VCC	Power Supply
24	GND	Ground
9	NC	No Connection

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	VCC + 0.5	V
V_{IL}	Input Low (1) Voltage	-0.5	0	+0.8	V
C_L	Output Load	-	-	30	pF

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +7V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC +0.5V
Operating Temperature, Topr . . . . . 0°C to +70°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Temperature Under Bias, Tbias . . . . . -10°C to +85°C
Power Dissipation, P_T 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, VCC = 5V ± 10%, GND = 0V)

Symbol	Parameter	A617308-10/12/15		Unit	Conditions
		Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage	-	5	µA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage	-	5	µA	$\overline{CE1}$ = V_{IH}, CE2= V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to VCC
I_{CC1} (2)	Dynamic Operating Current	-	150	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} , $I_{I/O}$ = 0 mA Min. Cycle, Duty = 100%
I_{SB}	Standby Power Supply Current	-	35	mA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}
I_{SB1}		-	12	mA	$\overline{CE1}$ ≥ VCC - 0.2V, CE2 ≤ 0.2V V_{IN} ≥ VCC -0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -4 mA

Notes: 1. V_{IL} = -3.0V for pulses less than 20 ns.
2. I_{CC1} is dependent on output loading, cycle rates, and Read/Write patterns.

Truth Table

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	H	High Z	I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC1}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance	-	8	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance	-	8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, VCC = 5V ± 10%)

Symbol	Parameter	A617308-10		A617308-12		A617308-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10	-	12	-	15	-	ns
t_{AA}	Address Access Time	-	10	-	12	-	15	ns
t_{ACE}	Chip Enable Access Time	-	10	-	12	-	15	ns
t_{OE}	Output Enable to Output Valid	-	5	-	6	-	8	ns
t_{CLZ}	Chip Enable to Output in Low Z	3	-	3	-	3	-	ns
t_{OLZ}	Output Enable to Output in Low Z	0	-	0	-	0	-	ns
t_{CHZ}	Chip Disable Output in High Z	0	5	0	6	-	8	ns
t_{OHZ}	Output Disable to Output in High Z	0	5	0	6	0	8	ns
t_{OH}	Output Hold from Address Change	3	-	3	-	3	-	ns

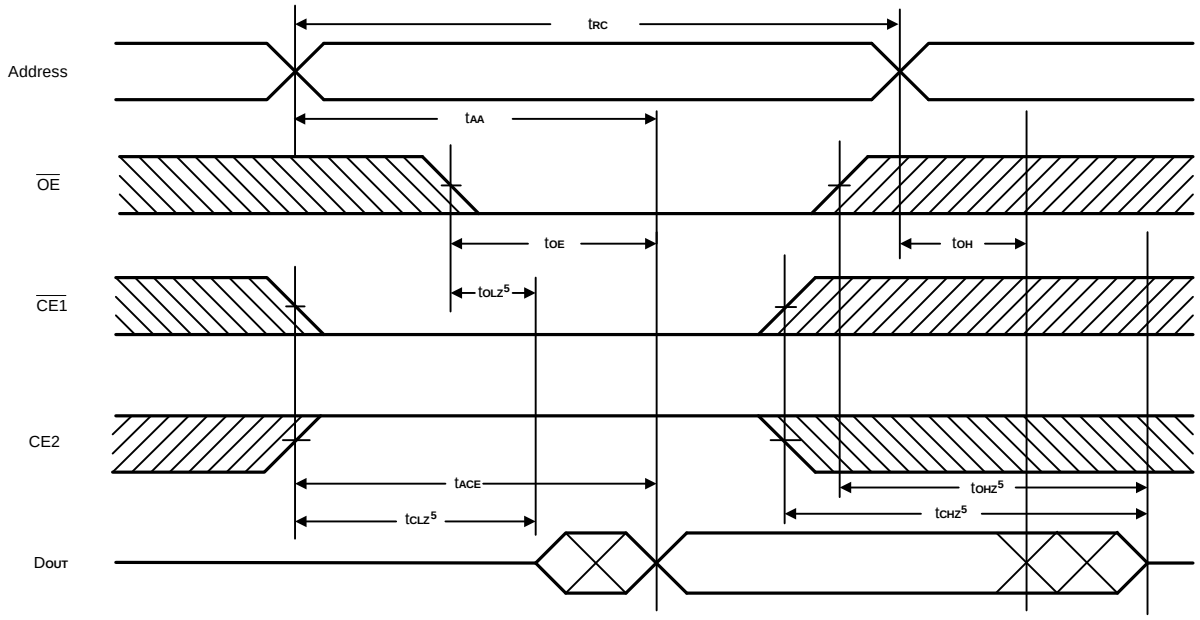
AC Characteristics (continued)

Symbol	Parameter	A617308-10		A617308-12		A617308-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle								
t_{WC}	Write Cycle Time	10	-	12	-	15	-	ns
t_{CW}	Chip Enable to End of Write	9	-	10	-	12	-	ns
t_{AS}	Address Setup Time of Write	0	-	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	9	-	10	-	12	-	ns
t_{WP}	Write Pulse Width	9	-	10	-	12	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	0	5	0	6	0	8	ns
t_{DW}	Data to Write Time Overlap	5	-	6	-	7	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
t_{OW}	Output Active from End of Write	3	-	3	-	3	-	ns

Notes: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

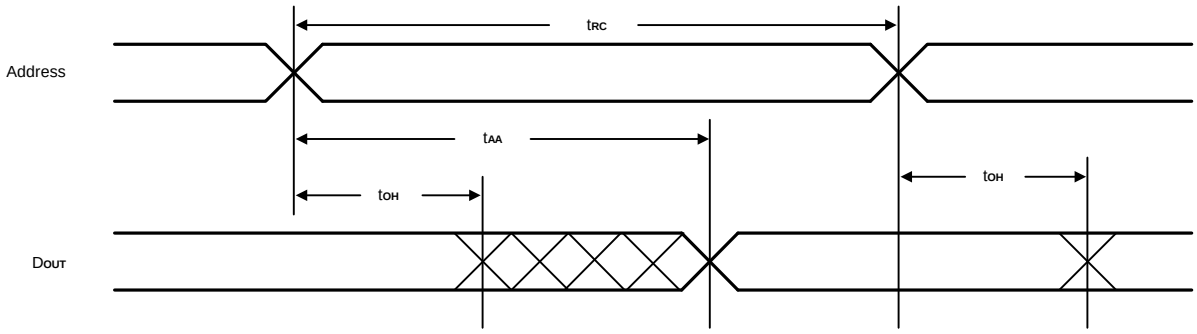
Timing Waveforms

Read Cycle 1[(1)]

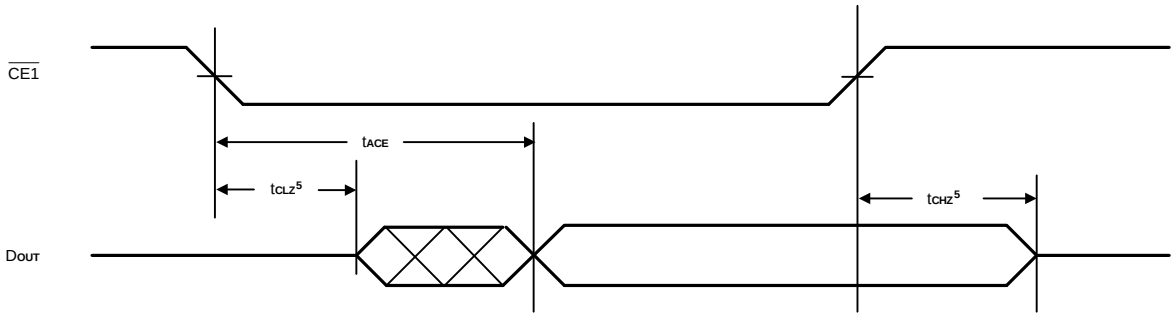


Timing Waveforms (continued)

Read Cycle 2[1, 2, 4]

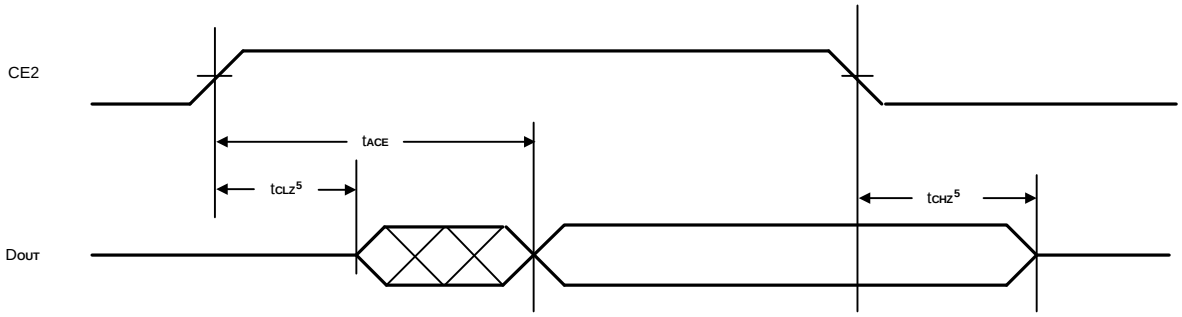


Read Cycle 3[1, 3, 4, 6]



Timing Waveforms (continued)

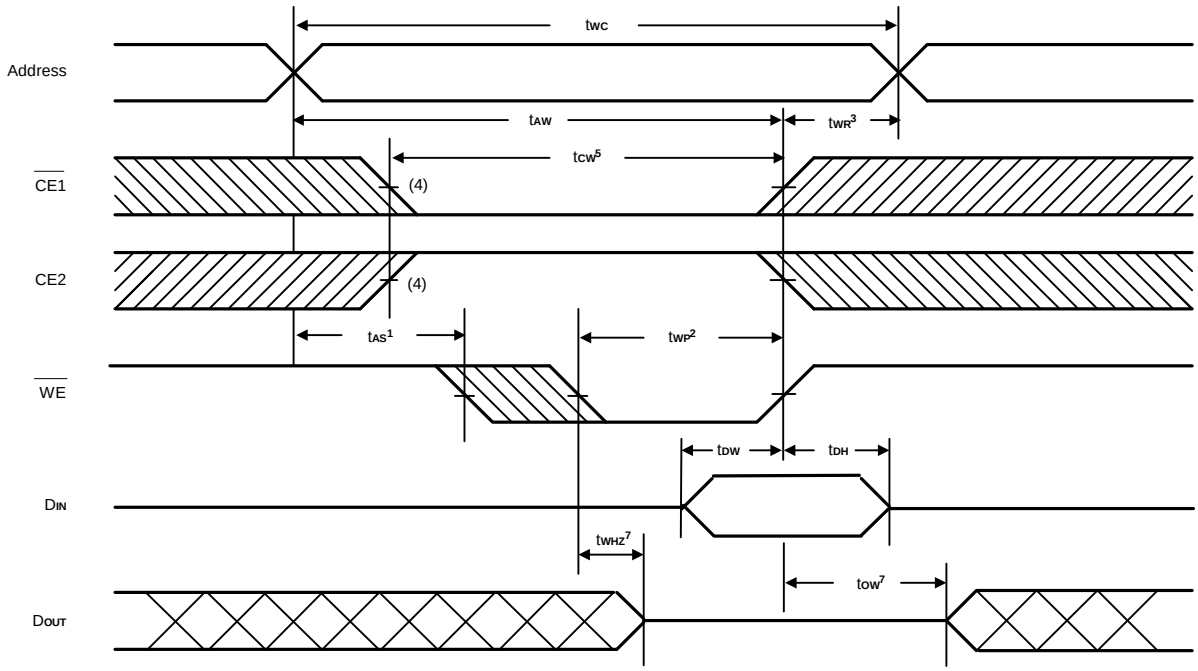
Read Cycle 4(1, 4, 7, 8)



Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled, $\overline{CE1}$= V_{IL} and CE2= V_{IH}
3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high.
7. $\overline{CE1}$ is low.
8. Address valid prior to or coincident with CE2 transition high.

Write Cycle 1(6)

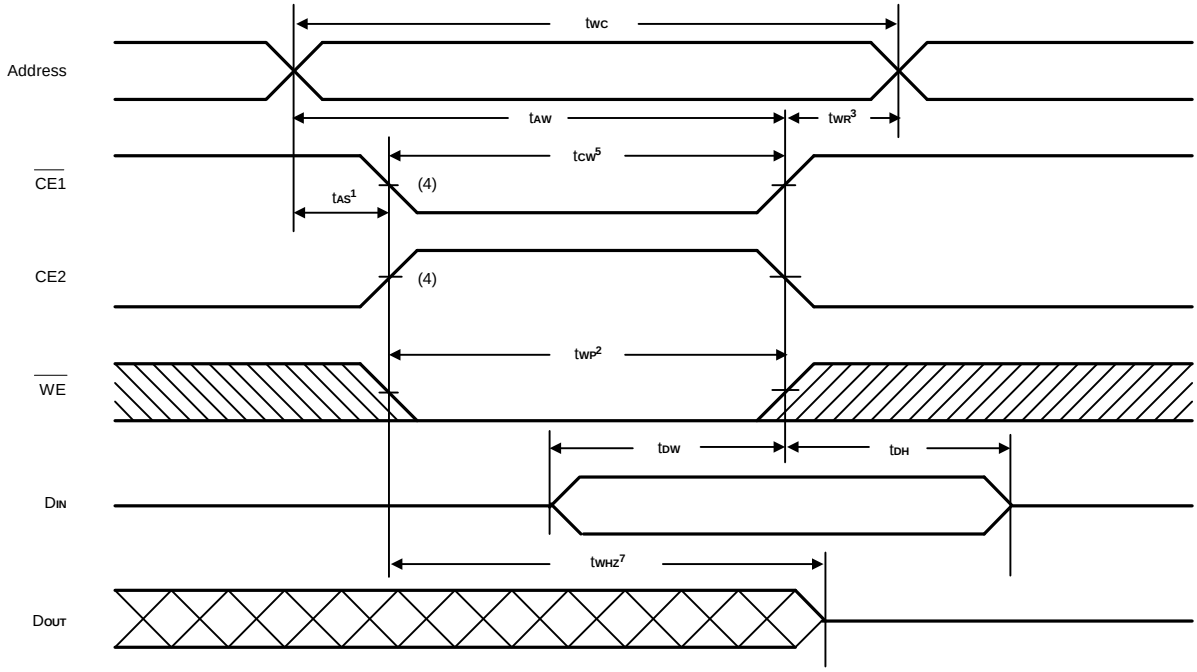
(Write Enable Controlled)



Timing Waveforms (continued)

Write Cycle 2

(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low to the end of the Write cycle.
4. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
7. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Time	2 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

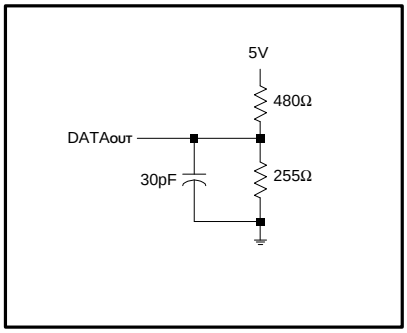


Figure 1. Output Load

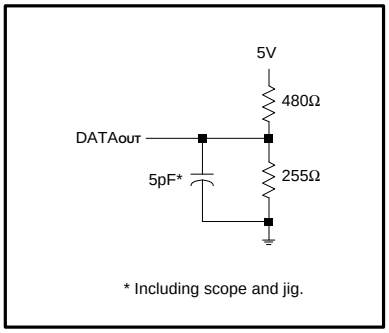


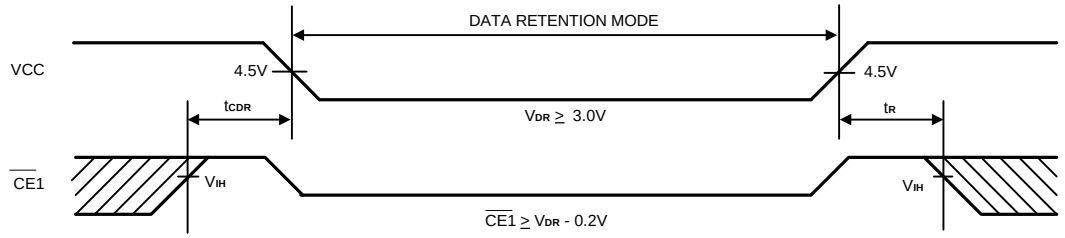
Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0°C to 70°C)

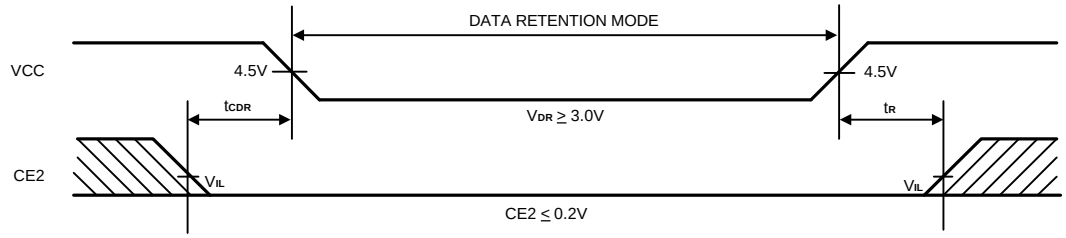
Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	3	5.5	V	$\overline{CE1} \geq$ VCC - 0.2V
I_{CCDR}	Data Retention Current	-	1	mA	VCC = 3.0V $\overline{CE1} \geq$ VCC - 0.2V CE2 ≤ 0.2V $V_{IN} \geq$ VCC - 0.2V or $V_{IN} \leq$ 0.2V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	T_{RC}*	-	ms	

t_{RC} = Read Cycle Time

Low VCC Data Retention Waveform (1) ($\overline{CE1}$ controlled)



Low VCC Data Retention Waveform (2) (CE2 controlled)



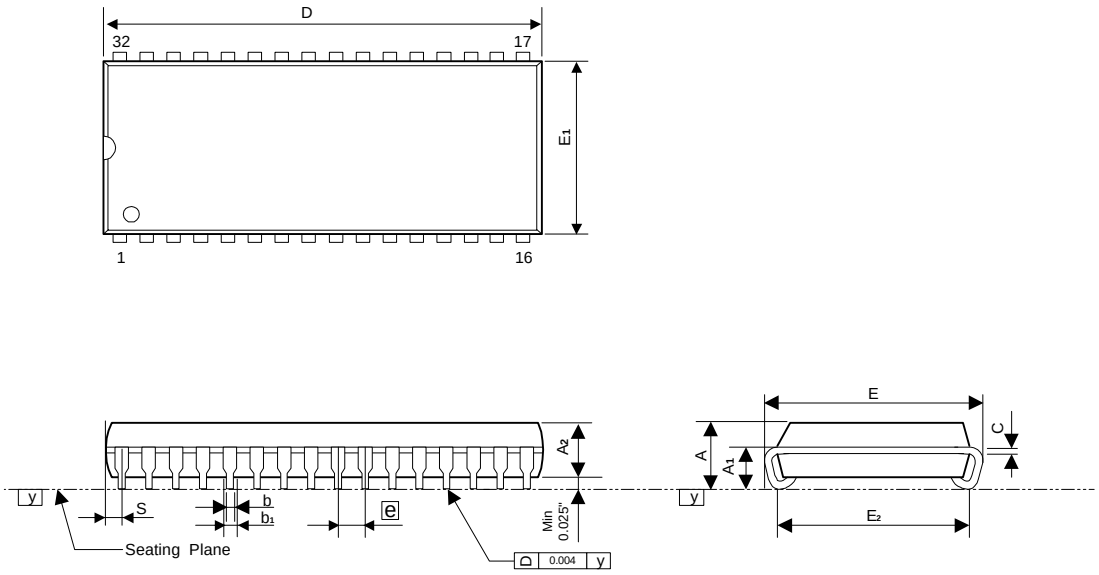
Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
A617308S-10	10	150	12	32L SOJ
A617308S-12	12	150	12	32L SOJ
A617308S-15	15	150	12	32L SOJ
A617308V-10	10	150	12	32L TSOP
A617308V-12	12	150	12	32L TSOP
A617308V-15	15	150	12	32L TSOP

Package Information

SOJ 32L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.128	0.132	0.140	3.25	3.35	3.56
A_1	0.052	-	-	2.08	-	-
A_2	0.095	0.100	0.105	2.41	2.54	2.67
b	0.016	0.018	0.020	0.41	0.46	0.51
b_1	0.026	0.028	0.032	0.66	0.71	0.81
C	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.825	0.830	20.83	20.96	21.08
E	0.330	0.335	0.340	8.39	8.51	8.63
E_1	0.295	0.300	0.305	7.49	7.62	7.75
E_2	0.260	0.267	0.274	6.61	6.78	6.96
e	-	0.050	-	-	1.27	-
S	-	-	0.048	-	-	1.22
y	-	-	0.004	-	-	0.10

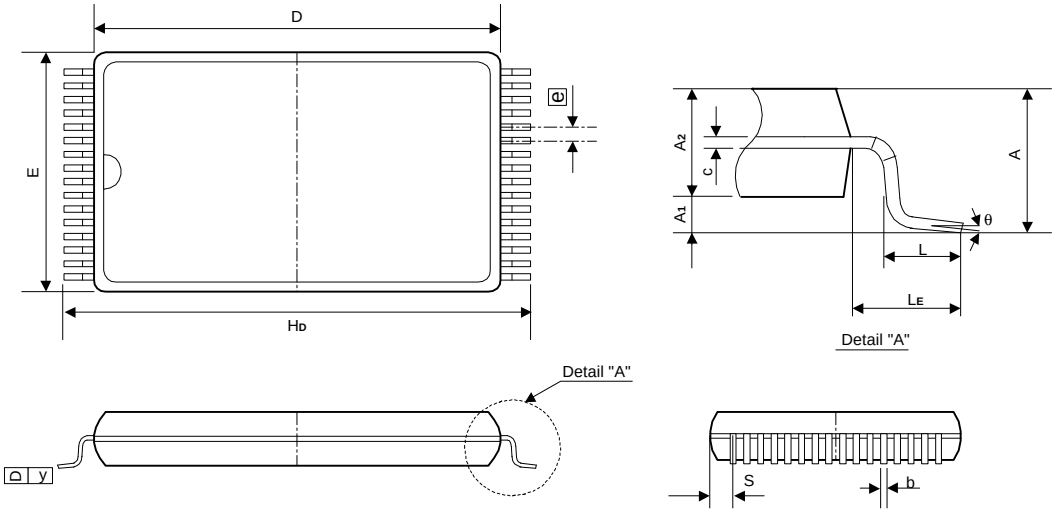
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension E_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.11	-	0.20
D	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.315	0.319	-	8.00	8.10
e	0.020 BSC			0.50 BSC		
H_D	0.779	0.787	0.795	19.80	20.00	20.20
L	0.016	0.020	0.024	0.40	0.50	0.60
L_E	-	0.032	-	-	0.80	-
S	-	-	0.020	-	-	0.50
y	-	-	0.003	-	-	0.08
θ	0°	-	5°	0°	-	5°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.