



A62S8316 Series

Preliminary

256K X 16 BIT LOW VOLTAGE CMOS SRAM

Document Title

256K X 16 BIT LOW VOLTAGE CMOS SRAM

Revision History

| <u>Rev. No.</u> | <u>History</u> | <u>Issue Date</u> | <u>Remark</u> |
|-----------------|----------------|-------------------|---------------|
| 0.0 | Initial issue | February 12, 2001 | Preliminary |



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Preliminary

256K X 16 BIT LOW VOLTAGE CMOS SRAM

Features

- Operating voltage: 2.7V to 3.6V
- Access times: 70 ns (max.)
- Current:
 - A62S8316-S series: Operating: 50mA (max.)
Standby: 10µA (max.)
 - A62S8316-SI series: Operating: 50mA (max.)
Standby: 15µA (max.)
- Extended operating temperature range : -25°C to 85°C for -SI series
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2V (min.)
- Available in 44-pin TSOP and 48-ball Mini BGA (6X8) packages.

General Description

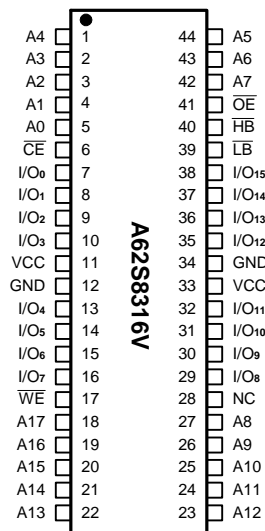
The A62S8316 is a low operating current 4,194,304-bit static random access memory organized as 262,144 words by 16 bits and operates on low power supply voltage from 2.7V to 3.6V. It is built using AMIC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing. Data retention is guaranteed at a power supply voltage as low as 2V.

Pin Configuration

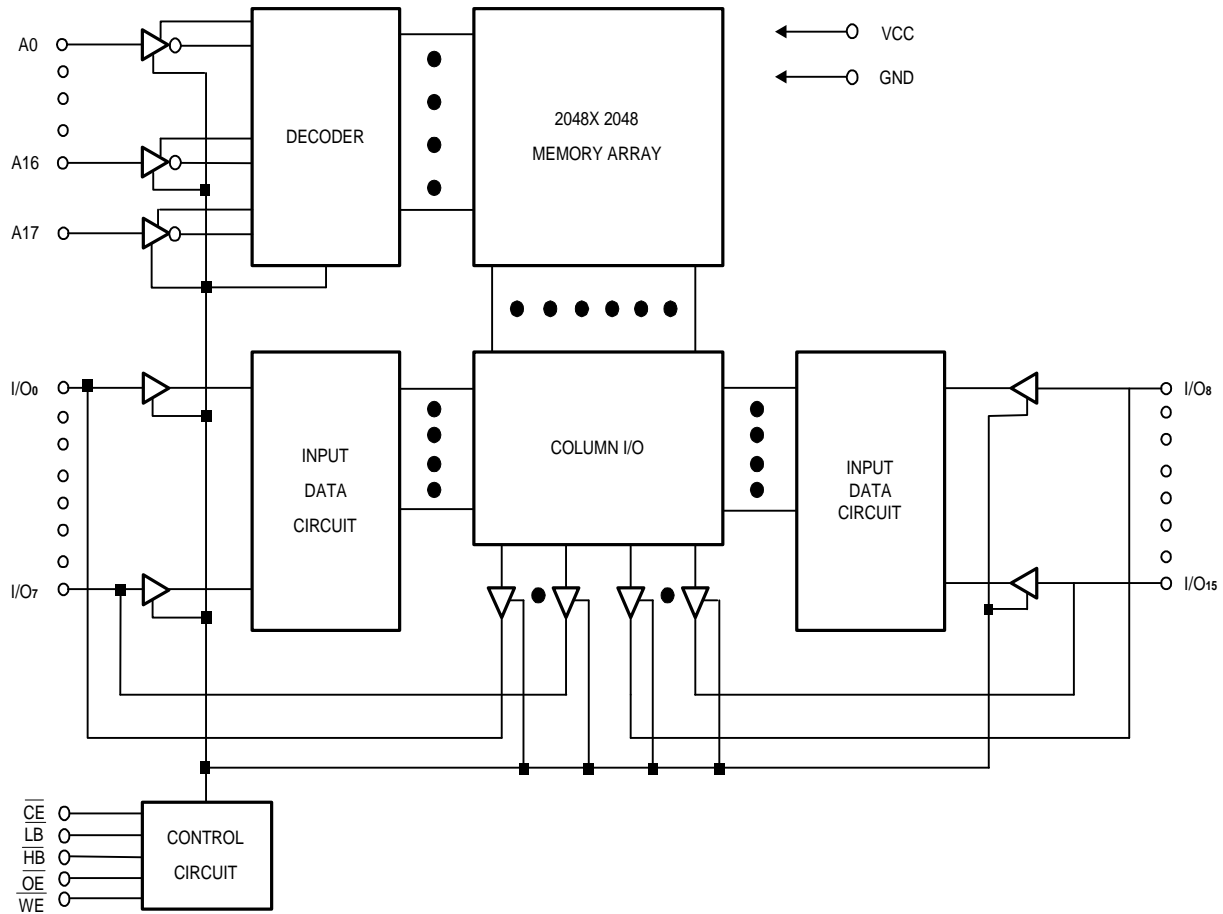
■ TSOP (Type II)



■ Mini BGA (6X8) Top View

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------------|------------------------|-----|-----|------------------------|------------------|
| A | $\overline{\text{LB}}$ | $\overline{\text{OE}}$ | A0 | A1 | A2 | NC |
| B | I/O ₈ | $\overline{\text{HB}}$ | A3 | A4 | $\overline{\text{CS}}$ | I/O ₀ |
| C | I/O ₉ | I/O ₁₀ | A5 | A6 | I/O ₁ | I/O ₂ |
| D | VSS | I/O ₁₁ | A17 | A7 | I/O ₃ | VCC |
| E | VCC | I/O ₁₂ | NC | A16 | I/O ₄ | VSS |
| F | I/O ₁₄ | I/O ₁₃ | A14 | A15 | I/O ₅ | I/O ₆ |
| G | I/O ₁₅ | NC | A12 | A13 | $\overline{\text{WE}}$ | I/O ₇ |
| H | NC | A8 | A9 | A10 | A11 | NC |

A62S8316G

Block Diagram


Pin Description - TSOP

| Pin No. | Symbol | Description |
|--------------------------------------|--------------------------------------|--|
| 1 - 5, 18 - 27, 42 - 44 | A0 - A17 | Address Inputs |
| 6 | \overline{CE} | Chip Enable Input |
| 7 - 10, 13 - 16, 29 - 32, 35 - 38 | I/O ₀ - I/O ₁₅ | Data Input/Outputs |
| 17 | \overline{WE} | Write Enable Input |
| 39 | \overline{LB} | Byte Enable Input (I/O ₀ to I/O ₇) |
| 40 | \overline{HB} | Byte Enable Input (I/O ₈ to I/O ₁₅) |
| 41 | \overline{OE} | Output Enable Input |
| 11, 33 | VCC | Power |
| 12, 34 | GND | Ground |
| 28 | NC | No Connection |

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C or -25°C to 85°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|------|------|-----------|------|
| VCC | Supply Voltage | 2.7 | 3.0 | 3.6 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.4 | - | VCC + 0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 | - | +0.6 | V |
| C _L | Output Load | - | - | 30 | pF |
| TTL | Output Load | - | - | 1 | - |



Absolute Maximum Ratings*

VCC to GND -0.5V to +4.6V
 IN, IN/OUT Volt to GND -0.5V to VCC + 0.5V
 Operating Temperature, T_{opr} -25°C to +85°C
 Storage Temperature, T_{stg} -55°C to +125°C
 Power Dissipation, P_T 0.7W
 Soldering Temp. & Time 260°C, 10 sec

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C or -25°C to 85°C, VCC = 2.7V to 3.6V, GND = 0V)

| Symbol | Parameter | A62S8316-70S | | A62S8316-70SI | | Unit | Conditions |
|------------------|------------------------------|--------------|------|---------------|------|------|--|
| | | Min. | Max. | Min. | Max. | | |
| I _{LI} | Input Leakage Current | - | 1 | - | 1 | μA | V _{IN} = GND to VCC |
| I _{LO} | Output Leakage Current | - | 1 | - | 1 | μA | $\overline{CE} = V_{IH}$ or $\overline{LB} = V_{IH}$ or $\overline{HB} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{IO} = GND to VCC |
| I _{CC} | Active Power Supply Current | - | 5 | - | 5 | mA | $\overline{CE} = V_{IL}$, I _{IO} = 0mA |
| I _{CC1} | Dynamic Operating Current | - | 50 | - | 50 | mA | Min. Cycle, Duty = 100% $\overline{CE} = V_{IL}$, I _{IO} = 0mA |
| I _{CC2} | | - | 10 | - | 10 | mA | $\overline{CE} = V_{IL}$, V _{IH} = VCC, V _{IL} = 0V, f = 1MHz, I _{IO} = 0 mA |
| I _{SB} | Standby Power Supply Current | - | 0.5 | - | 0.5 | mA | $\overline{CE} = V_{IH}$ |
| I _{SB1} | | - | 10 | - | 15 | μA | $\overline{CE} \geq VCC - 0.2V$ V _{IN} ≥ 0V |
| V _{OL} | Output Low Voltage | - | 0.4 | - | 0.4 | V | I _{OL} = 2.1mA |
| V _{OH} | Output High Voltage | 2.2 | - | 2.2 | - | V | I _{OH} = -1.0mA |



Truth Table

| \overline{CE} | \overline{OE} | \overline{WE} | \overline{LB} | \overline{HB} | I/O ₀ to I/O ₇ Mode | I/O ₈ to I/O ₁₅ Mode | VCC Current |
|-----------------|-----------------|-----------------|-----------------|-----------------|---|--|---|
| H | X | X | X | X | Not selected | Not selected | I _{SB1} , I _{SB} |
| L | L | H | L | L | Read | Read | I _{CC1} , I _{CC2} , I _{CC} |
| | | | L | H | Read | High - Z | I _{CC1} , I _{CC2} , I _{CC} |
| | | | H | L | High - Z | Read | I _{CC1} , I _{CC2} , I _{CC} |
| L | X | L | L | L | Write | Write | I _{CC1} , I _{CC2} , I _{CC} |
| | | | L | H | Write | Not Write/Hi - Z | I _{CC1} , I _{CC2} , I _{CC} |
| | | | H | L | Not Write/Hi - Z | Write | I _{CC1} , I _{CC2} , I _{CC} |
| L | H | H | L | X | High - Z | High - Z | I _{CC1} , I _{CC2} , I _{CC} |
| | | | X | L | High - Z | High - Z | I _{CC1} , I _{CC2} , I _{CC} |
| X | X | X | H | H | Not selected | Not selected | I _{SB1} , I _{SB} |

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|-------------------|--------------------------|------|------|------|----------------------|
| C _{IN} * | Input Capacitance | - | 6 | pF | V _{IN} = 0V |
| C _{IO} * | Input/Output Capacitance | - | 8 | pF | V _{IO} = 0V |

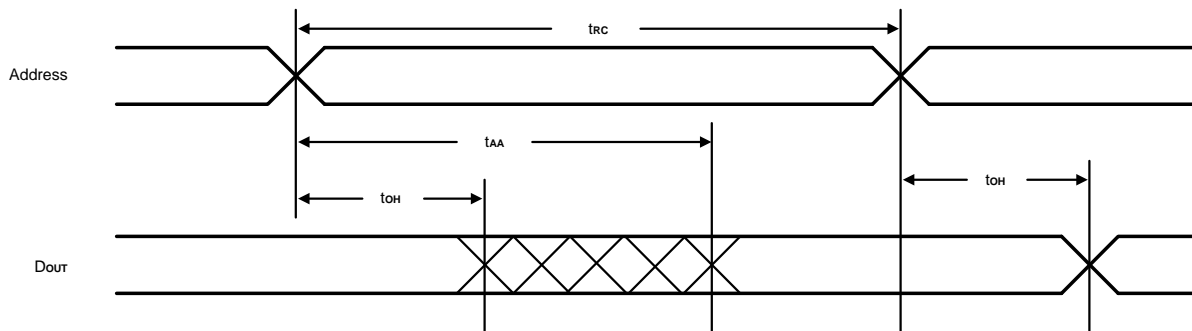
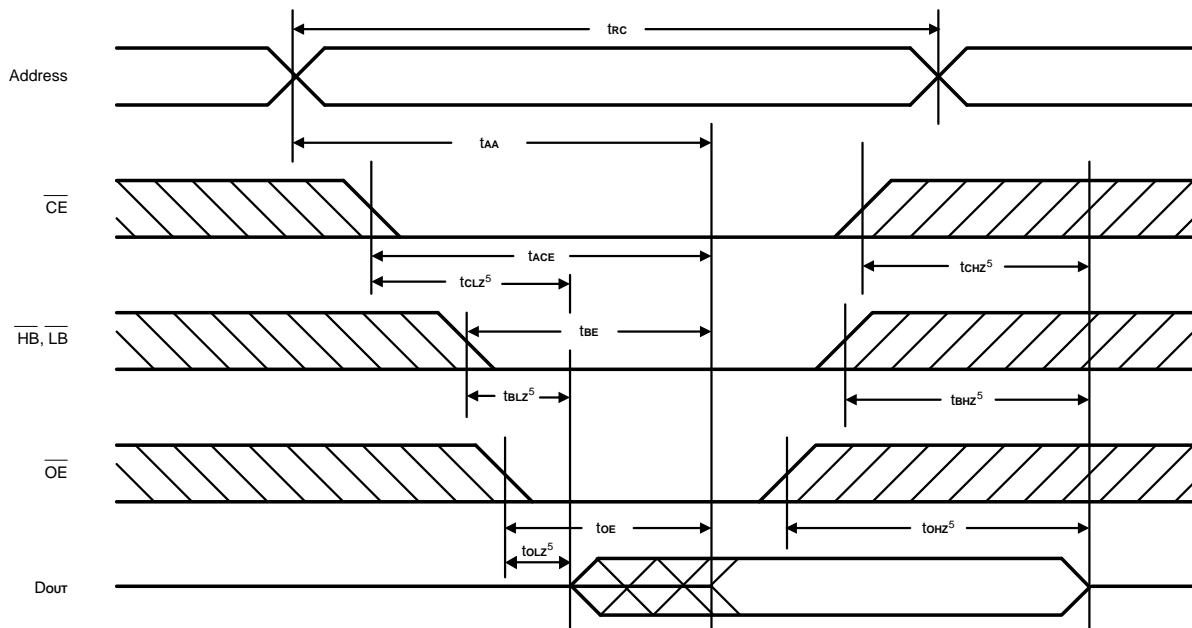
* These parameters are sampled and not 100% tested.



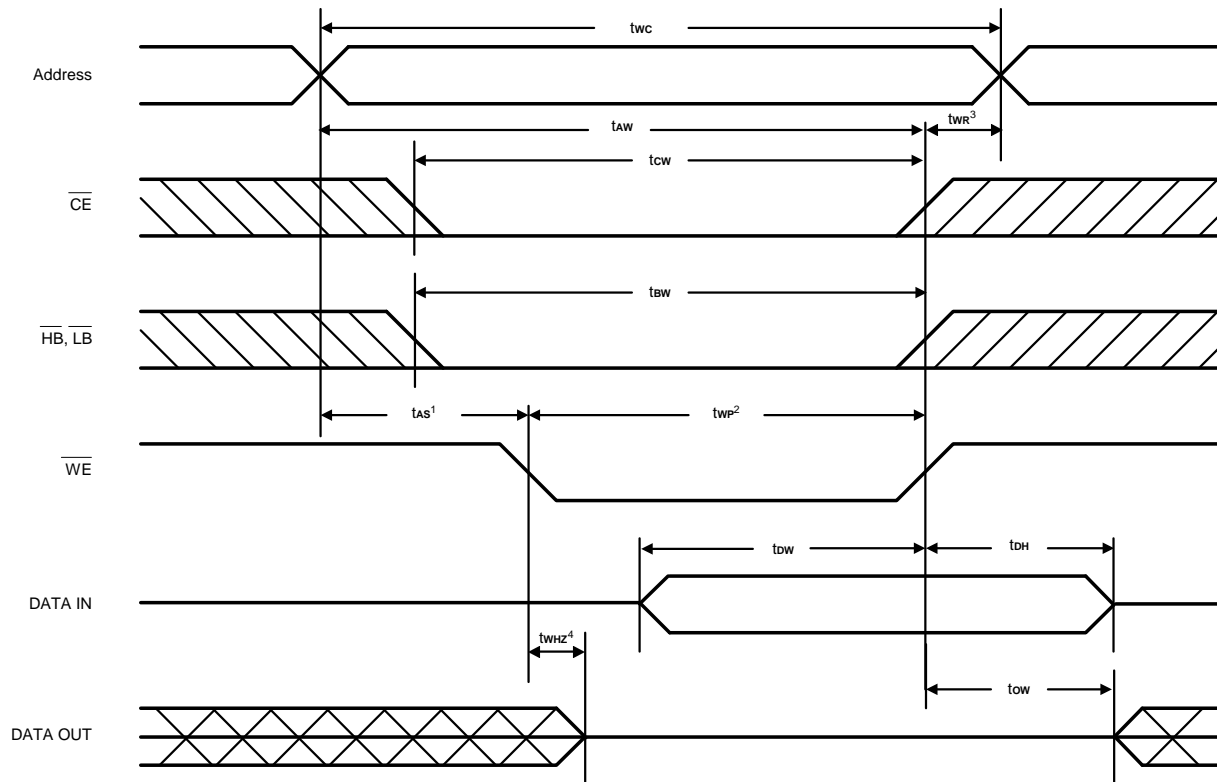
AC Characteristics (T_A = 0°C to +70°C or -25°C to 85°C, VCC = 2.7V to 3.6V)

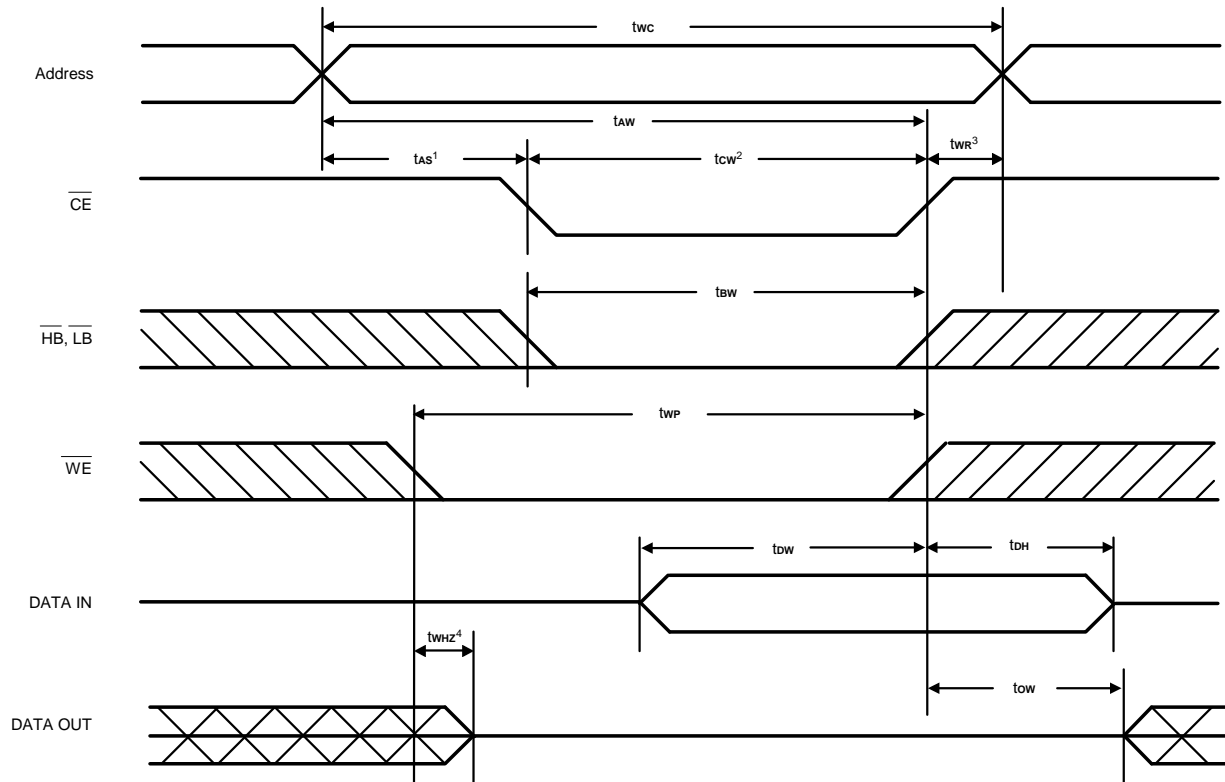
| Symbol | Parameter | A62S8316-70S/SI | | Unit |
|------------------|------------------------------------|-----------------|------|------|
| | | Min. | Max. | |
| Read Cycle | | | | |
| t _{RC} | Read Cycle Time | 70 | - | ns |
| t _{AA} | Address Access Time | - | 70 | ns |
| t _{ACE} | Chip Enable Access Time | - | 70 | ns |
| t _{BE} | Byte Enable Access Time | - | 70 | ns |
| t _{OE} | Output Enable to Output Valid | - | 35 | ns |
| t _{CLZ} | Chip Enable to Output in Low Z | 10 | - | ns |
| t _{BLZ} | Byte Enable to Output in Low Z | 5 | - | ns |
| t _{OLZ} | Output Enable to Output in Low Z | 5 | - | ns |
| t _{CHZ} | Chip Disable to Output in High Z | - | 25 | ns |
| t _{BHZ} | Byte Disable to Output in High Z | - | 25 | ns |
| t _{OHZ} | Output Disable to Output in High Z | - | 25 | ns |
| t _{OH} | Output Hold from Address Change | 10 | - | ns |
| Write Cycle | | | | |
| t _{WC} | Write Cycle Time | 70 | - | ns |
| t _{CW} | Chip Enable to End of Write | 60 | - | ns |
| t _{BW} | Byte Enable to End of Write | 60 | - | ns |
| t _{AS} | Address Setup Time | 0 | - | ns |
| t _{AW} | Address Valid to End of Write | 60 | - | ns |
| t _{WP} | Write Pulse Width | 50 | - | ns |
| t _{WR} | Write Recovery Time | 0 | - | ns |
| t _{WHZ} | Write to Output in High Z | - | 30 | ns |
| t _{DW} | Data to Write Time Overlap | 30 | - | ns |
| t _{DH} | Data Hold from Write Time | 0 | - | ns |
| t _{OW} | Output Active from End of Write | 5 | - | ns |

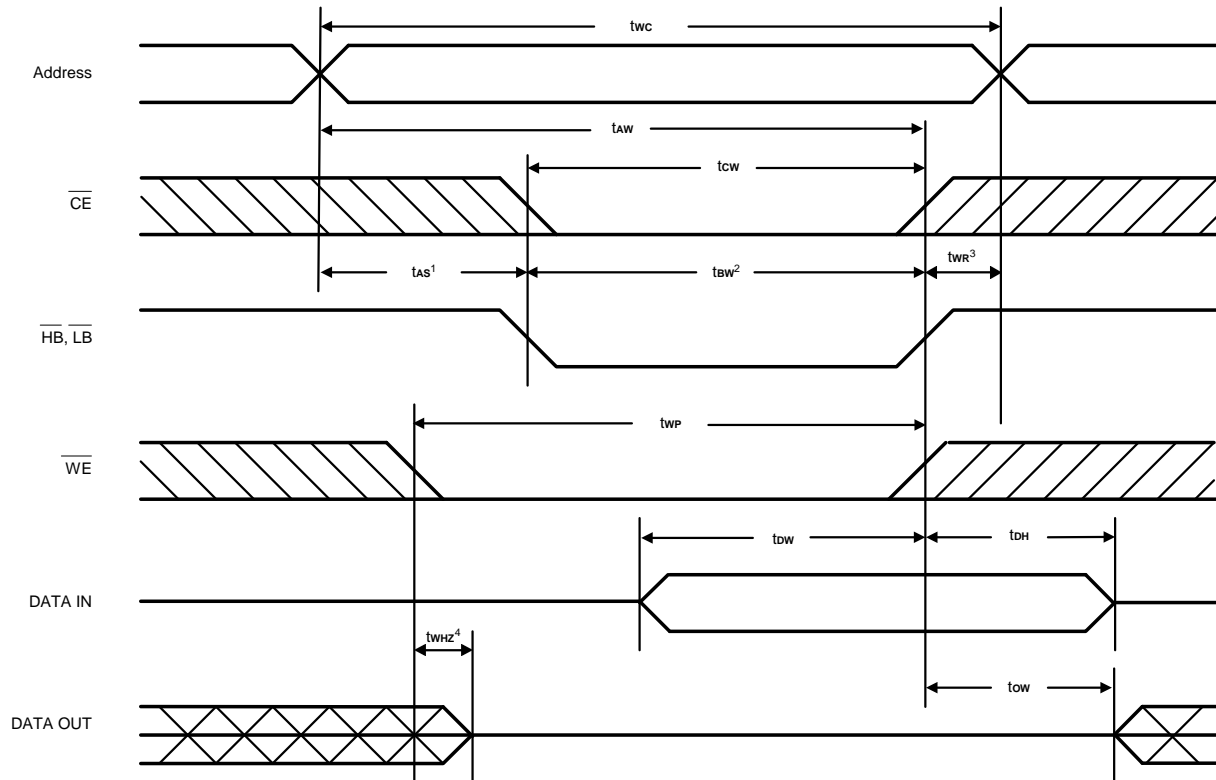
Note: t_{CHZ}, t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms
Read Cycle 1^(1, 2, 4)

Read Cycle 2^(1, 2, 3)


- Notes:
- \overline{WE} is high for Read Cycle.
 - Device is continuously enabled $\overline{CE} = V_{IL}$, $\overline{HB} = V_{IL}$ and, or $\overline{LB} = V_{IL}$.
 - Address valid prior to or coincident with \overline{CE} and (\overline{HB} and, or \overline{LB}) transition low.
 - $\overline{OE} = V_{IL}$.
 - Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.

Timing Waveforms (continued)
**Write Cycle 1
(Write Enable Controlled)**


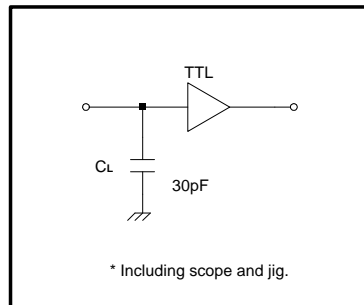
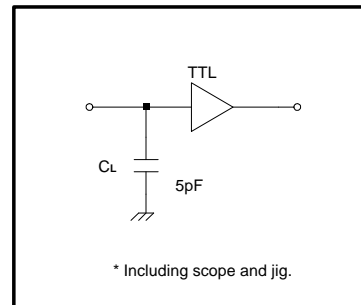
Timing Waveforms (continued)
**Write Cycle 2
(Chip Enable Controlled)**


Timing Waveforms (continued)
**Write Cycle 3
(Byte Enable Controlled)**


- Notes:
- t_{as} is measured from the address valid to the beginning of Write.
 - A Write occurs during the overlap (t_{wp}, t_{tw}) of a low \overline{CE} , \overline{WE} and (\overline{HB} and, or \overline{LB}).
 - t_{wr} is measured from the earliest of \overline{CE} or \overline{WE} or (\overline{HB} and, or \overline{LB}) going high to the end of the Write cycle.
 - \overline{OE} level is high or low.
 - Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

| | |
|--|---------------------|
| Input Pulse Levels | 0V to 3.0V |
| Input Rise And Fall Time | 5 ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Figures 1 and 2 |


Figure 1. Output Load

Figure 2. Output Load for tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, and tOW
Data Retention Characteristics (TA = 0°C to 70°C or -25°C to 85°C)

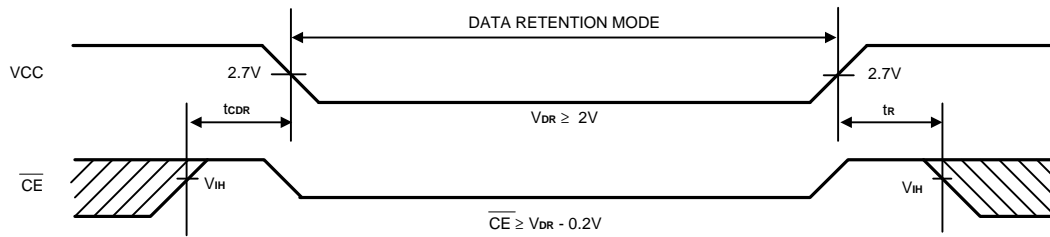
| Symbol | Parameter | Min. | Max. | Unit | Conditions | |
|-------------------|-------------------------------------|-----------------|------|------|---------------------------------|--|
| V _{DR} | VCC for Data Retention | 2.0 | 3.6 | V | $\overline{CE} \geq VCC - 0.2V$ | |
| I _{CCDR} | Data Retention Current | S-Version | - | 5* | μA | VCC = 2.0V, $\overline{CE} \geq VCC - 0.2V$ VIN ≥ 0V |
| | | SI-Version | - | 10** | | |
| t _{CDR} | Chip Disable to Data Retention Time | 0 | - | ns | See Retention Waveform | |
| t _R | Operation Recovery Time | T _{RC} | - | ns | | |

* A62S8316-70S

I_{CCDR}: max. 1μA at TA = 0°C to + 40°C

** A62S8316-70SI

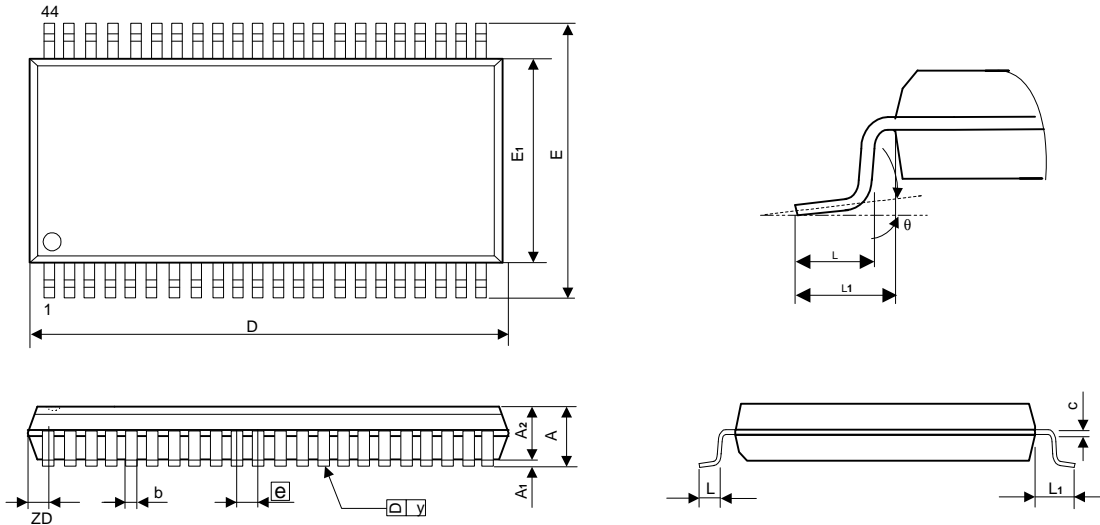
I_{CCDR}: max. 1μA at TA = 0°C to + 40°C

Low VCC Data Retention Waveform

Ordering Information

| Part No. | Access Time (ns) | Operating Current Max. (mA) | Standby Current Max. (mA) | Package |
|----------------|------------------|-----------------------------|---------------------------|--------------|
| A62S8316V-70S | 70 | 50 | 10 | 44L TSOP |
| A62S8316V-70SI | | 50 | 15 | 44L TSOP |
| A62S8316G-70S | | 50 | 10 | 48B Mini BGA |
| A62S8316G-70SI | | 50 | 15 | 48B Mini BGA |

Package Information
TSOP 44L (Type II) Outline Dimensions

unit: inches/mm



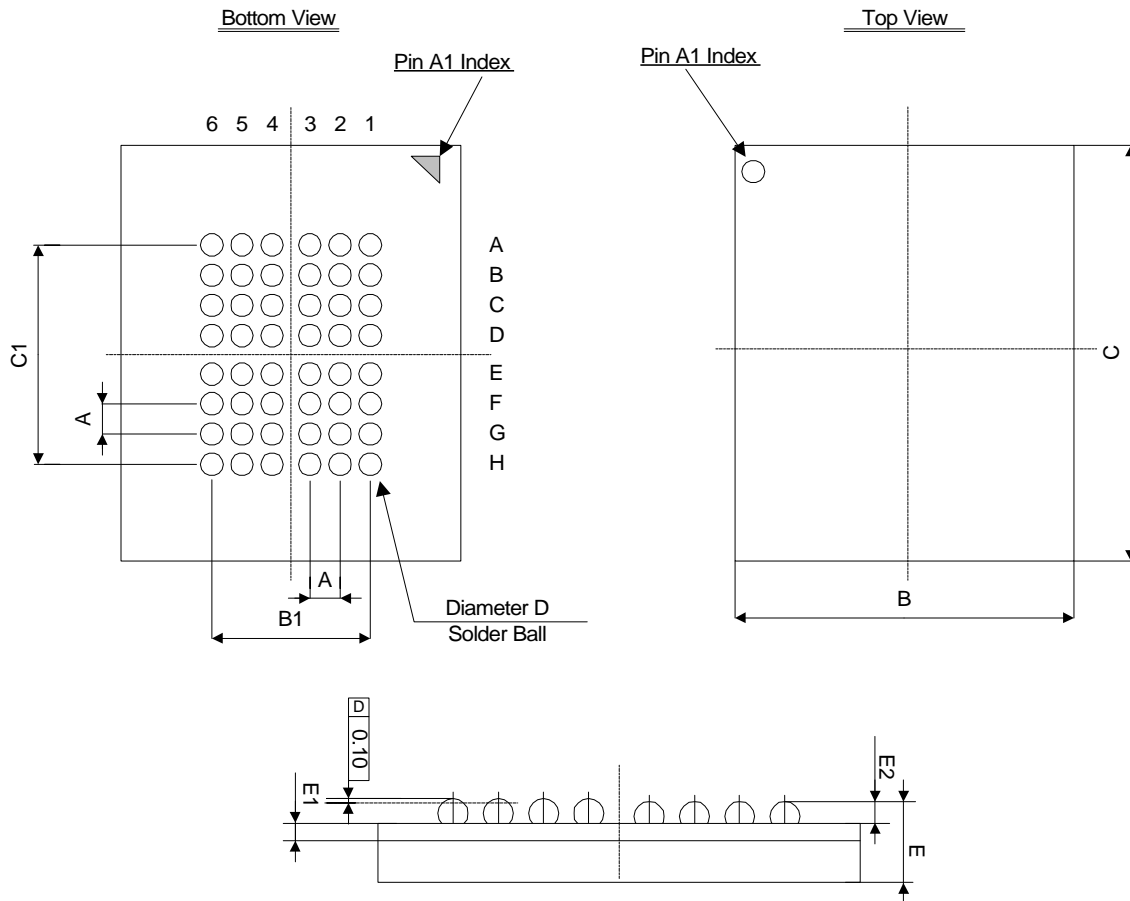
| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|----------------|----------------------|-------|-------|------------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | - | - | 0.047 | - | - | 1.20 |
| A1 | 0.002 | - | 0.006 | 0.05 | - | 0.15 |
| A2 | 0.037 | 0.039 | 0.041 | 0.95 | 1.00 | 1.05 |
| b | 0.012 | - | 0.018 | 0.30 | - | 0.45 |
| c | 0.005 | - | 0.008 | 0.12 | - | 0.21 |
| D | 0.720 | 0.725 | 0.730 | 18.28 | 18.41 | 18.54 |
| ZD | 0.032 REF | | | 0.805 REF | | |
| E | 0.455 | 0.463 | 0.471 | 11.56 | 11.76 | 11.96 |
| E1 | 0.395 | 0.400 | 0.405 | 10.03 | 10.16 | 10.29 |
| L | 0.019 | 0.023 | 0.027 | 0.49 | 0.59 | 0.69 |
| L1 | 0.031 REF | | | 0.80 REF | | |
| \overline{e} | 0.031 BSC | | | 0.80 BSC | | |
| y | - | - | 0.004 | - | - | 0.10 |
| θ | 0° | - | 5° | 0° | - | 5° |

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E1 does not include resin fins.
3. Dimension ZD includes end flash.

Package Information
Mini BGA 6X8 (48 BALLS) Outline Dimensions

unit : millimeter(mm)



| Symbol | Min | Typ | Max |
|--------|------|------|------|
| A | - | 0.75 | - |
| B | 5.90 | 6.00 | 6.10 |
| B1 | - | 3.75 | - |
| C | 7.90 | 8.00 | 8.10 |
| C1 | - | 5.25 | - |
| D | 0.30 | 0.35 | 0.40 |
| E | 1.00 | 1.10 | 1.20 |
| E1 | - | 0.36 | - |
| E2 | - | 0.22 | - |