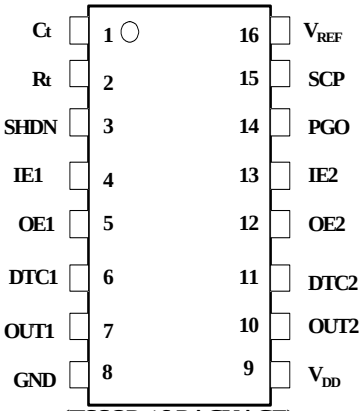
BUCK_BOOST & BOOST PWM CONTROLLER

Features

- Complete PWM Power Control Circuitry
  CH1: Buck_Boost, CH2: Boost
- Under-Voltage Lockout (UVLO) Protection
- Totem Pole Output
- Output Short Circuit Protection
- Dead-Time Control：0% to 100%
- Wide Operating Frequency：
  10kHz to 800kHz
- Shutdown Control
- Power Good Protection
- V_{DD} Range: 2.6V~6.5V

Pin Configuration

TOP VIEW



(TSSOP-16 PACKAGE)

General Description

The AAT1105A provides an integrated two-channel pulse-width-modulation (PWM) solution for the power supply of DC-DC system. This device offers system engineers the flexibility to tailor-make the power supply circuitry for specific applications. Each channel contains its own error amplifier, PWM comparator, dead–time control (DTC), and output driver. The under-voltage protection, oscillator, short circuit protection (SCP) and voltage reference circuit are the common features for the two channels.

The AAT1105A contains one step-up (boost) circuit at channel two (CH2) and one inverting (buck_boost) circuit at channel one (CH1). Dead-time control can be set to provide 0% to 100% dead-time through a resistive divider network. Soft-start can be implemented by paralleling the DTC resistor with a capacitor. Two dead-time control inputs are assigned for CH1 and CH2 individually, and dead-time control inputs can be used to control on / off operation.

The compact design and optimized external parts of AAT1105A offers a simple and effective solution.

Pin Description

Pin No	Name	I/O	Description
1	C_t	-	External Timing Capacitance
2	R_t	-	External Timing Resistance
3	SHDN	I	Shutdown Input Pin（Internal Pull "H"）
4	IE1	I	Inverting Input of Error Amplifier 1
5	OE1	O	Output for Error Amplifier 1
6	DTC1	I	Output 1 Dead-Time / Soft-Start Setting
7	OUT1	O	Output 1
8	GND	-	Ground
9	V_{DD}	-	Power Supply
10	OUT2	O	Output 2
11	DTC2	I	Output 2 Dead-Time / Soft-Start Setting
12	OE2	O	Output of Error Amplifier 2
13	IE2	I	Inverting Input of Error Amplifier 2
14	PGO	O	Power Good Output Pin
15	SCP	-	Timer Latch Setting
16	V_{REF}	O	Reference Voltage (1.293V) Output

Absolute Maximum Ratings

CHARACTERISTICS	SYMBOL	VALUE	UNIT
Supply Voltage	V_{DD}	7	V
Input Voltage (IE – , DTC, SHDN)	V_I	V_{DD}	V
Output Voltage	V_O	V_{DD} +0.3	V
Output Current	I_O	–120 /+120	mA
Operating Free-Air Temperature Range	T_C	– 20 to +85	°C
Storage Temperature Range	$T_{storage}$	– 45 to +125	°C
Power Dissipation	P_d	500	mW

Recommended Operating Conditions

	Symbol	Min	Max	Unit
Supply Voltage, V_{DD}	V_{DD}	2.6	6.5	V
Input Voltage, IE1, IE2	V_{cm}	0.3	1.5	V
Output Voltage	V_O	0	V_{DD}	V
Oscillator (OSC) Capacitance	C_{OSC}	100	15,000	pF
Oscillator (OSC) Resistance	R_{OSC}	3	50	kΩ
Oscillator (OSC) Frequency	f_{OSC}	10	800	kHz
Output Current, I_{out1}, I_{out2}	I_O		+50/– 50	mA
Operating Free-Air Temperature	T_C	– 20	85	°C

Electrical Characteristics, V_{DD} = 3.3V (Unless Otherwise Specified) (See Note 1)

Oscillator

Parameter		Test Condition	Min	Typ	Max	Unit
Frequency	f_{OSC}	C_{OSC} = 220pF, R_{OSC} = 5.6kΩ	320	400	480	kHz
Frequency Changes with V_{DD}	$f_{\Delta V}$	V_{DD} = 2.6V to 6.0V, T_C = 25°C C_{OSC} = 220pF, R_{OSC} = 5.6kΩ	-	1	-	%

Under-Voltage Protection

Parameter		Test Condition	Min	Typ	Max	Unit
Upper Threshold Voltage	V_{UPH}	T_C = 25°C	1.81	2.03	2.25	V
Lower Threshold Voltage	V_{UPL}	T_C = 25°C	1.57	1.79	2.01	V
Hysteresis (V_{UPH} – V_{UPL})	V_{HYS}	T_C = 25°C	-	0.24	-	V

Short Circuit Protection Control

Parameter		Test Condition	Min	Typ	Max	Unit
Input Threshold Voltage	V_{r2}	CH2	1.81	1.29	1.40	V
Input Threshold Voltage	V_{r1}	CH1	0.30	0.37	0.44	V
Short-Circuit Detect Threshold Voltage	V_{tscd}		0.76	0.85	0.94	V
SCP Terminal Source Current	I_{SCP}		– 3.8	– 2.6	– 1.4	µA
Stand-by Voltage	V_{STB}			50	100	mV
Latch Voltage	V_{LT}			30	100	mV

Shutdown Control

Parameter		Test Condition	Min	Typ	Max	Unit
Shutdown Enable Voltage	V_{SE}	T_C = 25°C	-	-	0.5	V
Shutdown Release Voltage	V_{SR}	T_C = 25°C	2.0	-	-	V

Note 1: Typical values of all parameters are specified at T_C =25°C.

Electrical Characteristics, V_{DD} = 3.3V (Unless Otherwise Specified) (See Note 1) (Cont.)

Reference Voltage

Parameter		Test Conditions	Min	Typ	Max	Unit
Internal Reference Voltage	V_{REFi}	$I_{REF} = -1mA$, $T_C = 25^oC$	0.622	0.641	0.660	V
Reference Voltage	V_{REF}	$I_{REF} = -1mA$, $T_C = 25^oC$	1.280	1.293	1.306	
Input Voltage Regulation	V_{RI}	$I_{REF} = -1mA$, V_{DD} = 2.6V to 6.0V	-	1	10	mV
Output Regulation	V_{RO}	I_{REF} = –0.1mA to –1mA	-	1	6	mV

EA (Error Amplifier)

Parameter		Test Condition	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	CH1,CH2, Unity Gain	-	-	6	mV
Input Bias Current	I_{IB}	CH1, CH2	-	±15	±100	nA
Input Voltage Range	V_{IR}	CH1, CH2	0.5	-	1.5	V
Open-Loop Voltage Amplification	A_{VO}		70	85	-	dB
Output Voltage Swing	V_{OS+}		1.7	2.0	-	V
	V_{OS-}		-	0.2	0.4	
Output Sink Current	I_{OS+}	OE=0.65V	3	10	-	mA
Output Source Current	I_{OS-}	OE=0.65V	-	– 65	– 45	µA
Common-Mode Rejection Ratio	CMRR		60	80	-	dB

PRDB (Power Good Protection)

Parameter		Test Condition	Min	Typ	Max	Unit
Low Level Output Voltage	V_{dbl}	Pull-High $R_{20} = 100k\Omega$	-	0.2	0.4	V

Electrical Characteristics, V_{DD} = 3.3V (Unless Otherwise Specified) (See Note 1) (Cont.)

Dead Time Control & PWM

Parameter		Test Condition	Min	Typ	Max	Unit
Input Bias Current	I_{IB}	V_{DTC} = 1.0V	-	0.1	1.0	µA
Input Threshold Voltage (DTC1)	V_{1d0}	Duty = 0%, f_{OSC} = 10kHz	0.92	1.00	1.08	V
	V_{1d100}	Duty = 100%, f_{OSC} = 10kHz	0.48	0.56	0.64	
Input Threshold Voltage (DTC2)	V_{2d0}	Duty = 0%, f_{OSC} = 10kHz	0.48	0.56	0.64	V
	V_{2d100}	Duty = 100%, f_{OSC} = 10kHz	0.92	1.00	1.08	
Latch Input Voltage (DTC1)	V_{1DTC}	I_{DTC} = 20µA	1.15	1.20	-	V
Latch Input Voltage (DTC2)	V_{2DTC}	I_{DTC} = 50µA	-	0.2	0.4	V
Latch Mode Source Current (DTC1)	I_{1DTC}	DTC1=1.08V	-	– 45	– 30	µA
Latch Mode Source Current (DTC2)	I_{2DTC}	DTC2=0.48V	150	200	-	µA

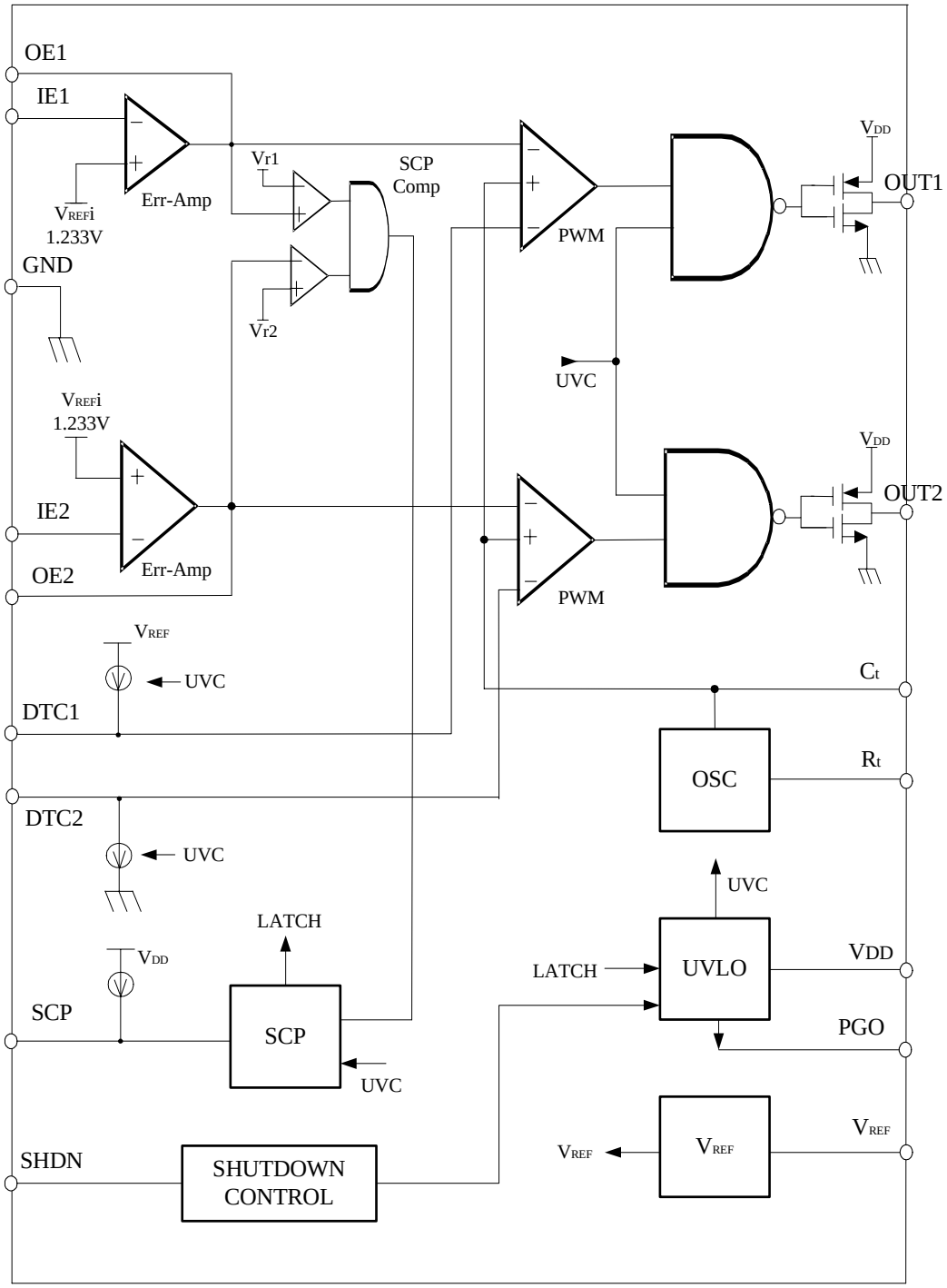
Output Stage

Parameter		Test Condition	Min	Typ	Max	Unit
High-Level Output Voltage	V_{OH}	I_O = – 50 mA	1.8	2.2	-	V
Low-Level Output Voltage	V_{OL}	I_O =+50mA	-	0.8	1.2	V
Rise Time	t_{RISE}	C_L =1,000pF	-	100	-	ns
Fail Time	t_{FALL}	C_L =1,000pF	-	100	-	ns
Leakage Current	I_{LEAK}	V_O =6.0V	-	-	5	µA
Capacitance at the Output Pin	C_L					

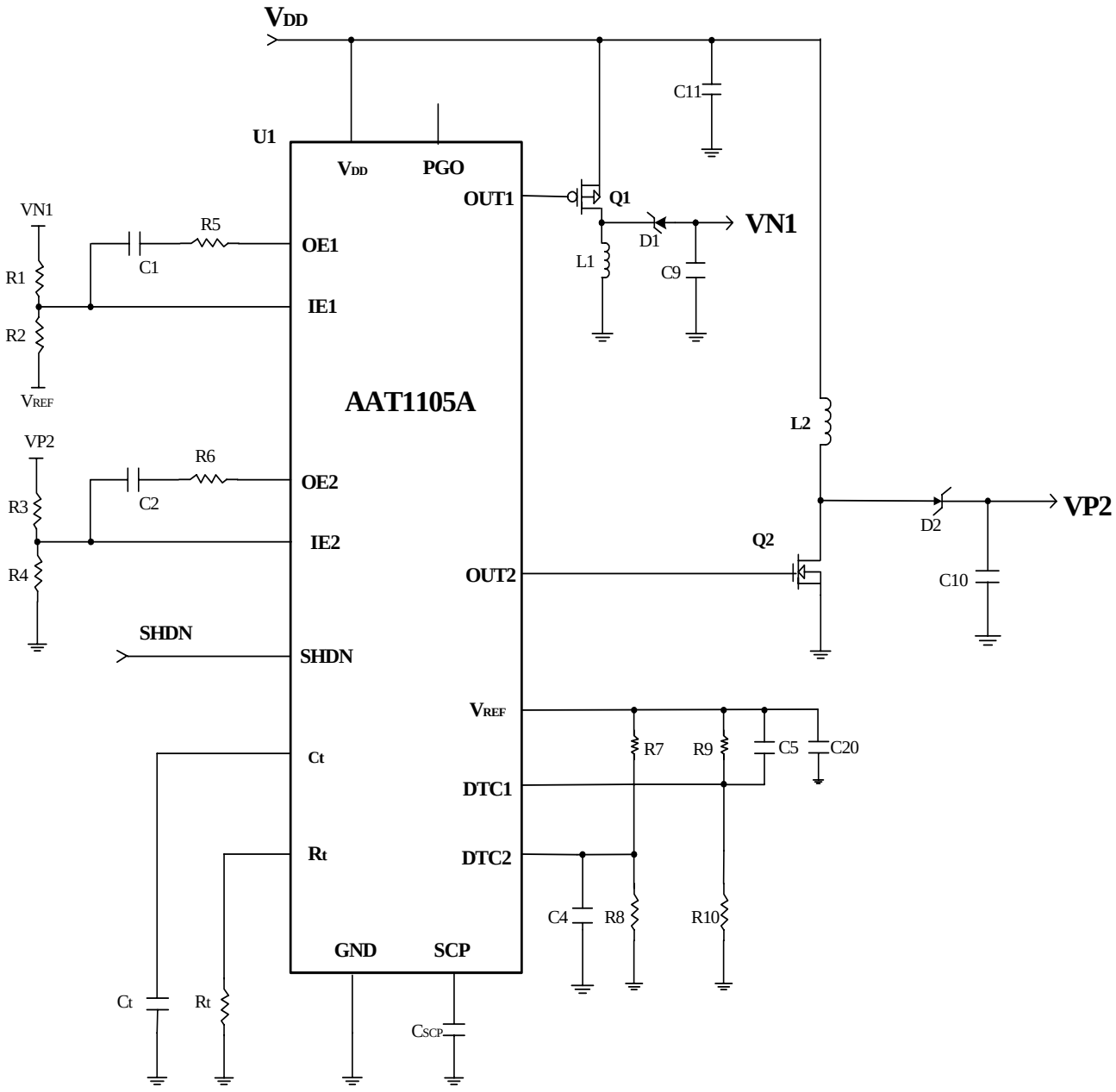
Operating Current

Parameter		Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD-OFF}	Output "OFF" State	-	1.8	-	mA
	I_{DD-ON}	R_{OSC} = 10kΩ	-	2.0	-	mA

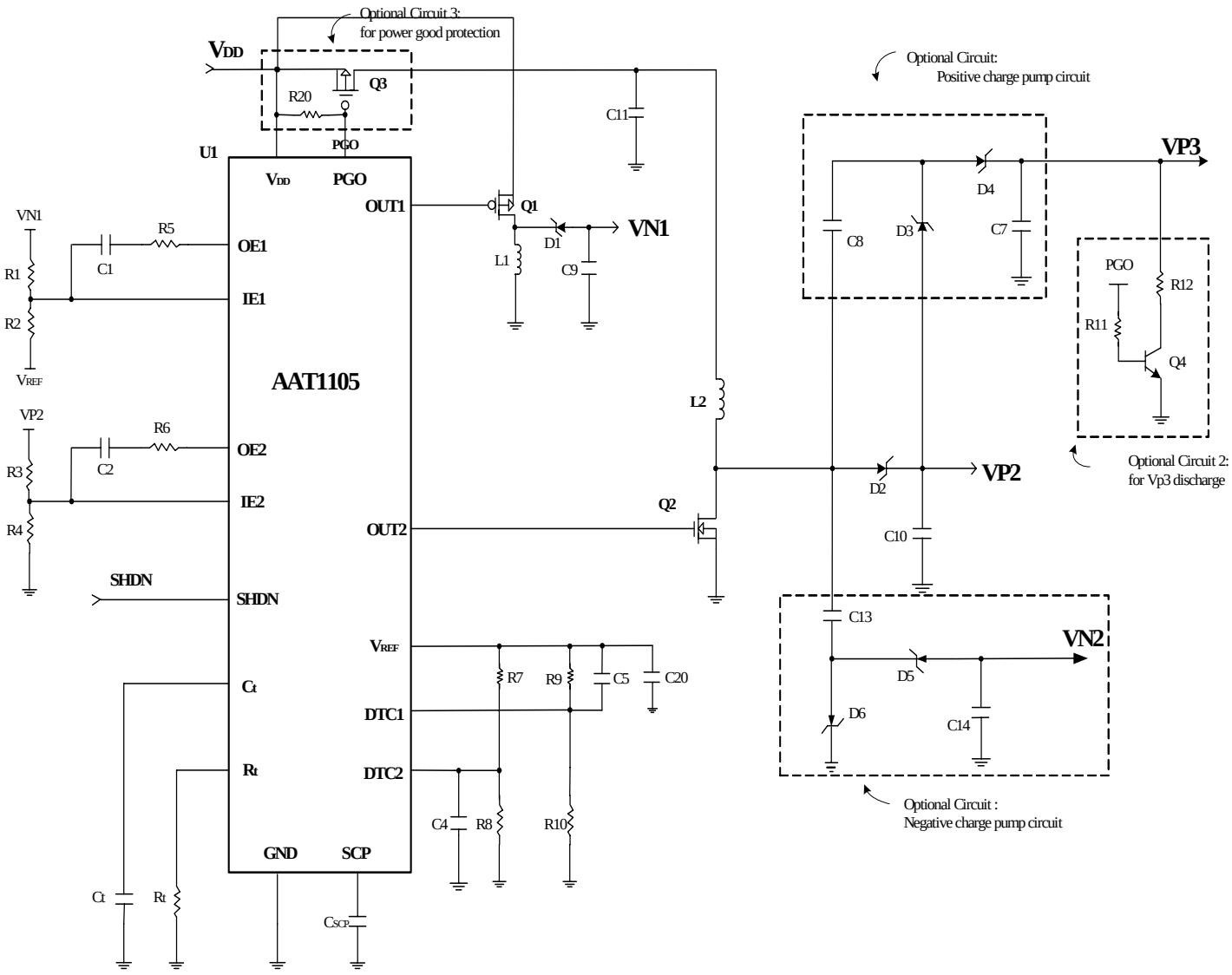
Block Diagram



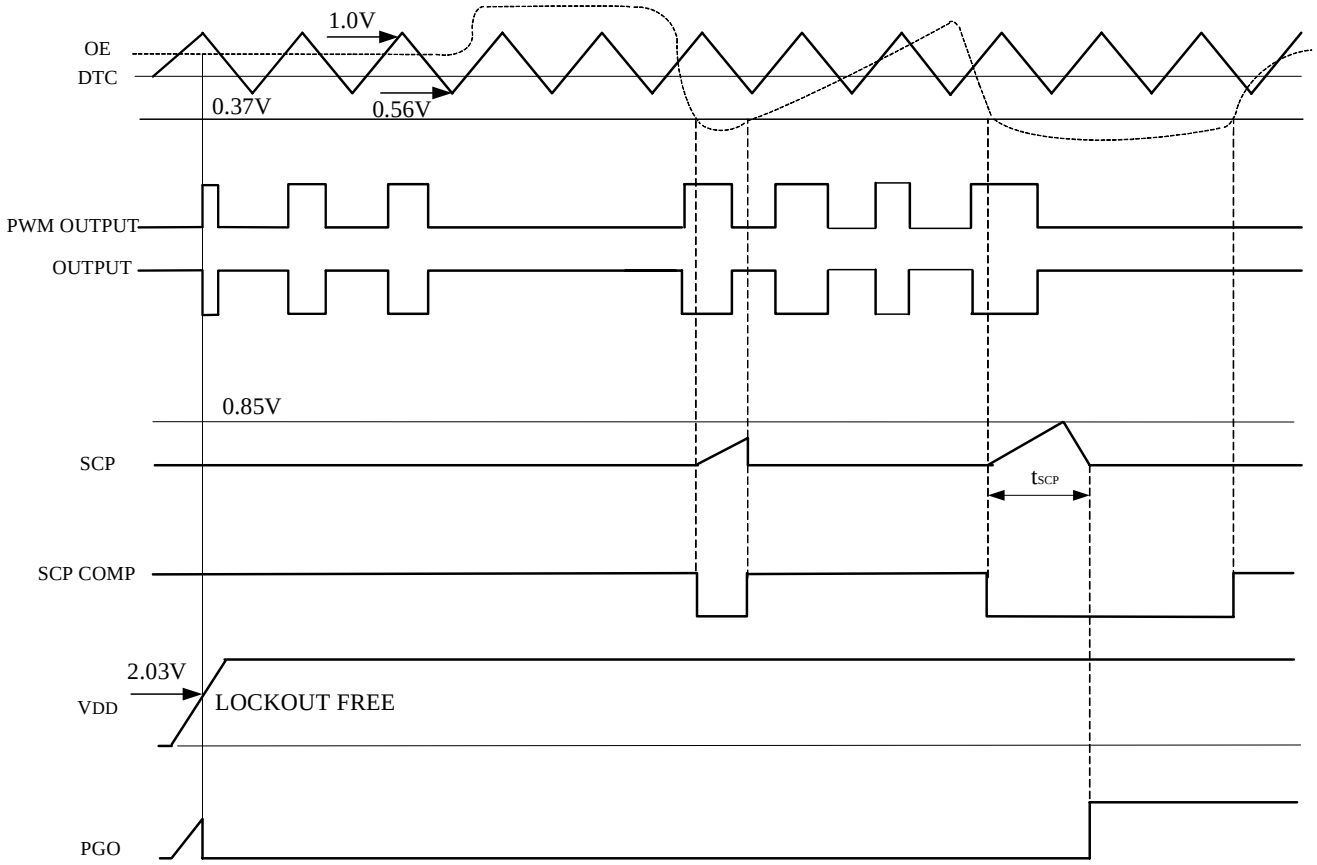
Application Circuit 1



Application Circuit 2

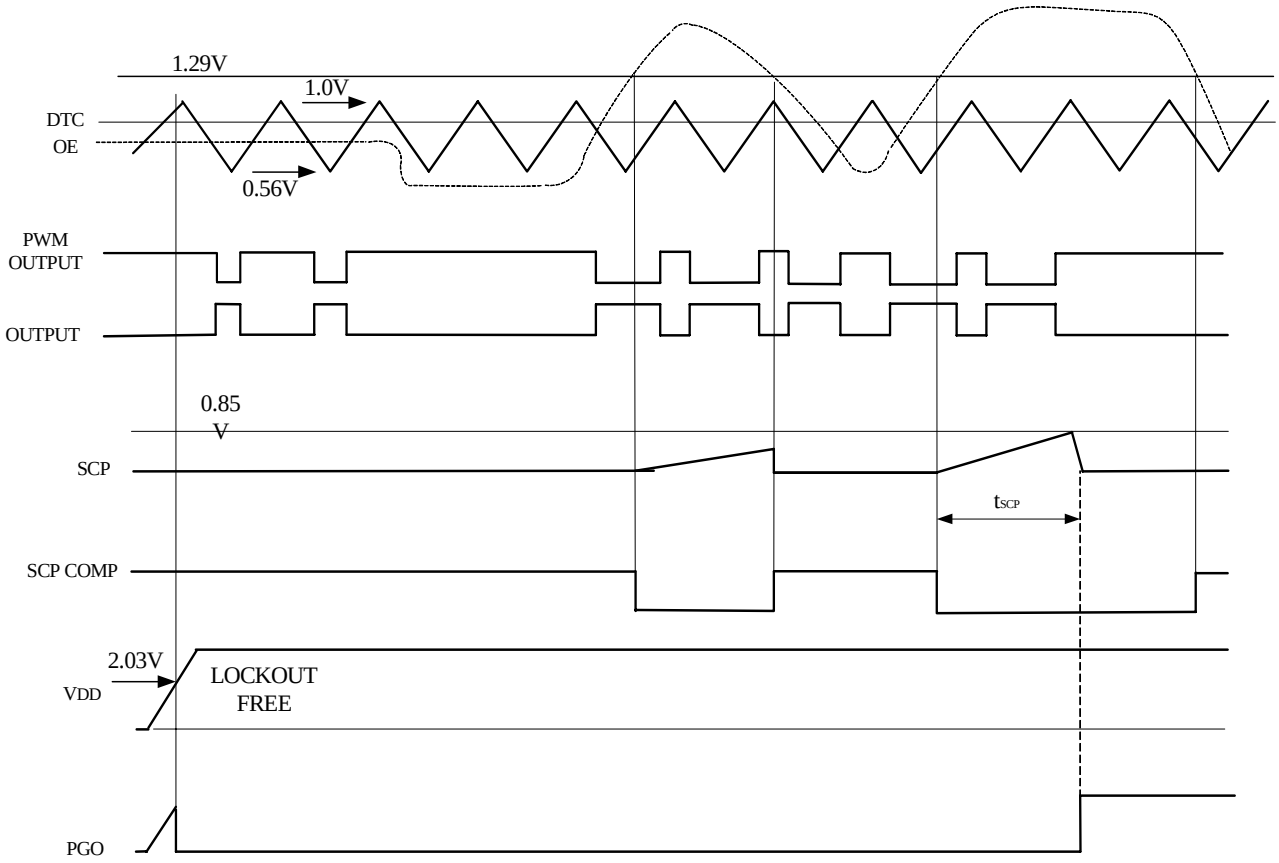


Buck-Boost（Inverting） Timing Chart （CH1）



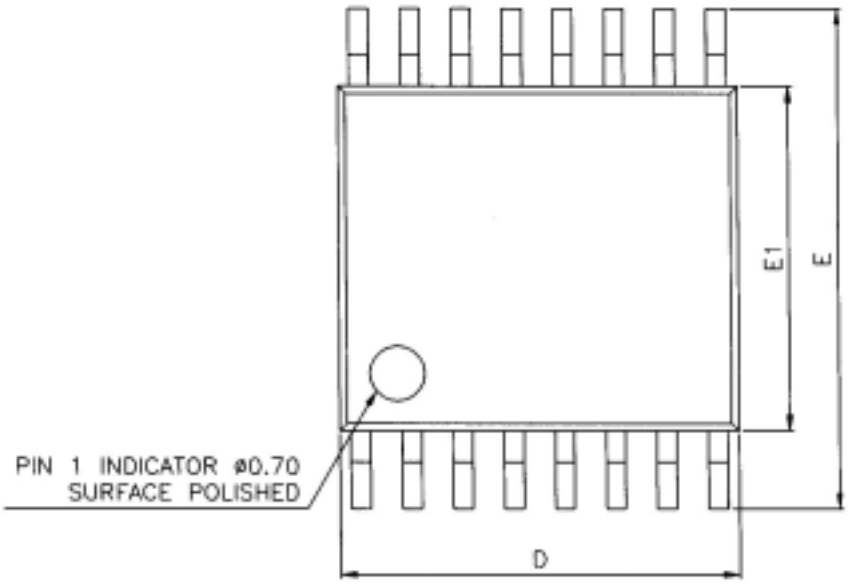
Note: $t_{SCP} \cong \frac{C_{SCP} V_{r2}}{I_{SCP}}$

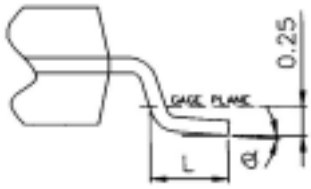
Boost （Step-up）Timing Chart （CH-2）

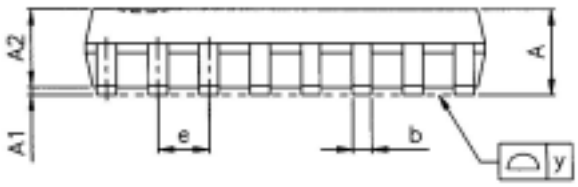


Note: $t_{SCP} \cong \frac{C_{SCP} V_{r2}}{I_{SCP}}$

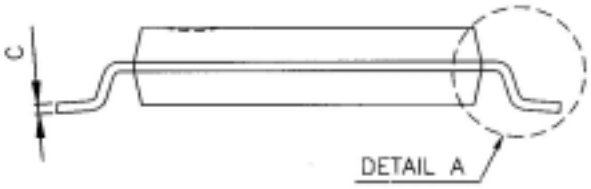
Package Dimension
16-Pin TSSOP







Package Dimension (Cont.)

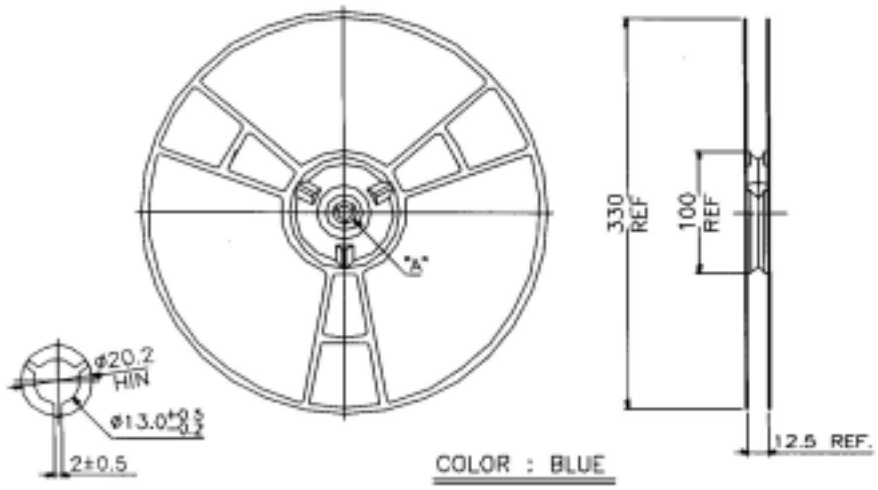


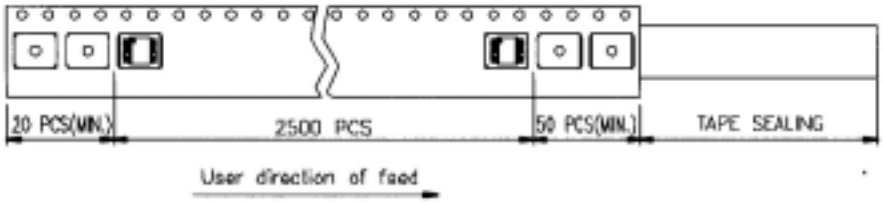
SYMBOLS	DIMENSIONS IN MILLIMETERS			DEMINSIONS IN INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	1.05	1.10	1.20	0.041	0.043	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	------	1.00	1.05	------	0.039	0.041
b	0.20	0.25	0.28	0.008	0.010	0.011
C	------	0.127	------	------	0.005	------
D	4.900	5.075	5.100	0.1930	0.1998	0.2000
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.170	0.173	0.177
e	------	0.65	------	------	0.026	------
L	0.50	0.60	0.70	0.020	0.024	0.028
y	------	------	0.076	------	------	0.003
θ	0°	4°	8°	0°	4°	8°

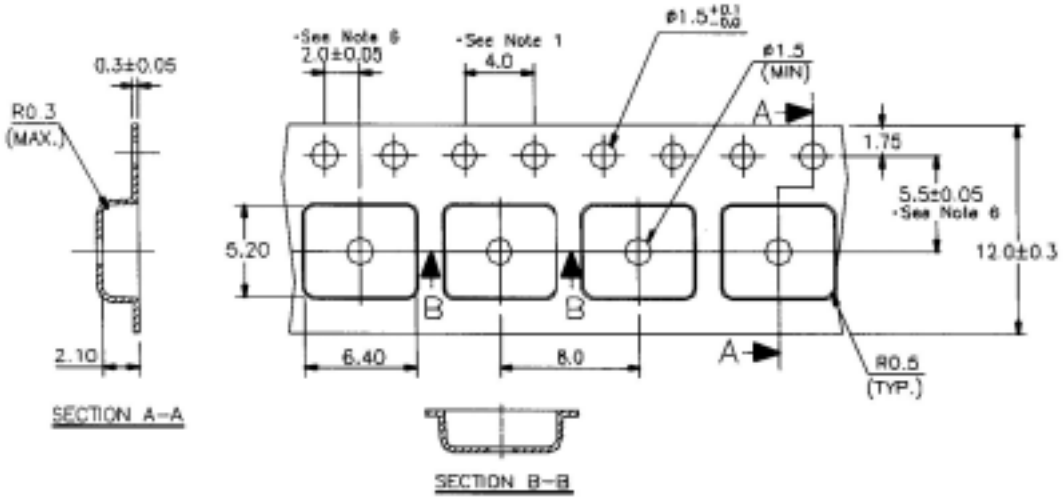
NOTE:

1. CONTROLLING DIMENSION: MILLIMETERS
2. LEAD FRAME MATERIAL: OLIN C7025/EFTEC 64T
3. DIMENSION “D” DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006” [0.15 MILLIMETERS] PER END. DIMENSION “E1” DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010” [0.25 MILLIMETERS] PER SIDE.
4. DIMENSION “b” DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003” [0.08 MILLIMETERS] TOTAL IN EXCESS OF THE “b” DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028” [0.07 MILLIMETERS].
5. TOLERANCE: ±0.010 [0.25 MILLIMETERS] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT: JEDEC SPEC MO-153.

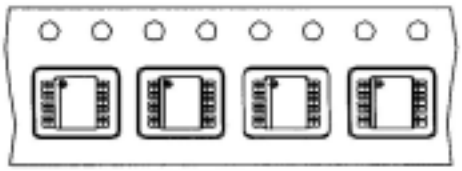
Tape and Reel







Tape and Reel (Cont.)



TSSOP 14L / 16L

NOTE:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2 MILLIMETERS.
2. CAMBER NOT TO EXCEED 1 MILLIMETER IN 100 MILLIMETERS.
3. MATERIAL: ANTI-STATIC BLACK ADVANTEK POLYSTYRENE.
4. A_0 AND B_0 MEASURED ON A PLANE 0.3 MILLIMETERS ABOVE THE BOTTOM OF THE POCKET.
5. K_0 MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER.
6. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.

Part Marking

TSSOP16 Top Marking

AAT1105A XXXXXX

TSSOP16 Back Marking

YYWW

Ordering Information