AAT2513
Dual 600mA Step-Down Converter with Synchronization

SystemPower™

General Description

The AAT2513 is a high efficiency dual synchronous step-down converter for applications where power efficiency, thermal performance and solution size are critical. Input voltage ranges from 2.7V to 5.5V, making it ideal for systems powered by single-cell lithium-ion/polymer batteries.

Each converter is capable of 600mA output current and has its own enable pin. Efficiency of the converters is optimized over full load range. Total no load quiescent current is 60µA, allowing high efficiency even under light load conditions.

The integrated power switches are controlled by pulse width modulation (PWM) with a 1.7MHz typical switching frequency at full load, which minimizes the size of external components. Fixed frequency, low noise operation can be forced by a logic signal on the MODE pin. Furthermore, an external clock can be used to synchronize the switching frequency of both converters.

A phase shift pin (PS) is available to operate the two converters 180° out of phase at heavy load to achieve low input ripple.

The AAT2513 is available in a Pb-free, thermally enhanced 16-pin QFN33 package and is specified for operation over the -40°C to +85°C temperature range.

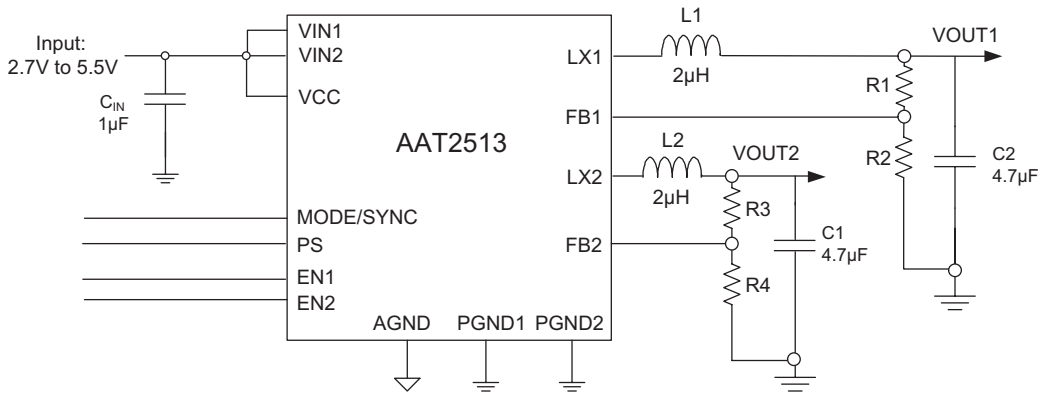
Features

- V_{IN} Range: 2.7V to 5.5V
- Output Current:
  - — Channel 1: 600mA
  - — Channel 2: 600mA
- 96% Efficient Step-Down Converter
- Low No Load Quiescent Current
  - — 60µA Total for Both Converters
- Integrated Power Switches
- 100% Duty Cycle
- 1.7MHz Switching Frequency
- Optional Fixed Frequency or External SYNC
- Logic Selectable 180° Phase Shift Between the Two Converters
- Current Limit Protection
- Automatic Soft-Start
- Over-Temperature Protection
- QFN33-16 Package
- -40°C to +85°C Temperature Range

Applications

- Cellular Phones / Smart Phones
- Digital Cameras
- Handheld Instruments
- Micro Hard Disc Drives
- Microprocessor / DSP Core / IO Power
- PDAs and Handheld Computers

Typical Application

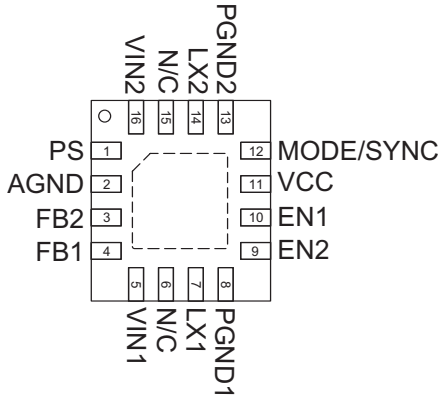


Pin Descriptions

Pin #	Symbol	Function
1	PS	Phase shift pin. Logic high enables the PS feature which forces the two converters to operate 180° out of phase when both are in forced PWM mode.
2	AGND	Analog ground. Return the feedback resistive divider to this ground. See section on PCB layout guidelines and evaluation board layout diagram.
4, 3	FB1, FB2	Feedback input pins. An external resistive divider ties to each and programs the respective output voltage to the desired value.
5, 16	VIN1, VIN2	Input supply voltage pins. Must be closely decoupled to the respective PGND.
6, 15	N/C	Not connected
7, 14	LX1, LX2	Output switching nodes that connect to the respective output inductor.
8, 13	PGND1, PGND2	Main power ground return. Connect to the input and output capacitor return. See section on PCB layout guidelines and evaluation board layout diagram.
10, 9	EN1, EN2	Converter enable input pins. A logic high enables the converter channel. A logic low forces the channel into shutdown mode, reducing the channel supply current to less than 1µA. This pin should not be left floating. When not actively controlled, this pin can be tied directly to VIN and/or VCC.
11	VCC	Control circuit power supply. Connect to the higher voltage of VIN1 or VIN2.
12	MODE/SYNC	Logic low enables automatic light load mode for optimized efficiency throughout the entire load range. Logic high forces low noise PWM operation under all operating conditions. Connect to an external clock for synchronization (PWM only).
EP		Exposed paddle (bottom). Use properly sized vias for thermal coupling to the ground plane. See section on PCB layout guidelines.

Pin Configuration

QFN33-16
(Top View)



Absolute Maximum Ratings[1]

T_A = 25°C unless otherwise noted.

Symbol	Description	Value	Units
VIN1/2	Input Voltage	-0.3 to 6.0	V
GND, PGND1/2	Ground Pins	-0.3 to +0.3	V
EN1/2, SYNC, LX1/2, FB1/2, PS	Maximum Rating	-0.3 to V_{CC} + 0.3	V
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance	50	°C/W
P_D	Maximum Power Dissipation	2	W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Electrical Characteristics[1]

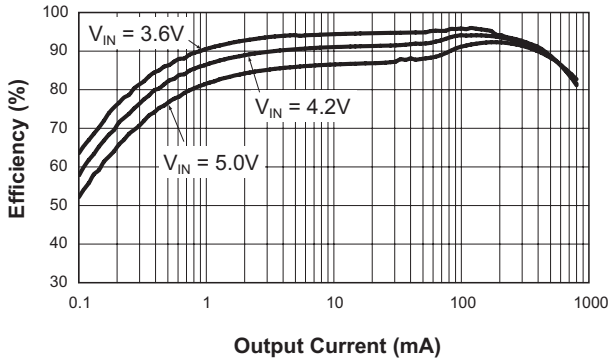
V_{IN} = V_{CC} = 3.6V, T_A = -40°C to +85°C, unless noted otherwise. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Power Supply						
V_{CC}, V_{IN1}, V_{IN2}	Input Voltage		2.7		5.5	V
UVLO	Under-Voltage Lockout	V_{CC} Rising			2.7	V
		V_{CC} Falling		2.35		
I_Q	Quiescent Current	V_{EN1} = V_{EN2} = V_{CC}, No Load		60	120	µA
I_{SHDN}	Shutdown Current	EN1 = EN2 = GND			1.0	µA
Each Converter						
V_{FB}	Feedback Voltage Tolerance	I_{OUT} = 0 to 600mA, V_{IN} = 2.9 to 5.5V	-3.0		-3.0	%
		I_{OUT} = 0 to 450mA, V_{IN} = 2.7 to 5.5V				
V_{OUT}	Output Voltage Range		0.6		V_{IN}	V
I_{LX_LEAK}	LX Reverse Leakage Current (Fixed)	V_{IN} Open, V_{LX} = 5.5V, EN = GND			1.0	µA
I_{LX_LEAK}	LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 0 to V_{IN}			1.0	µA
I_{FB}	Feedback Leakage	V_{FB} = 1.0V			0.2	µA
I_{LIM}	P-Channel Current Limit	Each Converter		1.0		A
$R_{DS(ON)H}$	High Side Switch On Resistance			0.45		Ω
$R_{DS(ON)L}$	Low Side Switch On Resistance			0.40		Ω
$\Delta V_{OUT}/V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{LOAD} = 0 to 600 mA		0.002		%/mA
$\Delta V_{OUT}/V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 2.7 to 5.5V, I_{LOAD} = 100 mA		0.125		%/V
V_{FB}	Feedback Threshold Voltage Accuracy	No Load, T_A = 25°C	0.591	0.600	0.609	V
F_{OSC}	Oscillator Frequency			1.7		MHz
T_S	Start-Up Time	From Enable to Output Regulation; Both Channels		150		µs
Logic						
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
V_{IL}	EN, MODE/SYNC, PS Logic Low Threshold				0.6	V
V_{IH}	EN, MODE/SYNC, PS Logic High Threshold		1.4			V
I_{EN}, $I_{MODE/SYNC}$, I_{PS}	Logic Input Current	V_{IN} = V_{FB} = 5.5V	-1.0		1.0	µA

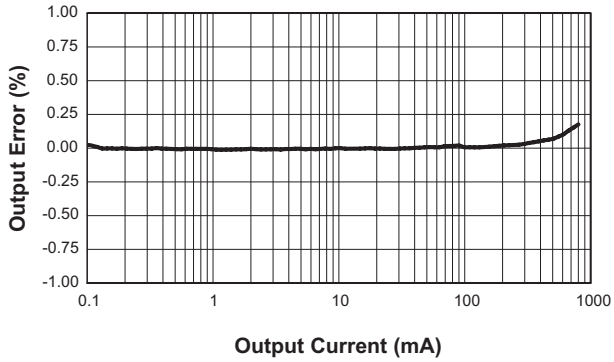
1. The AAT2513 guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics

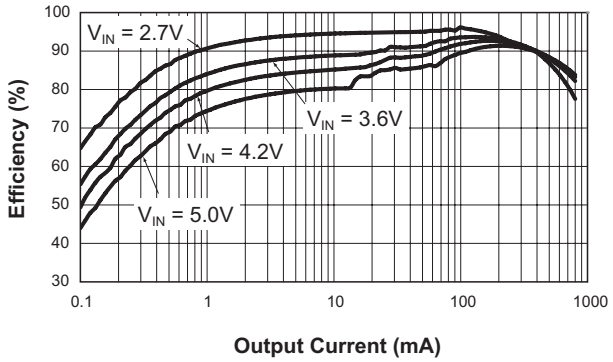
Efficiency vs. Load
(V_{OUT} = 3.3V; L = 4.7µH; LL Mode)



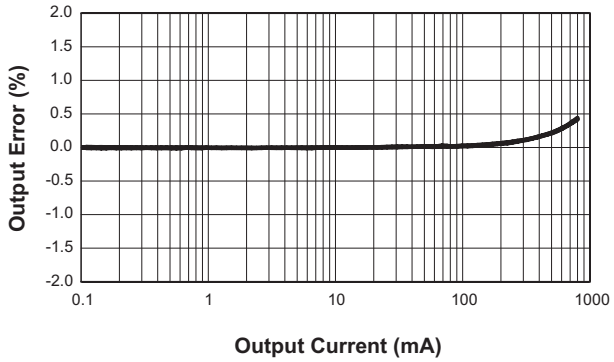
DC Regulation
(V_{IN} = 5.0V; V_{OUT} = 3.3V; L = 4.7µH; LL Mode)



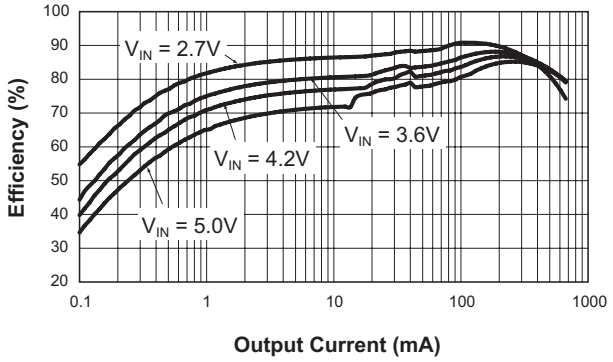
Efficiency vs. Load
(V_{OUT} = 2.5V; L = 3.3µH; LL Mode)



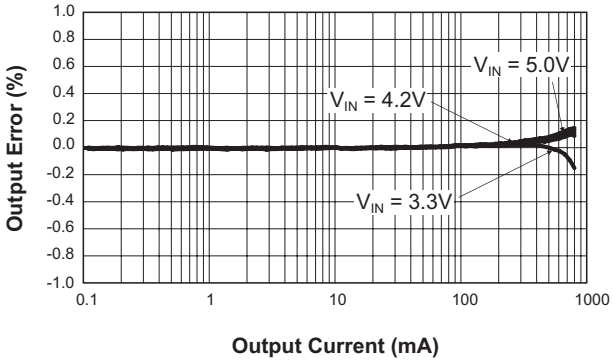
DC Regulation
(V_{IN} = 3.3V to 5.5V; V_{OUT} = 2.5V; L = 3.3µH; LL Mode)



Efficiency vs. Load
(V_{OUT} = 1.8V; L = 2.2µH; LL Mode)

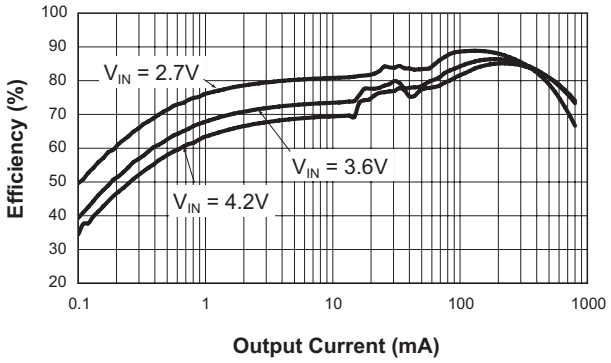


DC Regulation
(V_{OUT} = 1.8V; L = 2.2µH; LL Mode)

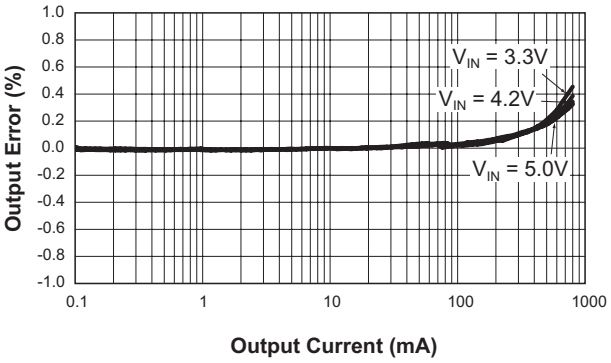


Electrical Characteristics

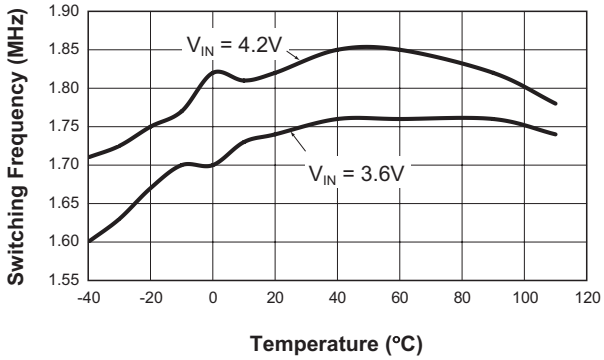
Efficiency vs. Load
(V_{OUT} = 1.5V; L = 2.2µH; LL Mode)



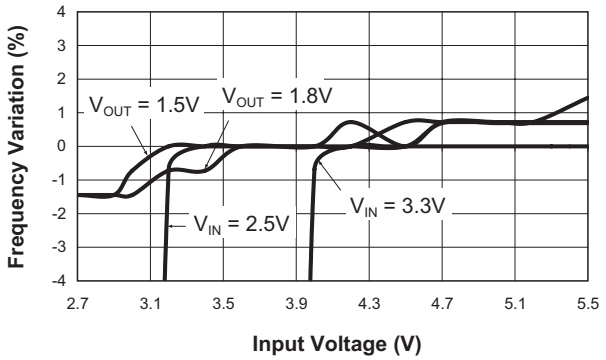
DC Regulation
(V_{OUT} = 1.5V; L = 2.2µH; LL Mode)



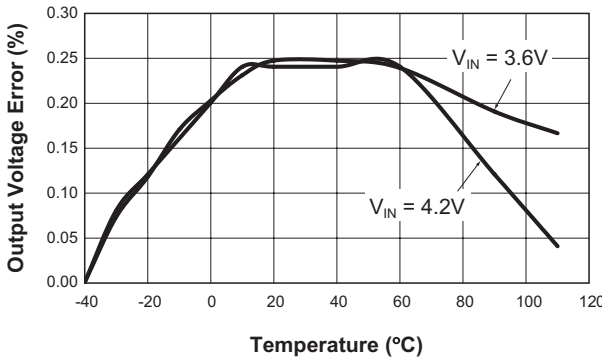
Switching Frequency vs. Temperature



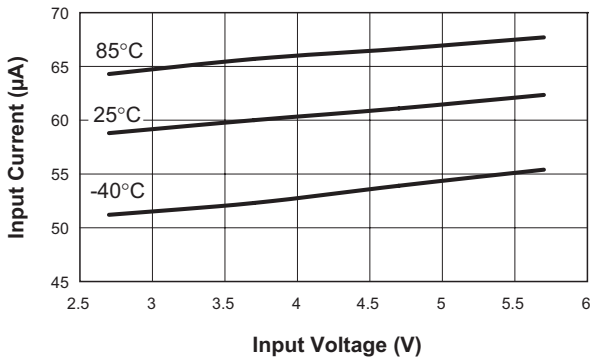
Switching Frequency vs. Input Voltage
(I_{OUT} = 600mA; 25°C)



Output Voltage Error Vs. Temperature
(V_{OUT} = 2.5V; I_{OUT} = 600mA)

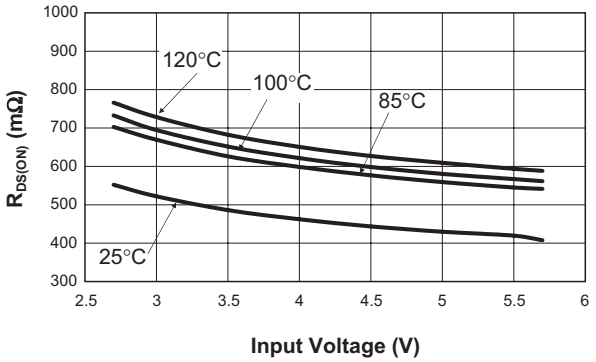


No Load Quiescent Current vs. Input Voltage

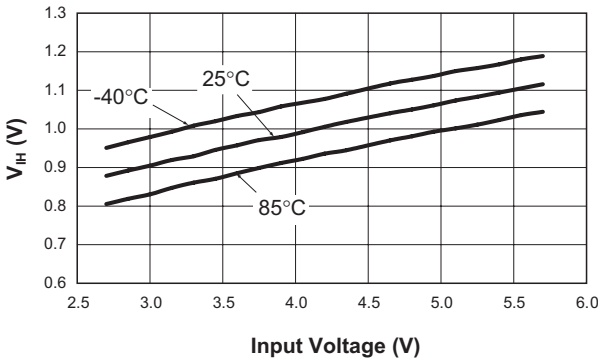


Electrical Characteristics

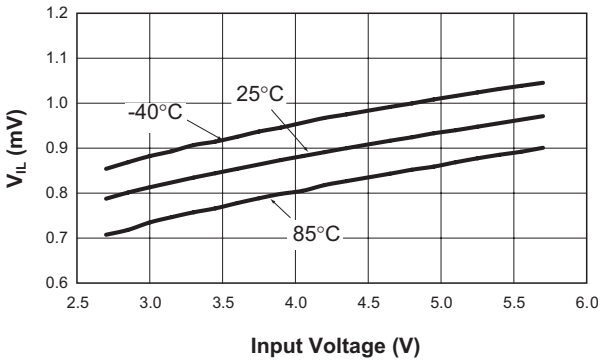
P-Channel $R_{DS(ON)}$ vs. Input Voltage



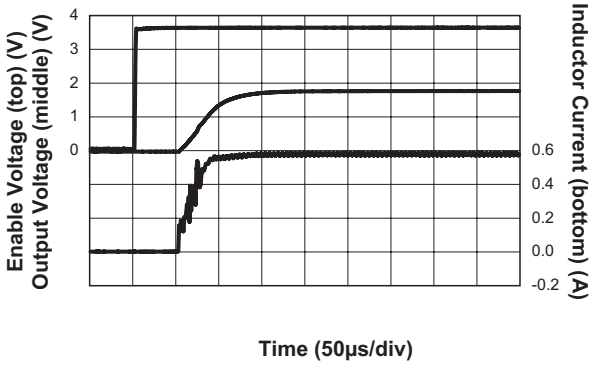
V_{IH} vs. Input Voltage



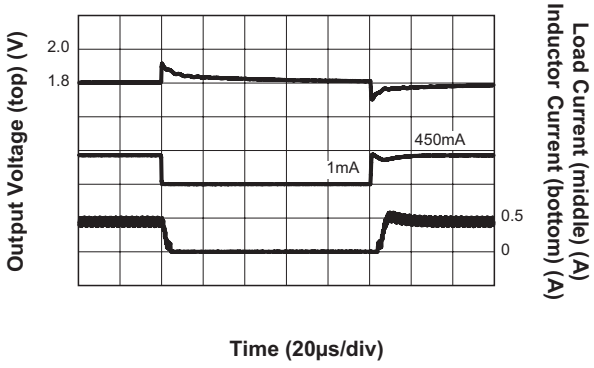
V_{IL} vs. Input Voltage



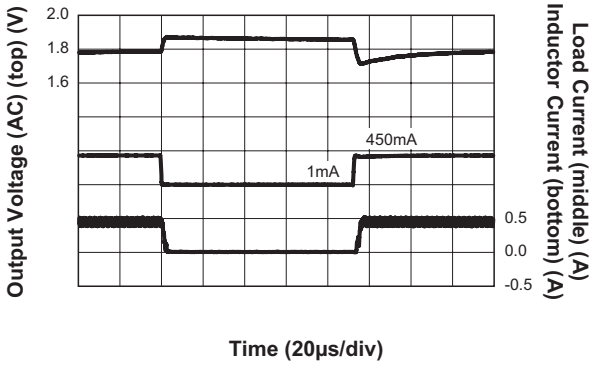
Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 600mA)



Load Transient
(1mA to 450mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 4.7µF)

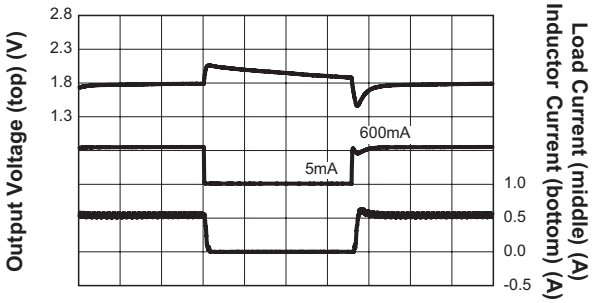


Load Transient
(1mA to 450mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 10µF; C_{FF} = 100pF)



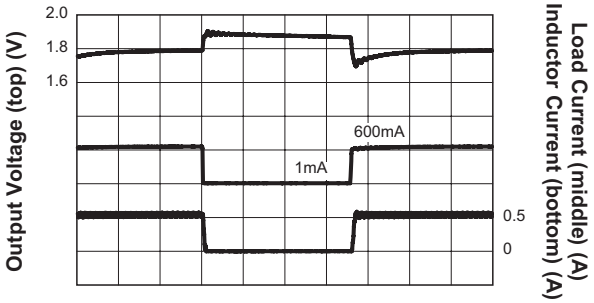
Electrical Characteristics

Load Transient
(5mA to 600mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 4.7µF)



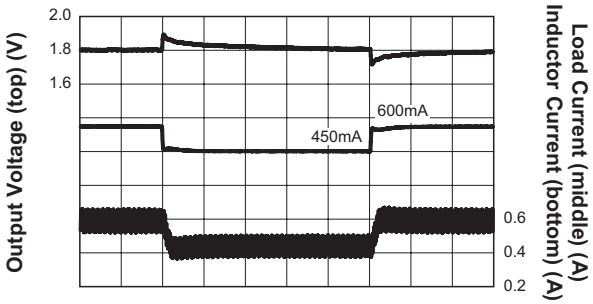
Time (40µs/div)

Load Transient
(1mA to 600mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 10µF; C_{FF} = 100pF)



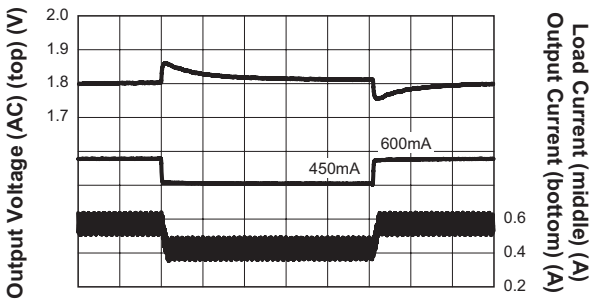
Time (40µs/div)

Load Transient
(450mA to 600mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 4.7µF)



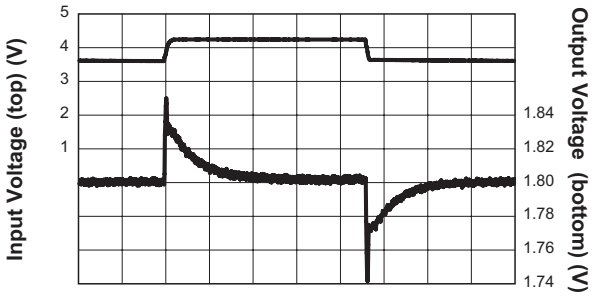
Time (20µs/div)

Load Transient
(450mA to 600mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 10µF; C_{FF} = 100pF



Time (20µs/div)

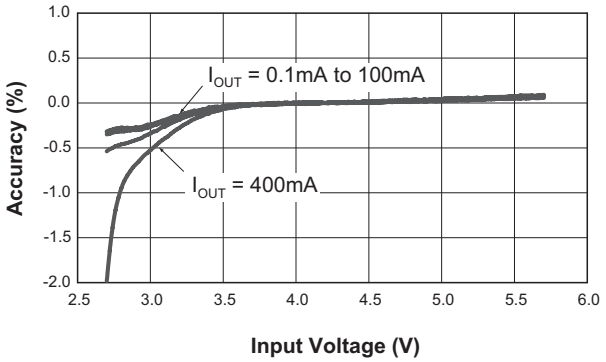
Line Transient
(V_{IN} = 3.6V to 4.2V; V_{OUT} = 1.8V; I_{OUT} = 600mA; C_{OUT} = 4.7µF)



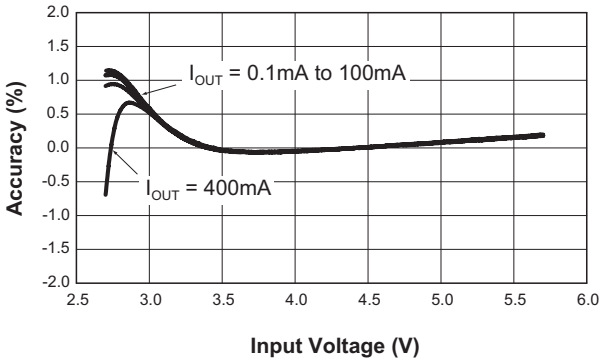
Time (40µs/div)

Electrical Characteristics

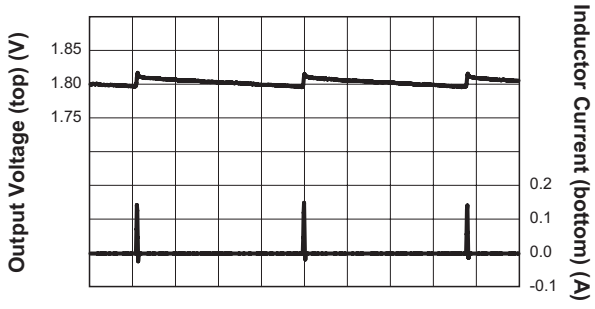
Line Regulation
(V_{OUT} = 1.8V; L = 2.2µH)



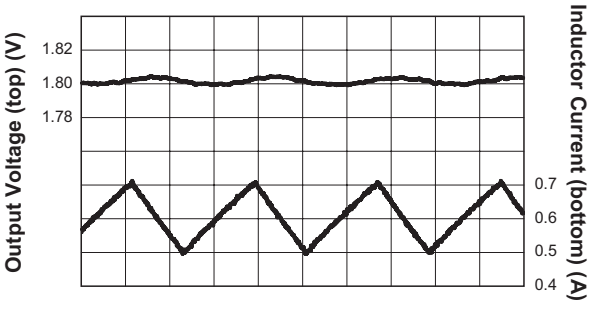
Line Regulation
(V_{OUT} = 1.5V; L = 2.2µH)



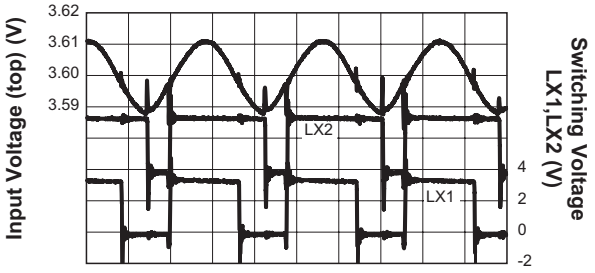
Output Voltage Ripple
(V_{OUT} = 1.8V; V_{IN} = 3.6V; Load = 1mA)



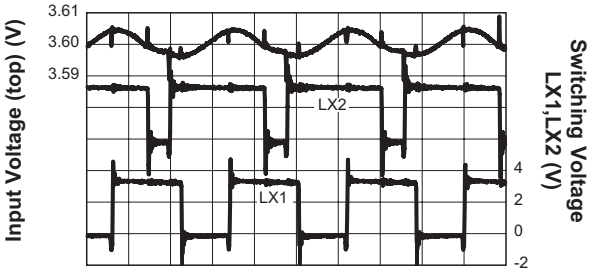
Output Voltage Ripple
(V_{OUT} = 1.8V; V_{IN} = 3.6V; Load = 600mA)



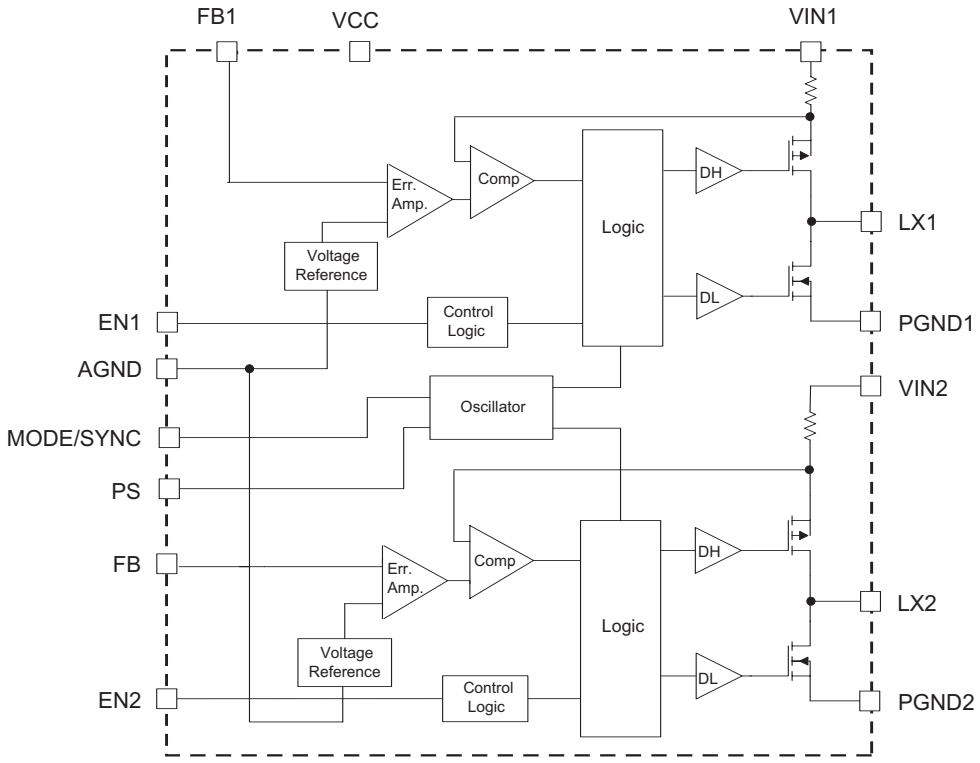
Input Ripple
(C_{IN} = 2 x 10µF; V_{IN} = 3.6V; V_{OUT1} = 1.8V; V_{OUT2} = 2.5V; $I_{OUT1,2}$ = 600mA; 0° Phase Shift; PS = Low)



Input Ripple
(C_{IN} = 2 x 10µF; V_{IN} = 3.6V; V_{OUT1} = 1.8V; V_{OUT2} = 2.5V; $I_{OUT1,2}$ = 600mA; 180° Phase Shift)



Functional Block Diagram



Functional Description

The AAT2513 is a peak current mode pulse width modulated (PWM) converter with internal compensation. Each channel has independent input, enable, feedback, and ground pins with a 1.7MHz clock. Both converters operate in either a fixed frequency (PWM) mode or a more efficient light load (LL) mode. A phase shift pin programs the converters to operate in phase or 180° out of phase. The converter can also be synchronized to an external clock during PWM operation.

The input voltage range is 2.7V to 5.5V. An external resistive divider as shown in Figure 1 programs the output voltage up to the input voltage. The converter MOSFET power stage is sized for 600mA load capability with up to 96% efficiency. Light load efficiency is up to 90% at a 1mA load.

Soft Start / Enable

The AAT2513 soft start control prevents output voltage overshoot and limits inrush current when either the input power or the enable input is applied. When pulled low, the enable input forces the converter into a low power non-switching state with a bias current of less than 1µA.

Low Dropout Operation

For conditions where the input voltage drops to the output voltage level, the converter duty cycle increases to 100%. As the converter approaches the 100% duty cycle, the minimum off time initially forces the high side on time to exceed the 1.7MHz clock cycle and reduce the effective switching frequency. Once the input drops below the level where the converter can regulate the output, the high side P-channel MOSFET is enabled continuously for 100% duty cycle. At 100% duty cycle the output voltage tracks the input voltage minus the I*R drop of the high side P-channel MOSFET.

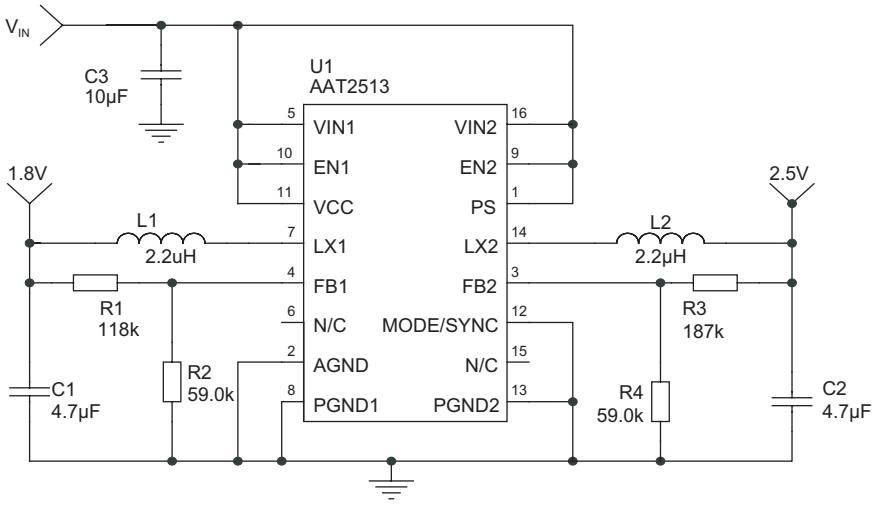


Figure 1: AAT2513 Typical Schematic.

Low Supply UVLO

Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

Fault Protection

For overload conditions, the peak inductor current is limited. Thermal protection disables the converter when the internal dissipation or ambient temperature becomes excessive. The over-temperature threshold for the junction temperature is 140°C with 15°C of hysteresis.

PWM/LL Operation

For fixed frequency, with minimum ripple under light load conditions, the MODE/SYNC pin should be tied to a logic high. For more efficient operation under light load conditions the MODE/SYNC pin should be tied to a logic low level.

Clock Phase and Frequency

A logic high on the PS pin while in PWM mode forces both converters to operate 180° out of phase thus reducing the input ripple by roughly half. A logic low on the PS pin synchronizes both converters in phase.

Applications Information

Inductor Selection

The step down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the adjustable and low voltage fixed versions of the AAT2513 is 0.6A/µsec. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.8V output and 2.2µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{2.2\mu H} = 0.6\,\frac{A}{\mu sec}$$

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75V \cdot V_O}{0.6\,\frac{A}{\mu s}} \approx 1.2\,\frac{\mu s}{A} \cdot V_O$$

$$= 1.2\,\frac{\mu s}{A}\,2.5V = 3.1\mu H$$

In this case a standard 3.3µH value is selected.

Table 1 displays the suggested inductor values for the AAT2513.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the inductor's saturation characteristics. The inductor should not show any appreciable saturation under all normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 2.2uH CDRH2D11 series inductor selected from Sumida has a 98mΩ DCR and a 1.27A DC current rating. At full load the inductor DC loss is 35mW which corresponds to a 3.2% loss in efficiency for a 600mA, 1.8V output.

Input Capacitor

A key feature of the AAT2513 is that the fundamental switching frequency ripple at the input can be reduced by operating the two converters 180° out of phase. This reduces the input ripple by roughly half, reducing the required input capacitance. An X5R ceramic input capacitor as small as 1µF is often sufficient. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

This equation provides an estimate for the input capacitor required for a single channel.

The equation below solves for the input capacitor size for both channels. It makes the worst case assumption that both converters are operating at 50% duty cycle with in phase synchronization.

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{O1} + I_{O2}} - ESR\right) \cdot 4 \cdot F_S}$$

Because the AAT2513 channels will generally operate at different duty cycles the actual ripple will vary and be less than the ripple (V_{PP}) used to solve for the input capacitor in the above equation.

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF 6.3V X5R ceramic capacitor with 5V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_{O1} \cdot \left(\sqrt{\frac{V_{O1}}{V_{IN}} \cdot \left(1 - \frac{V_{O1}}{V_{IN}}\right)}\right) + I_{O2} \cdot \left(\sqrt{\frac{V_{O2}}{V_{IN}} \cdot \left(1 - \frac{V_{O2}}{V_{IN}}\right)}\right)$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current of both converters combined.

$$I_{RMS(MAX)} = \frac{I_{O1(MAX)} + I_{O2(MAX)}}{2}$$

Configuration	Output Voltage	Inductor	Slope Compensation
0.6V adjustable with external resistive divider	0.6V-2.0V	2.2µH	0.6A/µs
	2.5V	3.3µH	
	3.3V	4.7µH	

Table 1: Inductor Values.

This equation also makes the worst-case assumption that both converters are operating at 50% duty cycle synchronized.

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations. It is at maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = D \cdot (1 - D) = 0.5^2 = 0.25$$

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2513. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize the stray inductance, the capacitor should be placed as close as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C3 and C9) can be seen in the evaluation board layout in Figures 3 and 4. Since decoupling must be as close to the input pins as possible it is necessary to use two decoupling capacitors, one for each converter.

A Laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires along with the low ESR ceramic input capacitor can create a high Q network that may effect the converter performance.

This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short printed circuit board trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not effect the converter performance, a high ESR tantalum or aluminum electrolytic (C10 of Figure 2) should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7µF to 10µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current the ceramic output capacitor alone supplies the load current until the loop responds. As the loop responds the inductor current increases to match the load current demand. This typically takes two to three switching cycles and can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 4.7µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot spot temperature.

Adjustable Output Resistor Selection

Resistors R1 through R4 of Figure 1 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string, the minimum suggested value for R2 and R4 is 59kΩ. Although a larger value will reduce the quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 2 summarizes the resistor values for various output voltages with R2 and R4 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2 = \left(\frac{1.5V}{0.6V} - 1\right) \cdot 59k\Omega = 88.5k\Omega$$

With an external feedforward capacitor (C4 and C5 of Figure 2) the AAT2513 delivers enhanced transient response for extreme pulsed load applications. The addition of the feedforward capacitor typically requires a larger output capacitor (C1 and C2) for stability.

V_{OUT} (V)	R2, R4 = 59kΩ R1, R3 (kΩ)	R2, R4 = 221kΩ R1, R3 (kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.3	265	1000

Table 2: Feedback Resistor Values.

Thermal Calculations

There are three types of losses associated with the AAT2513 converter: switching losses, conduction losses, and quiescent current losses. The conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. The switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the dual converter losses is given by:

$$P_{TOTAL} = \frac{I_{O1}^2 \cdot (R_{DSON(HS)} \cdot V_{O1} + R_{DSON(LS)} \cdot [V_{IN} - V_{O1}])}{V_{IN}}$$

$$+ \frac{I_{O2}^2 \cdot (R_{DSON(HS)} \cdot V_{O2} + R_{DSON(LS)} \cdot [V_{IN} - V_{O2}])}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot [I_{O1} + I_{O2}] + 2 \cdot I_Q) \cdot V_{IN}$$

I_Q is the AAT2513 quiescent current for one channel and t_{SW} is used to estimate the full load switching losses.

For the condition where channel one is in dropout at 100% duty cycle the total device dissipation reduces to:

$$P_{TOTAL} = I_{O1}^2 \cdot R_{DSON(HS)}$$

$$+ \frac{I_{O2}^2 \cdot (R_{DSON(HS)} \cdot V_{O2} + R_{DSON(LS)} \cdot [V_{IN} - V_{O2}])}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot I_{O2} + 2 \cdot I_Q) \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the QFN33-12 package which is 28°C/W to 50°C/W minimum.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

PCB Layout

Use the following guidelines to insure a proper layout:

1. Due to the pin placement of V_{IN} for both converters, proper decoupling is not possible with just one input capacitor. The input capacitors C3 and C9 should connect as closely as possible to the respective VIN and GND as shown in Figure 3.
2. Connect the output capacitor and inductor as closely as possible. The connection of the inductor to the LX pin should also be as short as possible.
3. The feedback trace should be separate from any power trace and connect as close as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. Place the external feedback resistors as close as possible to the FB pin. This prevents noise from being coupled into the high impedance feedback node.
4. Keep the resistance of the trace from the load return to GND to a minimum. This minimizes any error in DC regulation due to potential differences of the internal signal ground and the power ground.
5. For good thermal coupling, PCB vias are required from the pad for the QFN paddle to the ground plane. The via diameter should be 0.3mm to 0.33mm and positioned on a 1.2 mm grid.

Design Example

Specifications

V_{O1} 2.5V @ 600mA (adjustable using 0.6V version), pulsed load ΔI_{LOAD} = 300mA

V_{O2} 1.8V @ 600mA (adjustable using 0.6V version), pulsed load ΔI_{LOAD} = 300mA

V_{IN} 2.7V to 4.2V (3.6V nominal)

F_S 1.7 MHz

T_{AMB} 85°C

1.8V V_{O1} Output Inductor

$$L1 = 1.2\frac{\mu s}{A} \cdot V_{O1} = 1.2\frac{\mu s}{A} \cdot 1.8V = 2.2\mu H$$ (see table 1).

For Sumida CDRH2D11 2.2µH DCR = 98mΩ.

$$\Delta I1 = \frac{V_{O1}}{L \cdot F} \cdot \left(1 - \frac{V_{O1}}{V_{IN}}\right) = \frac{2.5V}{3.3\mu H \cdot 1.7MHz} \cdot \left(1 - \frac{2.5V}{4.2V}\right) = 230mA$$

$$I_{PK1} = I_{O1} + \frac{\Delta I1}{2} = 0.4A + 0.115A = 0.515A$$

$$P_{L1} = I_{O1}^2 \cdot DCR = 0.6A^2 \cdot 123m\Omega = 44mW$$

2.5V V_{O2} Output Inductor

$$L1 = 1.2\frac{\mu s}{A} \cdot V_{O1} = 1.2\frac{\mu s}{A} \cdot 2.5V = 3.3\mu H$$ (see table 1).

For Sumida inductor CDRH2D11 3.3µH DCR = 123mΩ.

$$\Delta I2 = \frac{V_{O2}}{L \cdot F} \cdot \left(1 - \frac{V_{O2}}{V_{IN}}\right) = \frac{2.5V}{3.3\mu H \cdot 1.7MHz} \cdot \left(1 - \frac{2.5V}{4.2V}\right) = 230mA$$

$$I_{PK2} = I_{O2} + \frac{\Delta I2}{2} = 0.4A + 0.115A = 0.515A$$

$$P_{L2} = I_{O2}^2 \cdot DCR = 0.6A^2 \cdot 123m\Omega = 44mW$$

1.8V Output Capacitor

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.3A}{0.2V \cdot 1.7MHz} = 4.8\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.8V \cdot (4.2V - 1.8V)}{2.2\mu H \cdot 1.7MHz \cdot 4.2V} = 31mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (31mA)^2 = 4.8\mu W$$

2.5V Output Capacitor

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.3A}{0.2V \cdot 1.7MHz} = 4.8\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{2.5V \cdot (4.2V - 2.5V)}{3.3\mu H \cdot 1.7MHz \cdot 4.2V} = 67mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (67mA)^2 = 22\mu W$$

Input Capacitor

Input Ripple V_{PP} = 25mV.

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{O1} + I_{O2}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{25mV}{1.2A} - 5m\Omega\right) \cdot 4 \cdot 1.7MHz} = 10\mu F$$

$$I_{RMS(MAX)} = \frac{I_{O1} + I_{O2}}{2} = 0.6Arms$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (0.6A)^2 = 0.8mW$$

AAT2513 Losses

The maximum dissipation occurs at dropout where V_{IN} = 2.7V. All values assume an 85°C ambient and a 120°C junction temperature.

$$P_{TOTAL} = \frac{I_{O1}^2 \cdot (R_{DSON(HS)} \cdot V_{O1} + R_{DSON(LS)} \cdot (V_{IN} - V_{O1})) + I_{O2}^2 \cdot (R_{DSON(HS)} \cdot V_{O2} + R_{DSON(LS)} \cdot (V_{IN} - V_{O2}))}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot I_{O2} + 2 \cdot I_Q) \cdot V_{IN}$$

$$= \frac{0.6^2 \cdot (0.725\Omega \cdot 2.5V + 0.7\Omega \cdot (2.7V - 2.5V)) + 0.6^2 \cdot (0.725\Omega \cdot 1.8V + 0.7\Omega \cdot (2.7V - 1.8V))}{2.7V}$$

$$+ (5ns \cdot 1.7MHz \cdot 0.6A + 60\mu A) \cdot 2.7V = 533mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 533mW = 111°C$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (28°C/W) \cdot 533mW = 100°C$$

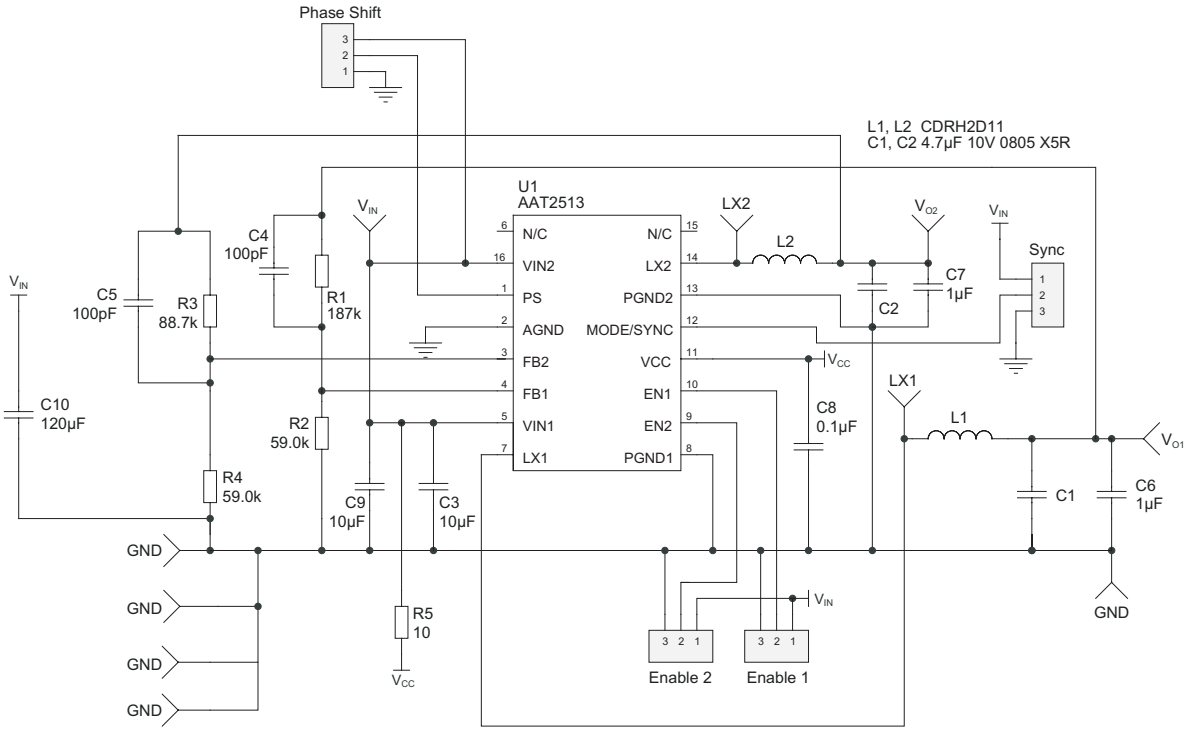


Figure 2: AAT2513 Evaluation Board Schematic[1].

1. For enhanced transient configuration C5, C4 = 100pF and C1, C2 = 10µF.

Adjustable Version (0.6V device)	R2, R4 = 59kΩ	R2, R4 = 221kΩ[1]	
V_{OUT} (V)	R1, R3 (kΩ)	R1, R3 (kΩ)	L1, L2 (µH)
0.8	19.6	75.0	1.0 - 1.5
0.9	29.4	113	1.0 - 1.5
1.0	39.2	150	1.0 - 1.5
1.1	49.9	187	1.0 - 1.5
1.2	59.0	221	1.0 - 1.5
1.3	68.1	261	1.0 - 1.5
1.4	78.7	301	2.2
1.5	88.7	332	2.2
1.8	118	442	2.2
1.85	124	464	2.2
2.0	137	523	3.3
2.5	187	715	3.3
3.3	265	1000	4.7
Fixed Version	**R2, R4 not used**		
V_{OUT} (V)	R1, R3 (kΩ)		L1, L2 (µH)
0.6-3.3V	zero		2.2

Table 5: Evaluation Board Component Values.

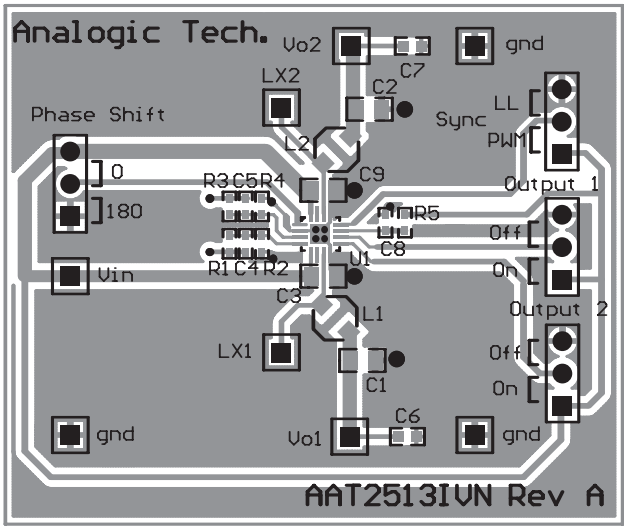


Figure 3: AAT2513 Evaluation Board Top Side.

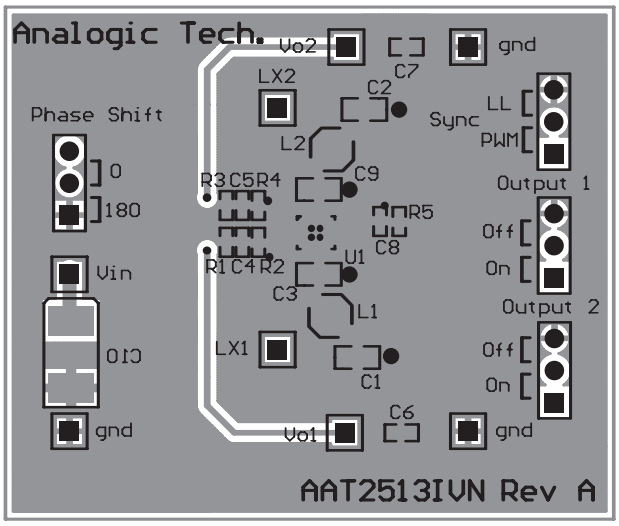


Figure 4: AAT2513 Evaluation Board Bottom Side.

1. For reduced quiescent current, R2 and R4 = 221kΩ.

Manufacturer	Part Number	Inductance (µH)	Max DC Current (A)	DCR (Ω)	Size (mm) LxWxH	Type
Sumida	CDRH2D11	1.5	1.48	0.068	3.2x3.2x1.2	Shielded
Sumida	CDRH2D11	2.2	1.27	0.098	3.2x3.2x1.2	Shielded
Sumida	CDRH2D11	3.3	1.02	0.123	3.2x3.2x1.2	Shielded
Sumida	CDRH2D11	4.7	0.88	0.170	3.2x3.2x1.2	Shielded
Taiyo Yuden	CBC2518T	1.0	1.2	0.08	2.5x1.8x1.8	Wire Wound Chip
Taiyo Yuden	CBC2518T	2.2	1.1	0.13	2.5x1.8x1.8	Wire Wound Chip
Taiyo Yuden	CBC2518T	4.7	0.92	0.2	2.5x1.8x1.8	Wire Wound Chip
Taiyo Yuden	CBC2016T	2.2	0.83	0.2	2.0x1.6x1.6	Wire Wound Chip

Table 3: Typical Surface Mount Inductors.

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
Murata	GRM219R61A475KE19	4.7µF	10V	X5R	0805
Murata	GRM21BR60J106KE19	10µF	6.3V	X5R	0805
Murata	GRM21BR60J226ME39	22µF	6.3V	X5R	0805

Table 4: Surface Mount Capacitors.

Ordering Information

Package	Voltage		Marking[1]	Part Number (Tape and Reel)[2]
	Channel 1	Channel 2		
QFN33-16	0.6V	0.6V	UFXYY	AAT2513IVN-AA-T1

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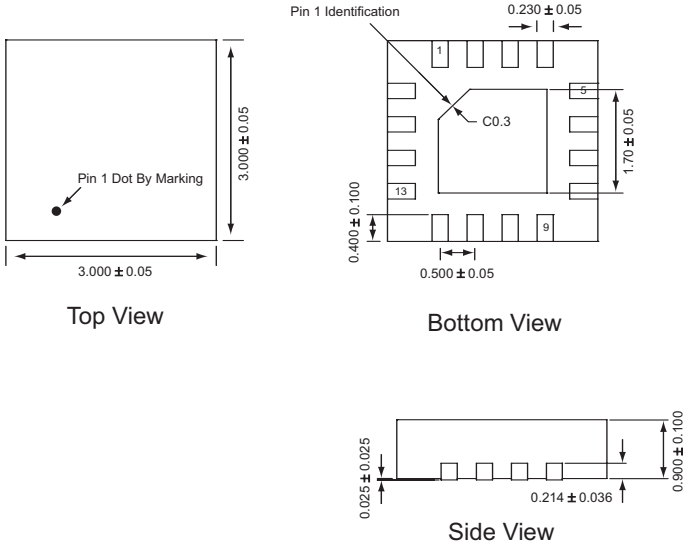
Legend	
Voltage	Code
Adjustable (0.6V)	A
1.5	G
1.8	I
1.9	Y
2.5	N
2.6	O
2.7	P
2.8	Q
2.85	R
2.9	S
3.0	T
3.3	W

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

Package Information[1]

QFN33-16



All dimensions in millimeters.

1. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

Advanced Analogic Technologies, Inc.
830 E. Arques Avenue, Sunnyvale, CA 94085
Phone (408) 737-4600
Fax (408) 737-4611