RAD Tolerant ACT–RS128K32 High Speed 4 Megabit SRAM Multichip Module

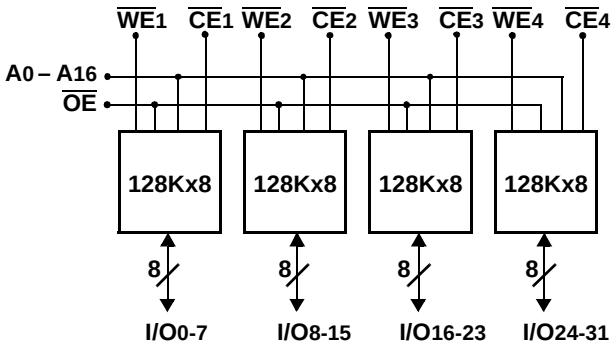
Preliminary

Features

- 4 Low Power CMOS 128K x 8 SRAMs in one MCM
- Overall configuration as 128K x 32
- Tolerant to 30KRad (Si)
- Latch-up Immunity to 112MeV/(mg/cm^2)
- Input and Output TTL Compatible
- 35 & 45ns Access Times
- Full Military (-55°C to +125°C) Temperature Range
- For Class K devices per MIL-PRF-38534 - Consult Factory
- +5V Power Supply
- Choice of 4 Hermetically sealed Co-fired Packages:
  - 68–Lead, Low Profile CQFP (F1), 1.56"SQ x .140"max
  - 68–Lead, Dual-Cavity CQFP (F2), .88"SQ x .20"max (.18"max thickness available, contact factory for details) *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
  - 66–Lead, PGA-Type (P1), 1.385"SQ x .245"max
- Internal Decoupling Capacitors

AEROFLEX CIRCUIT TECHNOLOGY
www.aeroflex.com/act1.htm

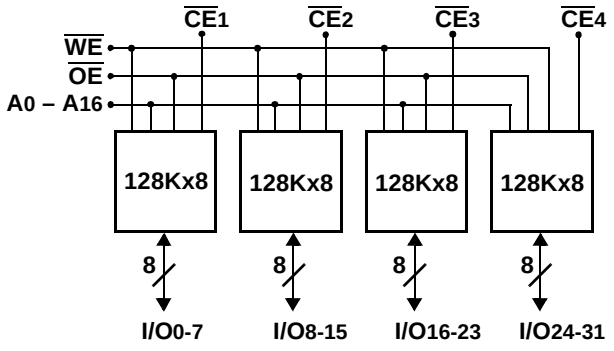
Block Diagram – PGA Type Package(P1) & CQFP(F2)



Pin Description

I/O0-31	Data I/O
A0–16	Address Inputs
WE1–4	Write Enables
CE1–4	Chip Enables
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

Block Diagram – CQFP(F1)



Pin Description

I/O0-31	Data I/O
A0–16	Address Inputs
WE	Write Enable
CE1–4	Chip Enables
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

General Description

The ACT–RS128K32 is a High Speed 4 megabit CMOS SRAM Multichip Module (MCM) designed for full temperature range, military, space, or high reliability mass memory and fast cache applications.

The MCM can be organized as a 128K x 32 bits, 256K x 16 bits or 512k x 8 bits device and is input and output TTL compatible. Writing is executed when the write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are low. Reading is accomplished when $\overline{WE}$ is high and $\overline{CE}$ and output enable ($\overline{OE}$) are both low. Access time grades of 35ns and 45ns maximum are standard.

The +5 Volt power supply version is standard.

The products are designed for operation over the temperature range of -55°C to +125°C and screened under the full military environment. DESC Standard Military Drawing (SMD) part numbers are pending.

The ACT-RS128K32 is manufactured in Aeroflex's 80,000ft^2 MIL-PRF-38534 certified facility in Plainview, N.Y.

Absolute Maximum Ratings

Symbol	Rating	Range	Units
T_C	Case Operating Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_D	Maximum Package Power Dissipation		
	F1 & P1 Packages	4.4	W
	F2 Package	3.3	W
$Ø_{J-C}$	Hottest Die, Max Thermal Resistance - Junction to Case		
	F1 & P1 Packages	2.0	°C/W
	F2 Package	8.0	°C/W
V_G	Maximum Signal Voltage to Ground	-0.5 to +7	V
T_L	Maximum Lead Temperature (10 seconds)	300	°C

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V

Truth Table

Mode	CE	OE	WE	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Read	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data In	Active

Capacitance

(f = 1MHz, T_C = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	A_0 – A_{16} Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
C_{WE}	CQFP(F1) Package	50	pF
	PGA(P1) and CQFP(F2) Packages	20	pF
C_{CE}	Chip Enable Capacitance	20	pF
$C_{I/O}$	I/O_0 – I/O_{31} Capacitance	20	pF

Capacitance is guaranteed by design but not tested.

DC Characteristics

(4.5Vdc≤ V_{CC} ≤ 5.5Vdc, V_{SS} = 0V, T_C = -55°C to +125°C, Unless otherwise specified)

Parameter	Sym	Conditions	–035		–045		Units
			Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = 0 or V_{CC}		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = 0 or V_{CC}		10		10	µA
Operating Supply Current 32 Bit Mode	I_{CC}x32	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5 MHz, V_{CC} = Max, CMOS Compatible		500		600	mA

DC Characteristics (Continued)

(4.5Vdc≤ V_{CC} ≤ 5.5Vdc, V_{SS} = 0V, T_C = -55°C to +125°C, Unless otherwise specified)

Parameter	Sym	Conditions	–035 Min	–035 Max	–045 Min	–045 Max	Units
Standby Current	I_{SB}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5 MHz, V_{CC} = Max, CMOS Compatible		30		30	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA, V_{CC} = Min	2.4		2.4		V

AC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, T_C = -55°C to +125°C)

Read Cycle

Parameter	Sym	–035 Min	–035 Max	–045 Min	–045 Max	Units
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time	t_{AA}		35		45	ns
Chip Enable Access Time	t_{ACE}		35		45	ns
Chip Enable to Output in Low Z*	t_{CLZ}	3		3		ns
Output Enable to Output in Low Z*	t_{OLZ}	0		0		ns
Chip Deselect to Output in High Z*	t_{CHZ}		20		20	ns
Output Disable to Output in High Z*	t_{OHZ}		10		15	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Sym	–035 Min	–035 Max	–045 Min	–045 Max	Units
Write Cycle Time	t_{WC}	35		45		ns
Chip Enable to End of Write	t_{CW}	25		35		ns
Address Valid to End of Write	t_{AW}	25		35		ns
Data Valid to End of Write	t_{DW}	18		20		ns
Write Pulse Width	t_{WP}	25		35		ns
Address Setup Time	t_{AS}	0		0		ns
Write to Output in High Z *	t_{WHZ}		10		15	ns
Data Hold from Write Time	t_{DH}	0		0		ns
Address Hold Time	t_{AH}	0		0		ns

* Parameters guaranteed by design but not tested

Data Retention Electrical Characteristics (Special Order Only)

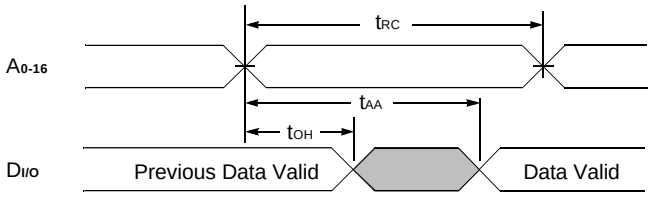
(T_C = -55°C to +125°C)

Parameter	Sym	Test Conditions	All Speeds Min	All Speeds Max	Units
V_{CC} for Data Retention	V_{DR}	$\overline{CE}$ ≥ V_{CC} – 0.2V	2	5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V, 35 & 45ns		4	mA

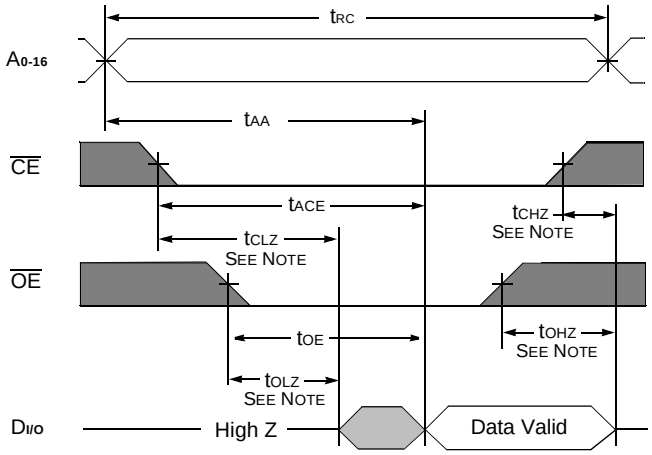
Timing Diagrams

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



Read Cycle 2 ($\overline{WE}$ = V_{IH})

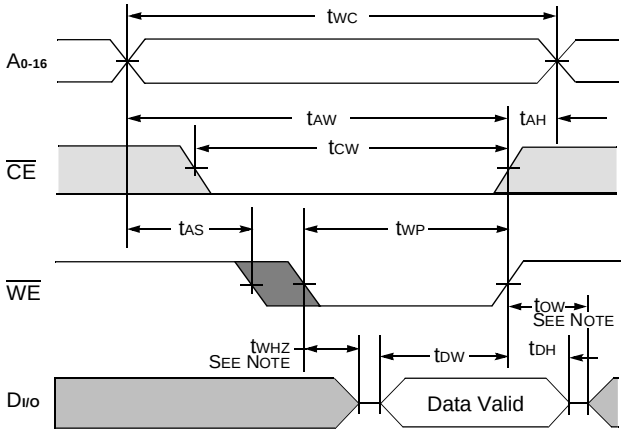


UNDEFINED DON'T CARE

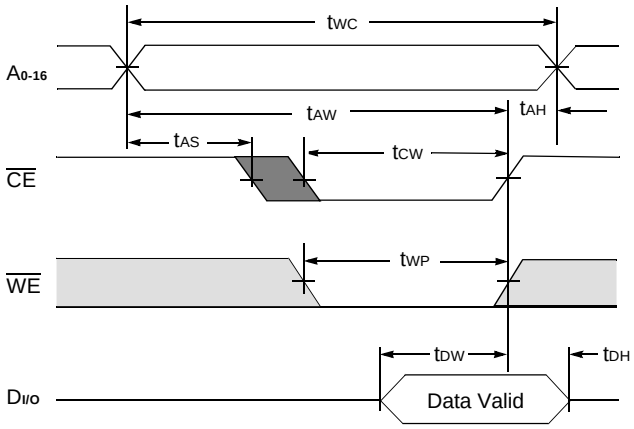
Note: Guaranteed by design, but not tested.

Write Cycle Timing Diagrams

Write Cycle 1 ($\overline{WE}$ Controlled, $\overline{OE}$ = V_{IL})

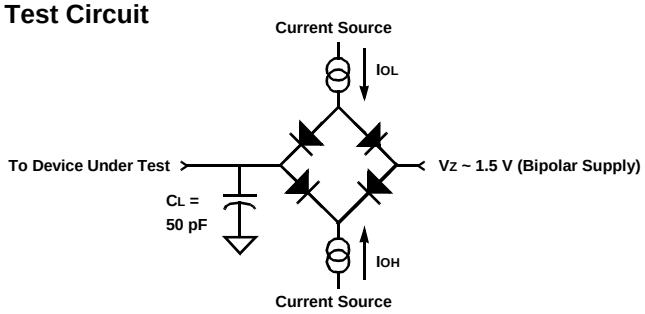


Write Cycle 2 ($\overline{CE}$ Controlled, $\overline{OE}$ = V_{IH})



Note: Guaranteed by design, but not tested.

AC Test Circuit



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V
Output Lead Capacitance	50	pF

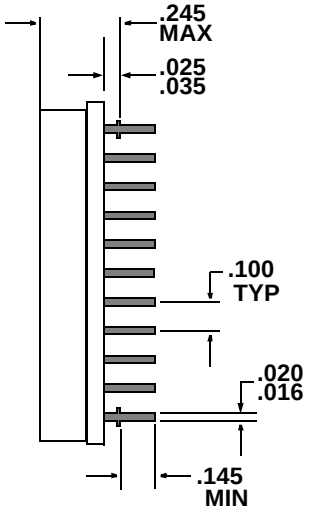
Notes:
1) V_Z is programmable from -2V to +7V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance Z_O = 75Ω. 4) V_Z is typically the midpoint of V_{OH} and V_{OL}. 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

Pin Numbers & Functions

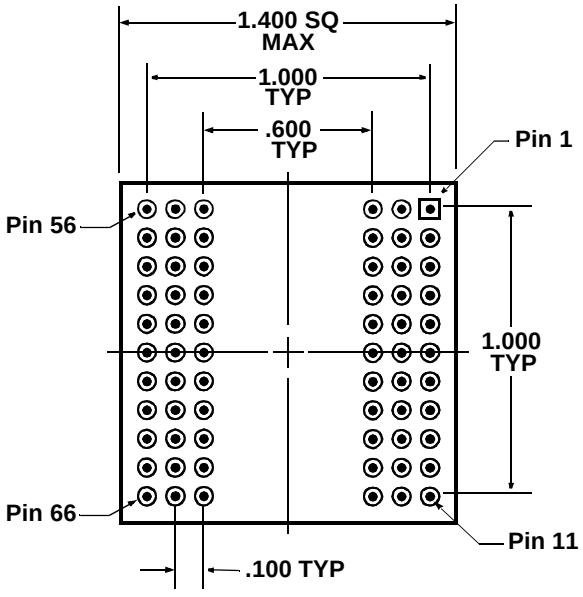
66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O_8	18	A_{12}	35	I/O_{25}	52	$\overline{WE}_3$
2	I/O_9	19	Vcc	36	I/O_{26}	53	$\overline{CE}_3$
3	I/O_{10}	20	$\overline{CE}_1$	37	A_6	54	GND
4	A_{13}	21	NC	38	A_7	55	I/O_{19}
5	A_{14}	22	I/O_3	39	NC	56	I/O_{31}
6	A_{15}	23	I/O_{15}	40	A_8	57	I/O_{30}
7	A_{16}	24	I/O_{14}	41	A_9	58	I/O_{29}
8	NC	25	I/O_{13}	42	I/O_{16}	59	I/O_{28}
9	I/O_0	26	I/O_{12}	43	I/O_{17}	60	A_0
10	I/O_1	27	$\overline{OE}$	44	I/O_{18}	61	A_1
11	I/O_2	28	NC	45	V_{CC}	62	A_2
12	$\overline{WE}_2$	29	$\overline{WE}_1$	46	$\overline{CE}_4$	63	I/O_{23}
13	$\overline{CE}_2$	30	I/O_7	47	$\overline{WE}_4$	64	I/O_{22}
14	GND	31	I/O_6	48	I/O_{27}	65	I/O_{21}
15	I/O_{11}	32	I/O_5	49	A_3	66	I/O_{20}
16	A_{10}	33	I/O_4	50	A_4		
17	A_{11}	34	I/O_{24}	51	A_5		

"P1" — 1.385" SQ PGA Type Package Standard

Side View



Bottom View

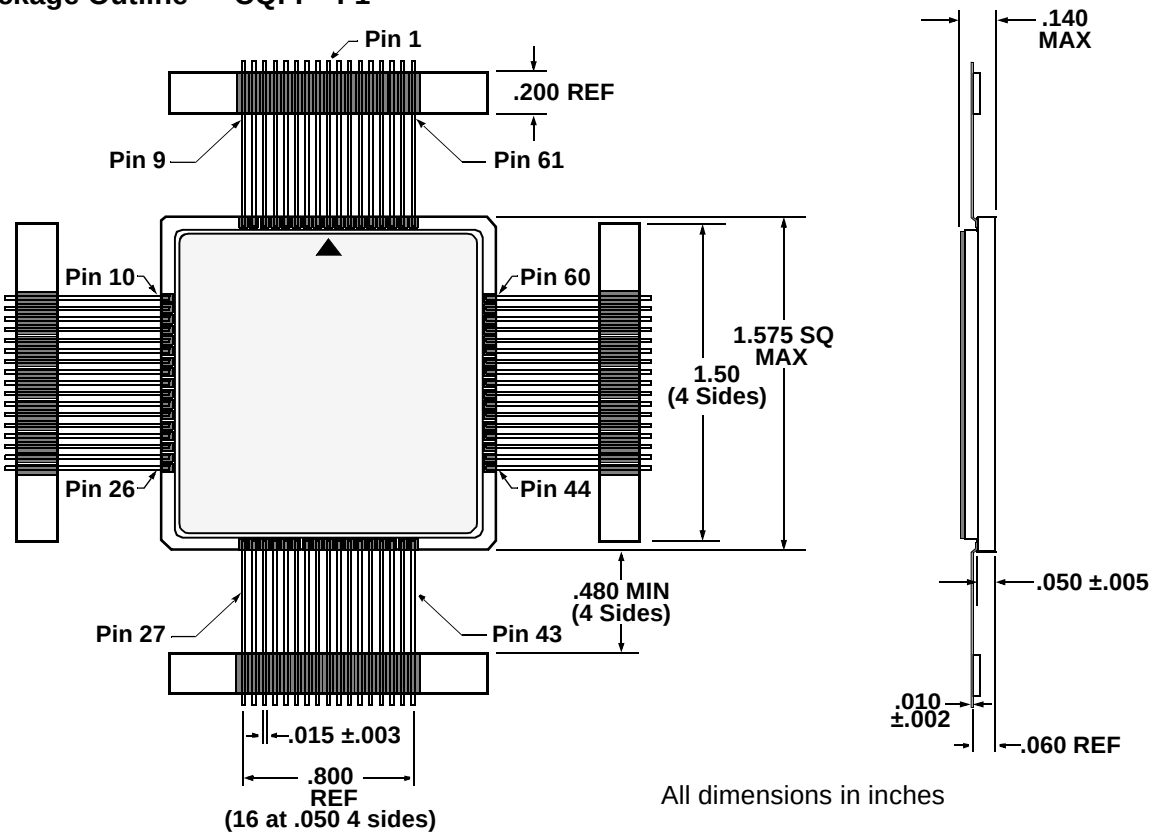


All dimensions in inches

Pin Numbers & Functions

68 Pins — CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_1$	19	I/O_8	36	$\overline{CE}_4$	53	I/O_{23}
3	A_5	20	I/O_9	37	NC	54	I/O_{22}
4	A_4	21	I/O_{10}	38	NC	55	I/O_{21}
5	A_3	22	I/O_{11}	39	NC	56	I/O_{20}
6	A_2	23	I/O_{12}	40	NC	57	I/O_{19}
7	A_1	24	I/O_{13}	41	NC	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE}$
17	I/O_7	34	$\overline{CE}_2$	51	I/O_{24}	68	$\overline{CE}_3$

Package Outline — CQFP "F1"



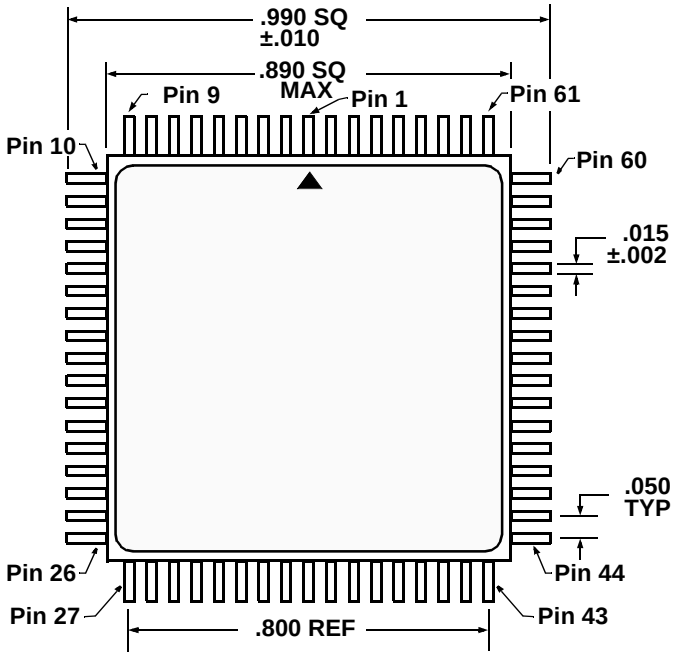
All dimensions in inches

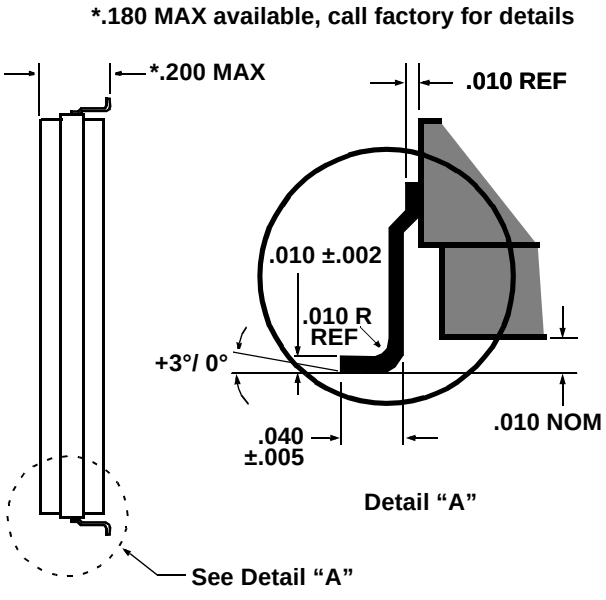
Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O_8	36	$\overline{CE}_2$	53	I/O_{23}
3	A_5	20	I/O_9	37	NC	54	I/O_{22}
4	A_4	21	I/O_{10}	38	$\overline{WE}_2$	55	I/O_{21}
5	A_3	22	I/O_{11}	39	$\overline{WE}_3$	56	I/O_{20}
6	A_2	23	I/O_{12}	40	$\overline{WE}_4$	57	I/O_{19}
7	A_1	24	I/O_{13}	41	NC	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE1}$
17	I/O_7	34	$\overline{CE}_1$	51	I/O_{24}	68	$\overline{CE}_4$

Package Outline — Dual-Cavity CQFP "F2"

Top View





All dimensions in inches

Note: Metallic lids and walls – both sides

Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT–RS128K32N–035F1Q	5962–TBD	35ns	1.56"sq CQFP
ACT–RS128K32N–035F2Q	5962–TBD		.88"sq CQFP
ACT–RS128K32N–035P1Q	5962–TBD		1.385"sq PGA-Type
ACT–RS128K32N–045F1Q	5962–TBD	45ns	1.56"sq CQFP
ACT–RS128K32N–045F2Q	5962–TBD		.88"sq CQFP
ACT–RS128K32N–045P1Q	5962–TBD		1.385"sq PGA-Type

Model Number Breakdown

ACT– RS 128K 32 N– 035 F2 M

Aeroflex Circuit Technology

Memory Type

RS = Radiation Tolerant SRAM

Memory Depth, Locations

Memory Width, Bits

Options

N = None

Memory Speed, ns

Screening

C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screened *
Q = MIL-STD-883 Compliant/SMD if applicable

Package Type & Size

Surface Mount Packages	*Thru-Hole Packages*
F1 = 1.56"SQ 68 Pin CQFP	P1 =1.385"SQ PGA 66 Pins
F2 = .88"SQ 68 Pin Dual-Cavity CQFP	

* **Screened to the individual test methods of MIL-STD-883**

Specifications subject to change without notice

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