ACTS20MS

Radiation Hardened Dual 4-Input NAND Gate

April 1995

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose 300K RAD (Si)
- Single Event Upset (SEU) Immunity <1 x 10^{-10} Errors/Bit-Day (Typ)
- SEU LET Threshold >80 MEV-cm^2/mg
- Dose Rate Upset >10^{11} RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55^{o}C to +125^{o}C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2V Min
- Input Current ≤1μA at VOL, VOH

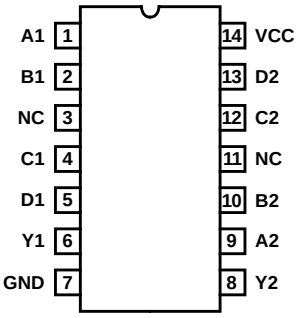
Description

The Intersil ACTS20MS is a radiation hardened dual 4-input NAND gate. A low on any input forces the output to a high logic state.

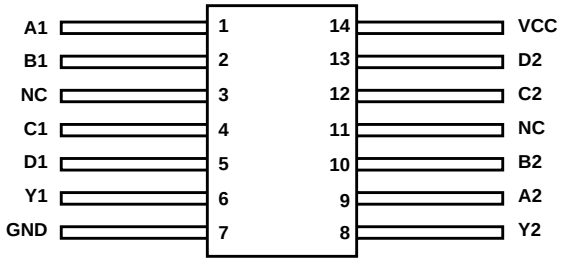
The ACTS20MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of the radiation hardened, high-speed, CMOS/SOS Logic Family.

Pinouts

14 LEAD CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T14, LEAD FINISH C
TOP VIEW



14 LEAD CERAMIC FLATPACK
MIL-STD-1835 DESIGNATOR, CDFP3-F14, LEAD FINISH C
TOP VIEW



Ordering Information

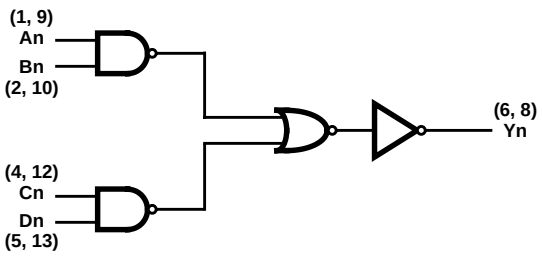
PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
ACTS20DMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	14 Lead SBDIP
ACTS20KMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	14 Lead Ceramic Flatpack
ACTS20D/Sample	+25^{o}C	Sample	14 Lead SBDIP
ACTS20K/Sample	+25^{o}C	Sample	14 Lead Ceramic Flatpack
ACTS20HMSR	+25^{o}C	Die	Die

Truth Table

INPUTS				OUTPUT
An	Bn	Cn	Dn	Yn
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

NOTE: L = Logic Level Low, H = Logic level High, X = Don't Care

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Spec Number **518824**
File Number **3611**